BPM ELECTRONICS UPGRADE FOR THE FERMILAB H- LINAC BASED UPON CUSTOM DOWNCONVERTER ELECTRONICS *

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Abstract

As part of the Fermilab Proton Improvement Plan [1], the readout electronics for the beam position monitors (BPMs) in the Fermilab H^- Linac [2] have been upgraded. The new custom electronics provide a low cost solution to process the 2nd harmonic of the 805 MHz RF. A single four-channel NIM-bin module is used to readout each four-plate stripline BPM pickup. Each module is locked to the external 805 MHz machine reference from the low level RF. A number of measurements at each BPM are provided, including average horizontal and vertical position, average intensity, and average relative phase for variable pulse lengths up to 50 µsec. The system is being exploited in a number of ways with new operations applications.

INTRODUCTION

New readout electronic modules for all 67 BPMs in the Linac and in the Booster injection line have been installed. These modules are housed in NIM bins inside 15 crates throughout the Linac and Booster equipment galleries, see Fig. 1. Up to six modules per crate are used. Each module has four input channels which are connected directly to the four BPM striplines.

The specification for this system is to provide a position resolution of 0.1 mm with a long-term stability of 0.25 mm, and phase resolution of 0.2º. These specifications have been achieved.

In this paper, the hardware design is covered first, and then the microcontroller and the front end software. Next, the high-level, operations software developed for this system is outlined. Finally, the measured resolution of the new BPMs in the operating Fermilab Linac is shown.

HARDWARE

A block diagram of a single input channel along with the key timing components is shown in Fig. 2.

Timing and Control

Each board receives an 805 MHz reference signal from the Linac RF system, which is used to generate all on-board clocks and the phase-locked reference signals. There are three RJ-45 connectors on the front panel: One is for the Ethernet and the other two are for a local serial link among the modules.

The Master module is identified by a 50 Ω terminator inserted into the front panel of a module. Any module can be a Master, but only one per crate is so designated. The Master is connected to the Ethernet and is responsible for sending triggers and data requests to all the modules in the crate and for gathering binary data and then distributing it over the Ethernet. The Master also receives the Fermilab 10 MHz clock system, TCLK [5], from which it decodes machine events and generates the trigger signals.

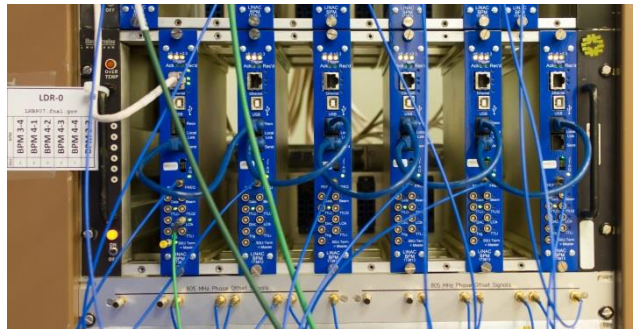

Figure 1: A typical installation of Linac BPM modules.

Signal Path

The input signal path consists of a band pass filter (290-490 MHz) to select the 2nd beam harmonic, an analog quadrature mixer (Analog Devices AD8348), and a dual channel 12-bit ADC (Linear Technologies LTC-2265) to digitize the in-phase and quadrature signals. There is also a 20 dB directional coupler used to inject a test signal and a 3 dB pad to limit the out-of-band reflections from the band pass filter. The local oscillator (LO) for the mixers is generated to produce an intermediate frequency (IF) of 3.125 MHz. There is a 5 MHz low pass filter on the IF signals. The mixers include a 40 dB variable gain amplifier in order to increase the usable dynamic range.

The IF is digitized at 50 MHz (805 MHz/16) with the 12-bit digitizers. The digitizer clock is phase locked to the RF reference, which simplifies the digital portion of the

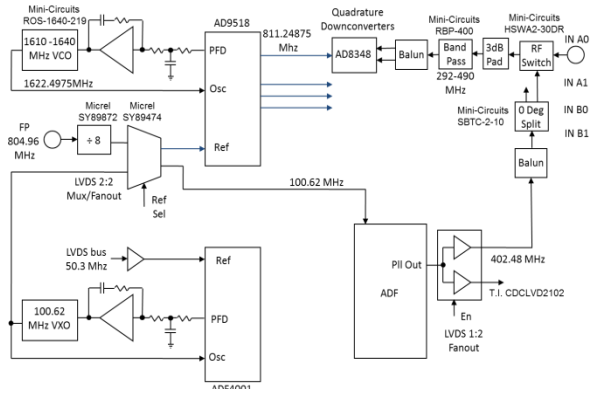

Figure 2: BPM Module Signal Path.

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down conversion. The FPGA does not need to track any phase drift between the IF input and the digitizer clock.

A fifth mixer is employed to measure the phase of one output of the LO driver with respect to the input RF reference. This phase difference is subtracted from the four phases derived from the plate signals. This differential measurement is robust with respect to the various sources of drift. A bench measurement shows a phase resolution of 0.05º RMS of the 402.5 MHz signal when averaged over an 8 µs interval. Assuming a Gaussian error distribution, a digitization sample has a phase uncertainty of ½º, or 4 picoseconds.

Digital Section

Data from the digitizer is processed by an Altera Cyclone II FPGA. Up to 40 µs of raw data can be stored in the FPGA static memory. Phases and magnitudes are calculated at 50 MS/sec using pipelined Cordic rotators. The position is calculated using a simple difference-over-sum algorithm. This algorithm could be changed to account for non-linearities in the BPMs, but it is not required at this time. Attached to the FPGA is 64 MB of low-power double data rate (DDR) random-access memory (RAM) operating at 100 MHz. This allows considerable diagnostic data to be saved.

The FPGA data are connected to an on-board microcontroller, an ARM Cortex-M3 processor operating at 80 MHz. The FPGA contains a memory controller and presents DDR RAM data on demand to the microcontroller bus. The microcontroller is used to respond to requests originating from Ethernet and to send data over the local bus or Ethernet, see below. The 100 Mbit Ethernet interface is attached to the microcontroller bus. This chip contains hardware support of multiple protocols and 128 kB of buffer memory.

Each module contains 1 kB of non-volatile flash in which is stored configuration parameters.

MICROCONTROLLER SOFTWARE

Software for the microcontroller in the BPM modules is written in C using IAR Embedded Workbench for ARM. This software is responsible for the configuration of the module, for the communications among the modules within a NIM crate and for the communications between the modules and the outside world via Ethernet.

On power up a data link between the Master and the slave modules is initialized. The Master is *Module 0* and the slaves are assigned as *Module 1* through *Module 5*.

Each module has four low-voltage differential signal (LVDS) serial data links at 1.48 Mbytes/sec, which are:

- 2 transmitters
  - Binary data return path
  - ASCII data return path
- 2 receivers for,
  - ASCII commands from the expert or the OAC
  - Reference clock and event timing codes

Each Master services up to three Telnet sockets over the Ethernet. These sockets are used to,

- Interact with an expert for module configuration and control. (TCP/IP)
- Interact with the Linac Control System through a customized binary protocol (see below). (UDP/IP)
- Interact with the Open-access Client (OAC) front end (see below). (TCP/IP).

Additionally, each module has a serial port, implemented through a USB connection. This port allows for the initial configuration of a module and is a fully reliable connection in case of a problem.

FRONT END SOFTWARE

The Fermilab Linac runs synchronously to the Booster at 15 Hz and the Linac control system [3] runs synchronously to the Linac.

The following data are sourced by the Linac BPM system at each and every BPM at 15Hz:

- Five scalar, floating-point readings
  - Horizontal and vertical positions
  - Beam phase and beam current
  - Pulse length
- Decimated data vectors of the beam positions (H and V) within the Linac beam pulse.

A local application [4] in Linac control system front ends named BPMD handles all the interactions between a Linac front end and a Master module. This application runs for a few milliseconds after every 15 Hz clock tick. Each instance of BPMD communicates with one BPM Master via UDP over the private Accelerator Controls Ethernet. All data are returned to BPMD by the 24 milliseconds mark in the 66.7 millisecond 15 Hz cycle. There are 15 instances of BPMD.

Many BPMD messages are sent in one UDP datagram. A reply message is always less than 1 Kbyte (plus headers) so that a datagram fits in a single network frame. Consequently the receiving front end does not have deal with dropped fragments; it will know at the end of the timeout if a packet has not arrived in time.

Table 1: Java Operations Applications

Application	Summary
Linac BPM Display	Show summary data from the BPMs during normal operations
Linac BPM Expert	Display and control of the registers, flash memory and calibration of the BPMs, one BPM at a time.
Linac BPM Expert Overview	Shows the value of one register for each BPM in the entire system.
Linac BPM Multiplex WF	Control the setup and display of multiplexed waveforms
Linac BPM Sync DAQ	Control and display of the Synchronous DAQ Waveforms throughout the system.
Linac BPM All Readings	Show the readings and the RMS deviations of the scalar values produced by all the BPMs.

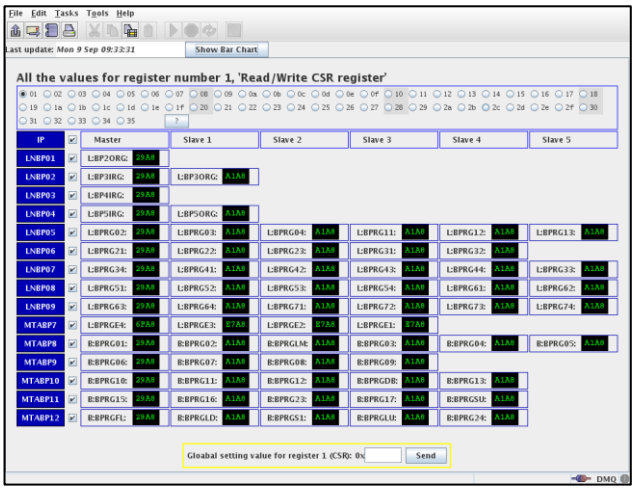

Figure 3: BPM Overview Application screen shot.

Since the front end and the Master are sensitive to TCLK, event-based requests for data are supported. Also there is support for time stamps on the data.

SOFTWARE FRONT END

A software front end has been implemented in the Fermilab Open-access client (OAC) framework [6]. This front end communicates with each of the BPM Masters via TCP/IP over Ethernet to provide 1Hz access to the registers and the flash memory in each module, and to the various large vector data sets provided by the modules. A single OAC instance handles all the BPMs in the Linac.

OPERATIONS SOFTWARE

Several operations applications have been deployed, all written in Java, see Table 1.

A screen shot of the Linac BPM Expert Overview application is shown, in Fig. 3. This capture shows the value of the main control register for each of the BPM modules installed in the Linac. The proper value for this register is `0x29A8` for the Master and `0xA1A8` for the slaves. Note how this display shows the modules in `MTABP7` are incorrect. The correct values can be set through the box at the bottom of the page. Each of the 53 (0x35) registers can be shown using the radio button array.

The Linac BPM Expert application gives the expert command and control over one module's registers. Many features are implemented here, like save/restore, data plotting, flash memory control and calibration.

RESOLUTION MEASUREMENTS

Data have been collected from the BPMs at each 20 µsec Linac beam pulse over a 4 hour period with no changes in the machine. The resolution has been calculated from these data using the Singular Value Decomposition (SVD) technique [7]. The results for both horizontal (blue) and vertical (red) position are shown in Fig. 4. The specified 0.1 mm resolution is achieved.

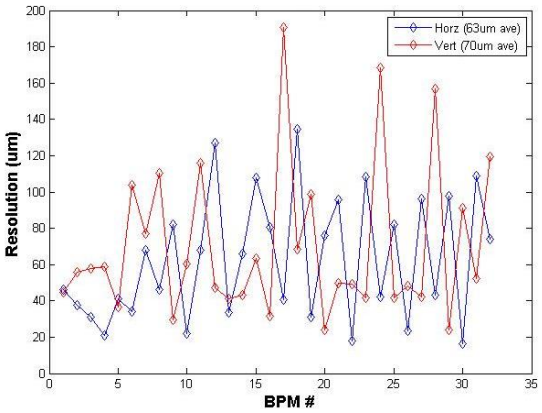

Figure 4: BPM resolution from an SVD analysis.

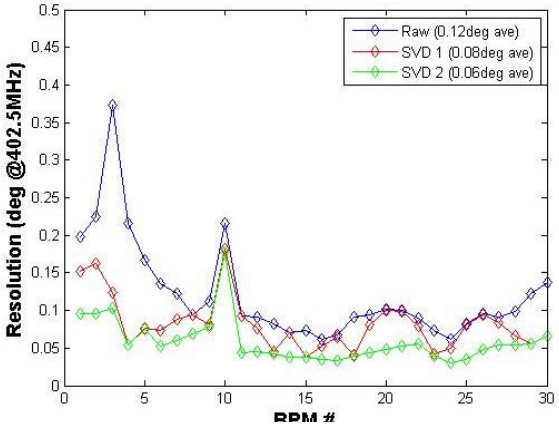

Figure 5: Phase resolution from an SVD analysis.

The phase resolution measurement is shown in Fig. 5. The three curves in the phase chart are for unmodified data (blue), and then for the first (red) and second (green) strongest correlations in the SVD removed. It is believed that most of the correlations are from beam effects, but systematic changes in the RF phase signal cannot be ruled out. The specified 0.2º resolution is achieved. (Note that these are 402.5 MHz degrees, but the resolution is for 805 MHz degrees.)

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