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Vertically Integrated Circuits at Fermilab

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Abstract– **The exploration of vertically integrated circuits, also commonly known as 3D-IC technology, for applications in radiation detection started at Fermilab in 2006. This paper examines the opportunities that vertical integration offers by looking at various 3D designs that have been completed by Fermilab. The emphasis is on opportunities that are presented by through silicon vias (TSV), wafer and circuit thinning, and finally fusion bonding techniques to replace conventional bump bonding. Early work by Fermilab has led to an international consortium for the development of 3D-IC circuits for High Energy Physics. For the first time, Fermilab has organized a 3D MPW run, to which more than 25 different designs have been submitted by the consortium.**

I. Introduction

Vertically integrated circuit technology (also referred to as 3D-IC technology) is defined as a structure composed of two or more layers of active electronic components, integrated both vertically and horizontally [1]. Methods that enable 3D-IC technology are emerging in the industry [2]. Those are: advanced and ultra high precision wafer thinning, through-silicon via (TSV) fabrication with high aspect (depth/diameter) ratio [3] [4], and oxide or metal fusion bonding. The required steps for wafer processing, which are not yet common in the microelectronics industry, include patterning of the back side of wafers, back-side metallization in order to provide connectivity between bonded layers (commonly called tiers), and establishing of bonding pads on the last tiers in the stack. The connectivity, enabling the flow of signals, biases and power supplies between different layers, is provided by a variety of technological means exhibiting different levels of advancement and complexity. Large diameter TSVs, located at the peripheral I/O pad areas, allow stacking of tiers that communicate only at the pad level. The most efficient use of 3D-IC technology is gained through the use of small diameter TSVs that vertically interconnect individual blocks located on different tiers. This shortens the interconnects, leading to the minimization of RC parasitics and the ability to integrate more transistors into the blocks while not causing a penalty in net surface area [5]. The functionality of processing units can therefore be extended. The latter is of extreme importance for a number of devices, especially for pixel detectors that target high spatial resolution. The inter-tier connectivity may extend to individual transistors, since TSVs placed on a pitch of a few micrometers are achievable in the most advanced 3D-IC processes.

The implementation of TSVs is approached in different ways by different manufacturers. TSVs may be added as the last step after wafer bonding, or may be an integral part of the foundry process. The first approach is referred to as “via last” and the second as “via first”. The stacking of tiers can be achieved by directly bonding whole wafers together (wafer-to-wafer), bonding singulated chips to host wafers (chip-to-wafer), or by bonding individual dice together (chip-to-chip). Wafer-to-wafer bonding is the most common and least expensive method, resulting from the ease of alignment. However, high fabrication yield of chips on these wafers is necessary since selection of known good dice is unachievable with this method.

Wafers are typically fused in one of two configurations, by face-to-face or face-to-back bonding. Face-to-face assembly uses bonding posts on the top metal layer, and wafers are bonded by bringing the front sides of both wafers into contact. Face-to-back bonding requires connection of bonding posts to the back side of one of the wafers, and bonding is achieved by adding the next tier in such way that front sides are facing the same direction. The requirements on the quality of the surfaces appropriate for bonding of tiers are generally satisfied with typical foundry criteria for modern planarized processes, including chemical-mechanical polishing and metal filled vias. The thinning of wafers leads to the reduction of their thickness from initially several hundreds of micrometers to thicknesses approaching 10 μm or even less. The post-thinning planes must be planar to the same degree as the top sides of bonded wafers. The surface topography requirements are stricter if bonding is based on oxide adhesion only. Topographical variations should typically not exceed a few hundreds of nanometers, and the wafer bow should typically not exceed a few tens of micrometers for successful 3D bonding [6] [7].

A. Steps at Fermilab

The exploration of 3D circuit technologies began at Fermilab in 2006. Fermilab participated in two Multi-Project-Wafer (MPW) runs (3DM2 and 3DM3) organized by MIT-LL under the DARPA Advanced Microelectronics Technology Development Program. Two versions of a prototype pixel readout chip targeting the specification of the vertex detector at the ILC were submitted. The MIT-LL 3D process stacks three 6” wafers that are fabricated in a 0.18 μm fully depleted Silicon-on-Insulator (FDSOI) process, using the via last approach [8][9][10].

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Following the experience with 3D stacking of circuits on SOI wafers, Fermilab gained access to a via first 3D process based on a commercial 0.13 μm bulk CMOS run at Chartered Semiconductor. The 3D integration is performed by Tezzaron Semiconductor using wafers with TSVs added after completion of the front-end-of-line (FEOL) part of the process [11][12].

The agreement with Tezzaron led Fermilab to the organization of an MPW run and formation of an international consortium oriented on exploration of 3D-IC technologies for applications in High Energy Physics (HEP) and related fields [13]. The reticule was divided into 12 units of 5.5×6.3 mm^2. Fermilab submitted three fully functional prototype implementations of structures for focused applications on the run that was submitted for fabrication in mid 2009.

B. Sketch of new frontiers for detectors with 3D-IC

3D-IC technologies allow an increase in the complexity of the circuitry that can be placed on a single die, by allowing larger density of transistors per unit area. This can result, for example, in significantly decreased access times for processors with cache memories in computer systems [14]. 3D-IC methods can be perceived from the nuclear instrumentation perspective as opening new possibilities in the architectures of detectors and imagers [15],[16].

Unprecedented opportunities for optimizing signal and power routing on highly segmented detectors are offered by the introduction of processing techniques such as TSVs embedded in the fabrication stage of the wafers, wafer thinning (leading to exposing of buried TSVs), and wafer bonding with vertical electrical connections. Typical 2D detector readout chips require peripheral pads on at least one side of the die. These pads occupy a few hundred micrometers of the chip periphery [17][18]. The mechanical mounting of the detectors in the imaging frame is thereby complicated since dead area is required by the pads and for wire bonding clearance. By applying 3D-IC methods, the dead area can be virtually eliminated, since all connections can be routed to the back-side of the stacked device and redistributed over the available surface. On the front side, instead of the typical bump bonding, a detector can be connected to the readout chip by means of one of the 3D-IC bonding techniques that can be called fusion bonding techniques to distinguish them from classical bump-bonding. This yields a structure that is indistinguishable from monolithic configurations. One of the available bonding processes is oxide-to-oxide direct bonding, called Direct Bond Interconnect (DBI®). The process was developed by Ziptronix [19][20]. Fermilab has gained first experience with DBI® working on the mating pixel detectors to the Fermi-Pixel (FPIX) chips [16][21].

3D-IC technology is an efficient tool in providing separation of low-noise analog circuitry from digital blocks. This task is crucial in detector readout systems. Typically, it can be difficult to minimize cross-talk, substrate currents, and capacitive coupling in a 2-dimensional chip. By using 3D stacking, the analog and digital functions can be allocated to separate tiers. Lines carrying active digital signals can be moved to tiers that are shielded and farthest away from the detector.

This paper discusses these new opportunities using the designs submitted by Fermilab as examples to illustrate the developed claims. Section II reviews the guidelines of the 3D-IC processes used by Fermilab. The details of the designed circuits are presented in Section III along with related perspectives and goals.

II. 3D-IC PROCESSES USED BY FERMILAB

The fabrication of the first 3D chip for HEP, called Vertically Integrated Pixel (VIP1) and designed at Fermilab, was realized in the 3D-IC MIT-LL process using a via last approach [22]. The VIP1 chip is a demonstrator serving as proof of the 3D-IC principle for HEP. The implemented functionality targeted the vertex detector at the International Linear Collider (ILC) [23]. The stacked wafers were manufactured in an SOI process, featuring a 400 nm-thick buried oxide (BOX) layer. The stacking processing consists of a few steps that are performed in sequence for each tier added. A simplified list of steps can be presented as follows: oxide-to-oxide bonding of planarized surfaces, thinning to the BOX level of the added tier, etching cavities for TSVs at the designated locations, filling the cavities with tungsten, and preparation of the surface for adding a new tier. The presence of BOX is used as a naturally available etch-stop in the wafer thinning process. Ubiquitous oxides lead to a significant simplification of the 3D stacking process by naturally isolating the inserted TSVs. The TSVs make contact to the routing metals by means of specially designed landing posts that also serve as etch stops in creation of the cavities for the TSVs. The fabrication of a 3D-IC chip using the via last method and CMOS SOI type wafers is shown in Fig. 1. It can be noticed that the first two wafers are bonded face-to-face, and the topmost wafer is added using back-to-face bonding. Each tier has 3 metal routing layers and the two top tiers have additional back metal layers deposited on the BOX after thinning. These back metals are used in establishing connectivity between tiers and are also available for additional signal routing. The total thickness of the structure after completion of the 3D assembly is about 700 μm. The majority of this is due to the handle wafer, while the thickness of the 3 active tiers is only about 22 μm.

The actual area required for each TSV is about 5×5 μm^2, which includes the required clearance from neighboring circuitry. A TSV can be a buried via, providing connectivity only between internal tiers, or can be a fully stacked pillow, allowing direct connectivity from the top tier to the bottom one.

The tests of the VIP1 chip showed correct functional operation of the structure. However, the fabrication yield was very poor and it was concluded that FDSOI processes are not optimal for mixed-mode circuitry that includes high precision and low noise parts. The performance of the analog circuitry was strongly compromised by a number of factors, like temperature variation in the structure due to oxides impeding heat flow, the presence of inter-tier cross-talk paths that may be dominant over interference between components on the

same tier, varying carrier mobility due to the straining of transistors on the BOX, variation of transistor threshold voltages due to flow of ions eased through oxides, etc. [24][25][26][27].

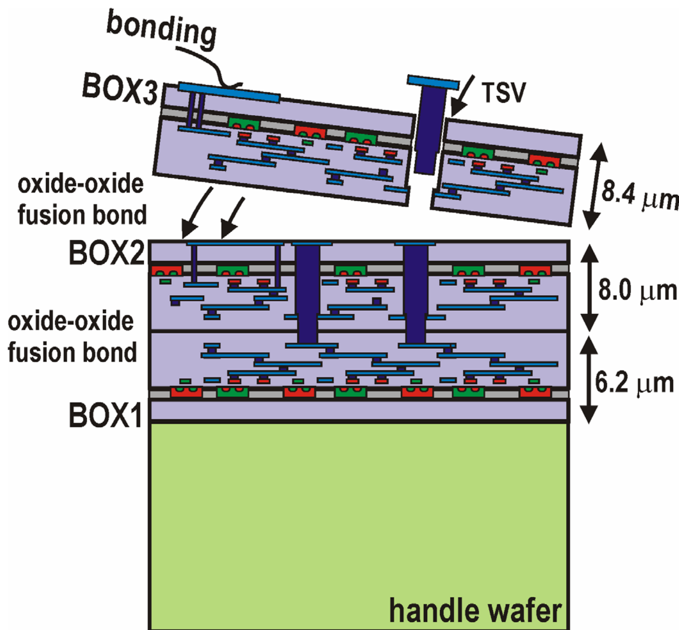

Fig. 1. Conceptual representation of the fabrication of a 3D-IC chip using the via last method and circuits manufactured on CMOS SOI type wafers.

The immediate successor to the VIP1 prototype is called VIP2a, and was submitted in 2008 to the subsequent MIT-LL 3D run (3DM3) in the FDSOI process. In order to increase yield and improve circuit operation, some self-imposed layout guidelines were adopted and used in the design of the VIP2a chip. The power and ground routings were strengthened by linking them in an extensive mesh with connections between tiers in each pixel. The MIT-LL-given rules for trace routing were scaled by a factor equal to 1.2, resulting in wider paths and larger clearances. Regarding the rules for transistor sizes, the process was virtually down-graded to a 0.5 μm feature size in order to decrease off-state leakages and to average structural effects. The delivery of the VIP2a chip is expected in 2010.

More recent design work at Fermilab has focused on a 3D-IC process using bulk CMOS 0.13 μm wafers with a Cu-Cu thermo-compression bond interface. The wafers are fabricated by Chartered Semiconductor and the subsequent 3D processing and stacking is done by Tezzaron. The processing of the CMOS wafers at Chartered is a standard CMOS flow supplemented by insertion of TSVs after completion of FEOL. The reactive ion etching (RIE) technique, used in the first place for installment of shallow trench isolations (STI), is applied for incising cavities for TSVs that are filled with tungsten afterwards. A sketch of a 3D-IC chip made using the Tezzaron via first method is shown in Fig. 2. The TSVs can be inserted either in one wafer only, as indicated in Fig. 2a, or in both wafers as shown in Fig. 2b. Addressed later in this paper, the use of TSVs in both wafers plays a crucial role in allowing a detector to be bonded to a readout chip on one side while bringing all control signals, power supplies, etc., to the opposite side of the structure. In order to make possible bringing together and fusing two wafers together with electrical connections between tiers, a so called bonding interface must be provided on both wafers. The bonding interface is composed of uncovered metal bond-points and is a pert of the IC design. The bond-points are small 2 μm hexagons instantiated on a continuous hexagonal grid at a pitch equal to 4 μm. The bond-points are on the last (top) metal layer. Some of bond points are present only for providing mechanical strength of the connection; some other may carry signals between tiers. The view of the bonding interface is highlighted in Fig. 2a. The first operation realized by Tezzaron is face-to-face bonding of wafers delivered from Chartered. The second operation is thinning of one side of the obtained 3D stack. The substrate material is removed until exposing bottom ends of TSVs that were buried until this processing step. Aluminum bonding pads are patterned at the last step, providing connectivity down to the chip using TSV. The sketch in Fig. 2b shows that the 'top tier' wafer remains thick and the 'bottom tier' wafer is thinned down to expose the tips of TSVs after bonding. This structure is delivered from Tezzaron. It is worth mentioning that the top tier can in principle be thinned down too. The whole structure may require interim attachment to a handle wafer to achieve this thinning goal. Although as many as five stacked tiers have been demonstrated by Tezzaron, the current Fermilab designs only use two layers and the face-to-face stacking method.

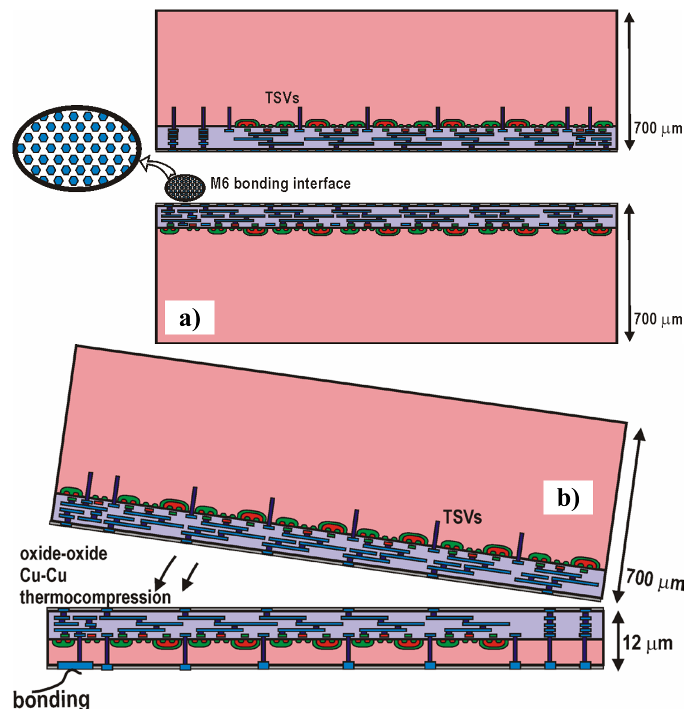

Fig. 2. Conceptual representation of the fabrication of a 3D-IC chip using the via first method and circuits manufactured on CMOS bulk type wafers, bonding interface a), bonding, thinning and I/O pads b).

The characteristics of the Chartered CMOS process used are: large reticule (about 26×31 mm^2), single poly layer, 6 Cu metal layers, redistribution metal layer for pads, deep nwell, single mask Metal-Insulator-Metal capacitors, low power 1.5V

transistors (standard threshold voltage or SVT), low threshold voltage transistors (LVT), zero threshold voltage transistors (ZVT), 3.3V I/O transistors, and high resistivity poly resistors. TSVs are intrinsic to the wafer processing, and are 1.3 µm in diameter and 6 µm deep, with 3.8 µm minimum spacing.

The costs of the Chartered run were limited by using only one set of masks. The reticule was divided symmetrically into two halves, so that the reticule hosts top-tier chips and bottom-tier chips on its left and right side, respectively. The vertical symmetry about the center of the reticule guarantees alignment of circuits for 3D assembly performed by flipping one wafer over on top of another. The view of the whole fabricated reticule is shown in Fig. 3. The Fermilab sub-reticules are H-H*, I-I* and J-J*, where the H-H* sub-reticule is occupied by the VICTR chip (Vertically Integrated CMS Tracker Readout), the I-I* sub-reticule is occupied by the VIP2b chip (Vertically Integrated Pixel Version 2b), and the J-J* sub-reticule is occupied by the VIPIC chip (Vertically Integrated Photon Imaging Chip).

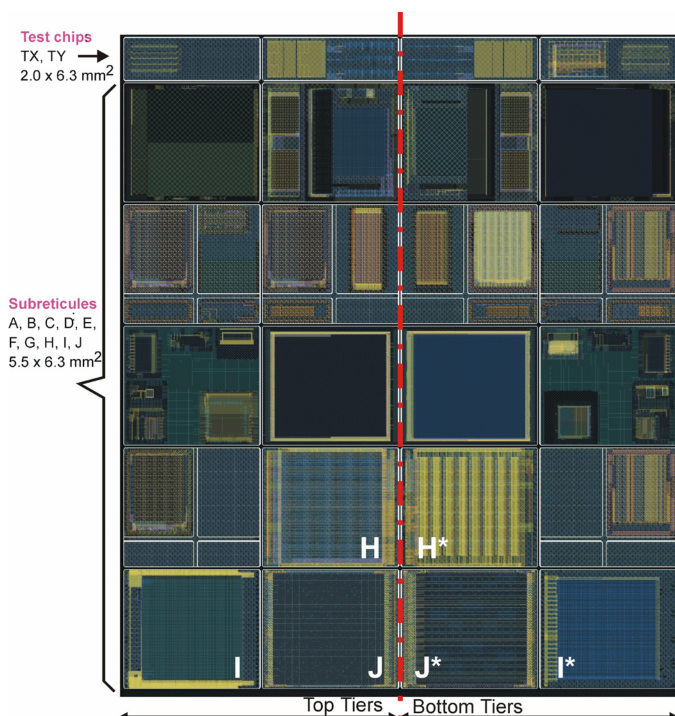

Fig. 3. View of the whole frame with Fermilab chips (H-H*, I-I*, J-J*).

Simple planar silicon detectors are under preparation for use with the 3D-chips submitted on the Tezzaron run. The detectors are in fabrication at the Instrumentation Division at Brookhaven National Laboratory (BNL). The designs follow the rules for the DBI® wafer bonding process. The DBI® process begins with very small metal contacts imbedded in a smooth oxide surface. The wafer bond is achieved immediately after the two oxide surfaces are brought together. After the desired strength of the oxide bond is established, the heating is applied to expand the metal contacts to fuse compression bonds. Sub 10 µm bonding pitches are achievable, while the upper limit on the bonding metal density is around 10%. The DBI® process is not limited to wafer-to-wafer type bonding. Indeed, the assembly of the chips from the Tezzaron run to the detector will be done on a chip-to-wafer basis.

III. 3D-IC Designs by Fermilab

A. VIP2b

The VIP2b is a time stamping pixel readout chip for the vertex detector at the ILC. The chip is a new version of the earlier VIP1/VIP2a 3-tier MIT-LL device, redesigned using the Chartered/Tezzaron 2-tier process. The new circuit has an array of 192×192 square pixels laid out with a pitch of 24 µm^2. It has an 8-bit digital time stamp, allowing time bins equal to Δt=3.9 µs in the ILC time operation regime with readout between ILC bunch trains. The chip implements sparsification based on the token passing scheme that remains unchanged from the earlier prototypes. The front-end is a single stage integrating charge signal amplifier with discriminator, along with two sample/hold (S/H) cells for correlated double sampling (CDS) and analog readout. The front-end implements a polarity switch allowing collection of e^- or h^+. Each pixel features a separate test input allowing injection of test charges through a series capacitor. The addresses of hit pixels are output on a serial bus, along with the correlated samples available on the analog outputs.

The detector for the VIP2b chip has diode implants on a 24 µm pitch. The conceptual view of the mounting of a single VIP2b chip onto a detector is shown in Fig. 4. The detector wafers, fabricated at BNL, contain sensors for all Fermilab 3D-IC chips. The whole sensor wafers undergo necessary processing finished up with metal bonding posts. Similar processing is performed on the wafers with readout chips. The chips with prepared bonding posts are diced from the 3D wafer. The individual chips are mounted on the corresponding sensors. The alignment targets, which are integrated on both bonded components, can be seen in infra-red light through the whole structure and allow precise alignment. All pads for power supplies, biases, and analog and digital I/Os are routed to the pad-ring around the matrix of pixels on the VIP2b chip. The DBI® bonding includes transferring of the VIP2b pads onto the sensor. New pads are recreated on the sensor where the access is not obscured by the VIP2b chip and the pads are reachable with a wedge or ball bonding head. There is a fan-out connection routed on the sensor. The traces are shielded from the sensor by a metal plane. The solid plane extends under the traces between the bonding positions and the pads on the sensor and fills an empty space between the diode implants. The VIP2b chip and its assembly with the detector qualifies as the most moderate challenge in the transition from conventional detector architectures to those that might be allowed by exploiting 3D-IC technologies.

B. VICTR

The next 3D chip, VICTR, embodies an initial step toward developing an intelligent tracker capable of participating in the production of a Level 1 trigger at the upgrade of the CMS experiment at SLHC. It is expected that the tracker will be able to identify hits associated with transversal momentum

p_t>2 GeV for data transfer off the tracker, and to participate in building tracks and identification of those with p_t>15-25 GeV. The need for momentum cut automatically asks for high spatial resolution in the rϕ plane. However, the tracker should also provide about 1 mm resolution in the 'z' coordinate to identify primary vertices [28].

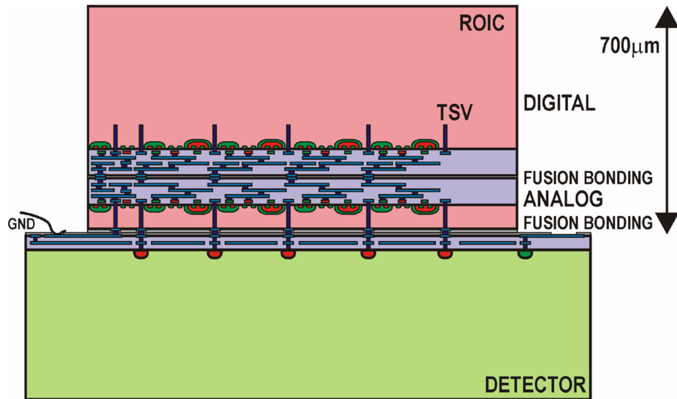

Fig. 4. Assembly of the VIP2b chip on the dedicated detector with the fan-out connection and pads for wire bonding on the detector.

The p_t cut of the desired threshold can be achieved by processing hit coincidences from two layers of strips sensors. Provided the pitch of strips is tight enough and the layers are separated by enough distance, track curvature in a magnetic field can be detected by observing offsets of hit positions from the two layers.

80 μm, and its active part is 5 mm long. The bottom sensor is a matrix of 64×5 short "z strips" of 80 μm×1 mm. The VICTR chip is designed in such way that charge signals are transferred to the VICTR chip from two directions normal to the surface, i.e. from both the bottom and the top sensor. The spacing between the sensors, required for the momentum resolution, is achieved by insertion of a 1 mm thick interposer between the top sensor and the VICTR chip. The candidate material for the interposer is silicon, and charge signals are transferred through deep TSVs to the VICTR chip. Studies of the interposer are underway. The top tier of the VICTR chip looks at the ϕ strips, while the bottom tier looks at the z strips. The coincidences are detected between each strip on the ϕ layer and each group of 5 short strips on the z layer. The processing electronics uses the FEI4 front-end design for the pixel detectors at the ATLAS experiment at LHC [29]. The design was graciously shared with Fermilab by the ATLAS pixel community.

The segmentation of the z layer provides the necessary spatial resolution but it is not used in the processing of coincidences. The VICTR chip processes signals with the typical LHC cadence of 25 ns. It provides serial readout of all top and bottom strips along with coincidence information. In the final circuit, the simple coincidence circuit that is currently based on the AND logic between reciprocal channels will need an upgrade. Processing will need to include the spread of signals onto the neighboring strips for improved spatial resolution. Physics simulations are needed to establish architecture of the circuit.

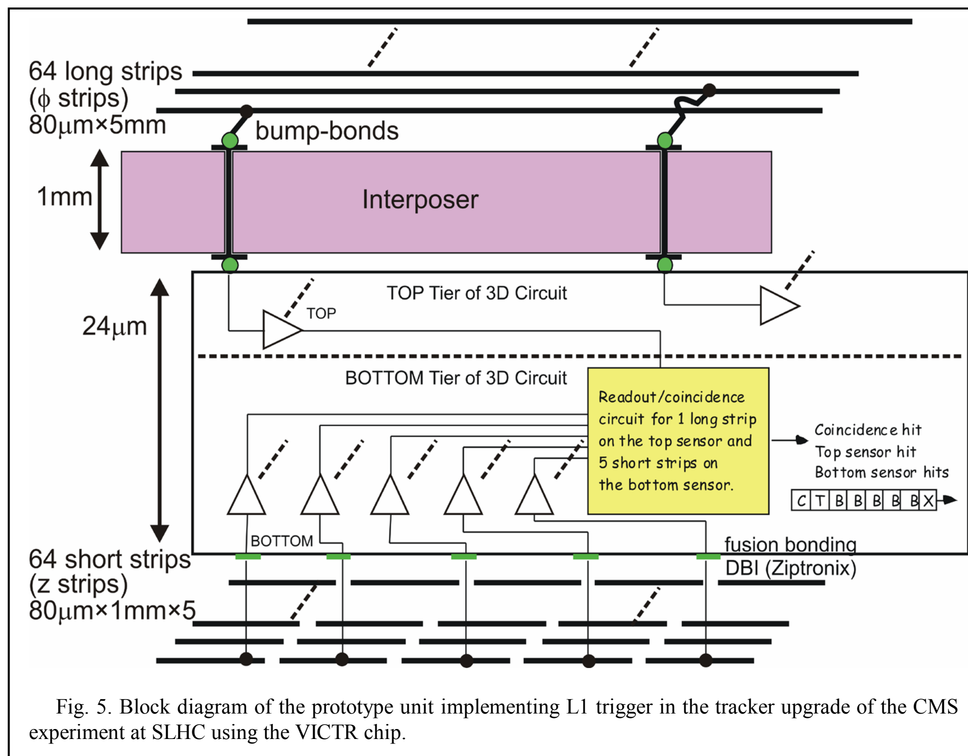

Fig. 5. Block diagram of the prototype unit implementing L1 trigger in the tracker upgrade of the CMS experiment at SLHC using the VICTR chip.

The prototype system for the intelligent tracker is sketched in Fig. 5. The sensors for the VICTR chip are also being fabricated in the BNL sensor run. There are two sensors used in the prototype since different strip arrangements are required. The top sensor has 64 "ϕ strips" laid out on a pitch of

The construction of the prototype unit for the implementation of the L1 trigger in the tracker upgrade of the CMS experiment at SLHC extends significantly exploitation of the 3D-IC methods compared to the VIP2b chip. The VICTR chip must be thinned to about 24 μm so that the connections

on the top and bottom of the chip can be used. Typically, silicon wafers cannot be handled if so aggressively thinned. Thus, a handle wafer must be used in the fabrication of the final structure of the trigger module. The process starts with deposition of back metal, forming a base for the future bump bonding pads on the top tier that is thinned by Tezzaron at the very first step. Then, a dummy handle wafer is bonded to the 3D wafer at the top tier. The seeds of bump-bonding pads are buried. The bond to the handle wafer is strong enough for the shearing forces to allow thinning of the opposite side of the wafer to expose the TSVs that will contact the bottom sensor. The preparation of the bottom bonding posts for fusion bonding is performed on the exposed thinned surface and the 3D chips are then diced. Next, diced VICTR chips are mounted to the bottom sensor wafer. After accomplishing of the last step, the handle wafer is removed and the mechanical stability of the structure is provided by the bottom sensors. Then the bottom sensor wafer with mounted VICTR chips is diced. These assemblies are then ready for mounting to the top sensor via an interposer.

C. VIPIC

The last 3D chip, VIPIC, was designed for X-ray photon correlation spectroscopy (XPCS) experiments on light sources. XPCS is a technique that is used for studying the dynamics in various processes on nanometer scale lengths [30]. In these analyses, so called speckle patterns are generated. The photons are registered at different spatial positions with their arrival times. The results of the analysis are time correlation functions that are calculated for different sampling time intervals at different positions. The detector must allow time resolved data acquisition. The targeted readout is continuous, registering all data from the observed process. The time resolution set for the design was $\Delta t=10\ \mu s$.

The VIPIC chip is a prototype matrix of 64×64 pixels. The pixel size is $80\times80\ \mu m^2$. The chip has two modes of operation, i.e. readout with data sparsification and an imaging mode, where accumulated events are read from all pixels without addresses. The data sparsification is the primary readout mode for the VIPIC chip and works well at low levels of pixel occupancy. Continuous sending of hits to the data acquisition system with a minimum delay after their arrivals guarantees good timing precision. Each pixel is able to count individual radiation events in both modes; however the imaging mode leads to reading out all pixels without sending out their addresses to the data acquisition system. The VIPIC chip functions dead-timelessly in both modes of operation.

The main components of each pixel are: a charge sensitive amplifier followed by a 2-stage shaping filter and a single threshold level discriminator, two DACs for tuning the decay time constant of the amplifier response and the threshold of the discriminator, test charge injection circuitry, hit holder circuitry, and two alternately used 5-bit long event counters. The analog part of the pixel was designed in collaboration with UST-AGH, Krakow, Poland. The hit holder is a central part of the hit acquisition system. It acquires new hits. The hit holder operates as a two-cell pipeline. The toggling between phases of the pipe-line occurs with rising edges of the main time stamping clock. The first cell of the pipeline fires with a first hit arriving in a new time cycle. Then, the hit information is handed off from the first cell to the cell connected to the readout with each rising edge of the time stamping clock. The hit is fed to the sparsification circuitry. The sparsification circuitry, in turn, outputs hits from the matrix according to the built-in order. The sparsification circuitry sends generated binary addresses of hit pixels to the serializer connected to the LVDS driver. The time bins are defined by the time stamping clock. The period of the clock must be selected aiming at readout of all data within it each cycle as a function of the desired timing precision but is constrained by the occupancy. The hit holder provides flexibility in managing acquisition of hits. It can be permanently set to ignore any hits or to always contain the hit. It operates as a pipe-line.

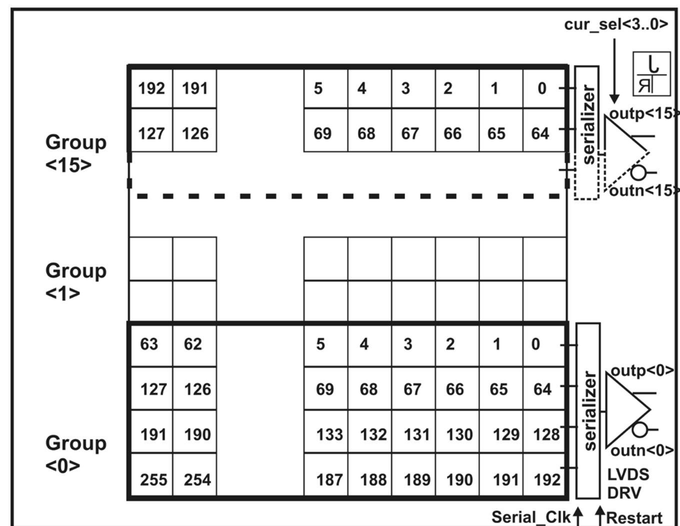

Fig. 6. Block diagram of the VIPIC chip.

The chip is divided into 16 groups of 256 pixels, which are read out in parallel through separate serial ports running on the LVDS standard. The data sparsification process is performed simultaneously in each group. The block diagram of the VIPIC chip showing subdivision into the readout groups is presented in Fig. 6. The sparsification circuitry is common for each group of 256 pixels, and is a modified version of an old idea proposed for the MEPHISTO prototype [31]. It is primarily a multi-input logic OR gate integrated with priority encoder. The encoder selects pixels for readout and generates addresses of hit pixels automatically in binary code. The layout of the sparsification circuit is distributed into all pixels.

The readout of the VIPIC chip is binary. Each hit is represented by a 16 bit-long word, where 3 bits are the start sign, 5 consecutive bits are the content of the in-pixel counter and the remaining 8 bits are the pixel address in the sparsification mode. The pixel addresses are not required in the imaging mode, thus the output word is shorter. One group of 256 pixels can send out a maximum of 60 hits within a $10\ \mu s$ time period. This estimate assumes a moderate frequency of 100 MHz for the serial clock and occupation of separate pixels by 60 hits, i.e. each pixel is hit only once.

The imaging mode allows the rate of 50×10^3 frame/s. The

5-bit counter length guarantees dead-timeless and lossless operation in the imaging mode. This confidence stems from the fact that the time required to send out all data from all pixels in the group is shorter than the time to fill the working counter by new hits with the serializer operating at 100 MHz. The maximum speed at which counting can occur is limited by the time at which the front-end returns to the baseline; otherwise signal pile-up would be present.

The VIPIC main features are summarized in Table I.

TABLE I. MAIN FEATURES OF THE VIPIC CHIP

Feature	Comments
X-ray detection (8 keV) with Si pixel detector	XPCS application
64×64 pixels, pixel area: 80×80 μm^2	5120×5120 μm^2
separate analog and digital tiers	
analog=280 transistors, digital=1400 transistors	
chip area 6.3×5.5 mm^2 (6.3×5.6 mm^2)	larger dicing for DBI®
single threshold for discriminator,	
trim DAC/pixel for offset corrections	3 bits CSA feedback, 7 bits discriminator threshold
permanent set and permanent disable bit per pixel	
test charge injection circuitry	C_{inj}=1.7 fF
single ended or differential configuration of the front-end	
power consumption 25 µW/analog pixel	
CSA: noise ENC < 150 e^-, τ_p < 250 ns, gain 115 mV / 8 keV,	C_{feed}=8fF
readout modes:	
- sparsified, binary readout (sparsified time slicing mode),	
- imaging binary readout mode (5 bit signal depth)	
dead-timeless and trigger-less operation in both readout modes	
sparsification: priority encoder based sparsification circuitry	
16 parallel serial LVDS output lines (16 groups of 4×64 pixels)	
two 5 bit counters per pixel for recording multiple hits per time slice (useable in the imaging mode)	
frame readout at 100 MHz serial readout clock	
- 160 ns / hit pixel in sparsified time slicing mode (up to 60 hit pixels / 10 µs)	
- 50×10^3 frame/s in imaging mode (5 bit counting)	

Of all the Fermilab chip designs, the VIPIC uses the capacities of the 3D-IC technology in the most complete way. Firstly, full separation of analog and digital circuits is achieved. The dividing line runs along the interface between tiers. The analog part of the pixel is connected to the digital part by 27 signal connections passing through the bonding interface. Additional connections, consisting of multiple bond-points, are used to transfer power supplies and grounds. The 27 signal connections include ten pairs of complementary inputs of DACs that are routed from the shadow latches of the configuration shift registers implemented on the digital level, one complementary global strobe signal for injection of test charges into the selected pixel, one complementary signal for selecting the pixel for charge injection, and one complementary signal for toggling between the single-ended and differential administration of the reference level in the shaping filter. The remaining signal is the output of the discriminator feeding the hit holder circuitry located on the digital layer. Secondly, the layout is done in such a way as to make all pins of the chip available on both sides of the die. This provides an opportunity for comparative testing between a classical "2D" configuration and the more recently possible "3D" configuration.

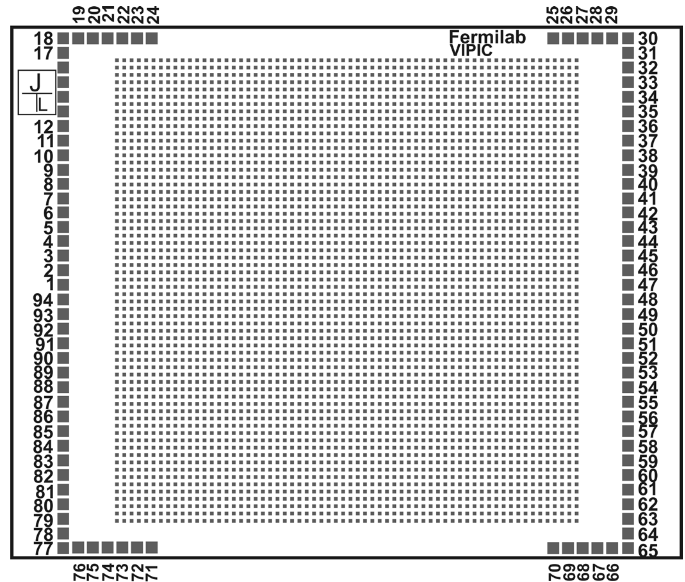

Fig. 7. Front-side view of the chip with bonding posts to the diodes and the signal fan-out routed on the detector.

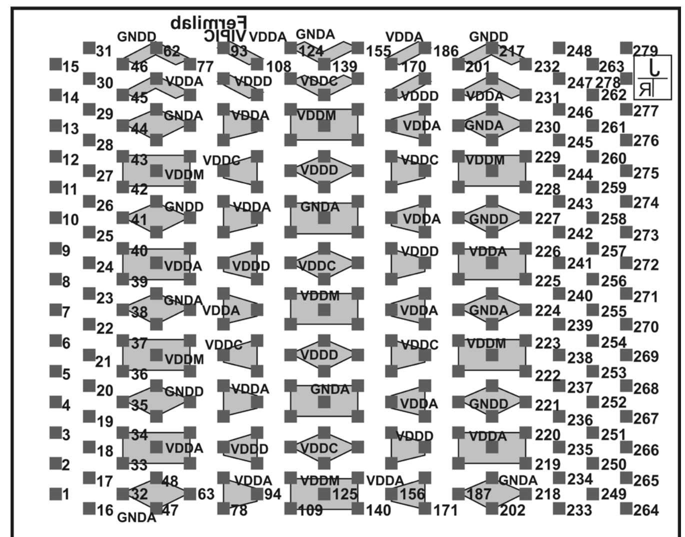

Fig. 8. Back-side view of the chip with bump-bonding pads distributed over the whole surface of the chip; the polygon shadowed shapes mark pins holding the same potential and the same use.

In a 2D configuration, both the control pads (including power supply) and the detector diode inputs are on the same side, which inevitably introduces a significant and undesirable dead area. With a 3D configuration, all control and power supply pads can be moved to the back side of the chip, leaving only the sensor connections on the front side. This potentially eliminates the dead area and enables a 4-side buttable structure. It is planned to test mounting of the VIPIC chip to the detector in a manner similar to that discussed for the VIP2b chip. The front-side view of the VIPIC is in Fig. 7, showing bonding posts designed to connect the pixel front-

ends to the detector diodes and the 2D control signal fan-out traces routed on the detector. The corresponding view of the back-side pins is shown in Fig. 8. In pursuit of the lowest impedance, a better distribution of the power supplies and grounds is achieved by multiple, intertwined connection points spread over the whole area of the matrix of pixels. The distance between these chip connection pins on the back side is 450 μm. Low density pitch bump bonding, like Sn bump bonding or gold stud bonding, is proposed for mounting of the VIPIC chip on the dedicated host board. The embedding of TSVs in a single layer detector readout integrated circuit, or more generally on both sides of the multi-layer structure, provides the feasibility of a full 4-side buttable pixel detector tile. The cross-section of the targeted detector architecture is shown in Fig. 9. The chip designs carried out at Fermilab should gradually lead to the achievement of this objective. The VIPIC chip, being the most advanced prototype, is actually a demonstration of the possibility of achieving this new technological dimension.

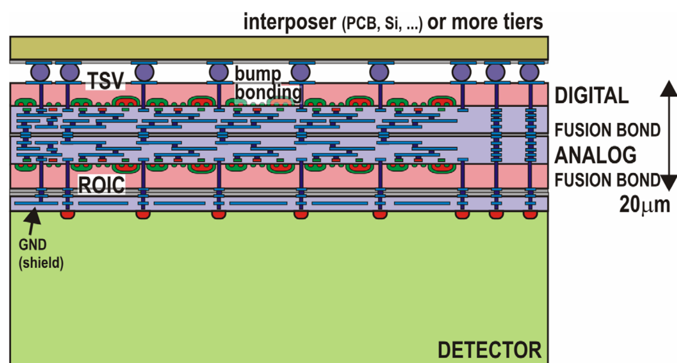

Fig. 9. Cross-section of a 4-side buttable pixel detector tile.

The detector can be fabricated as a homogeneous array of diodes using the whole area available on a wafer. Individual readout chips can be tiled on the detector wafer by fusion bonding. The low density pitch connectivity on the back of the chips can be connected to the host substrate. The system can be built on an alumina or silicon interposer board, a classical printed circuit board, etc.

D. *Sensors and DBI® bonding*

The chips submitted to the Tezzaron/Chartered run require radiation sensors with characteristics that make them able to use the direct bonding technology. The fabrication of the dedicated sensors is underway at BNL. The sensors are p-on-n. The thickness and the resistivity of the wafer are 500 μm and 4 kΩcm, respectively. The pitch of the pixel devices is 24 μm and 80 μm for the VIP2 and VIPIC chip, respectively. The sensors for the VICTR chip are short strips laid out with a pitch of 80 μm. The cross-section of a single direct bonding node of a 3D readout chip fabricated on the Tezzaron/Chartered 3D-IC run bonded to a detector is shown in Fig. 10. The bonding process is Ziptronix's DBI® technology. The detector processing lacks of features, like metal filled vias and planarization. In order to be able to make up, the thicknesses of the deposited layer must have been chosen carefully in order to provide surface topography sufficiently flat for the DBI® process. The thickness of oxide I is 2000 Å, the thickness of sensor metal is 2000 Å and the thickness of oxide II is 2000 Å on the detector. The seed metal, DBI® post and DBI® oxide are deposited in the processing by Ziptronix. The size (diameter) of the DBI® post is 6 μm.

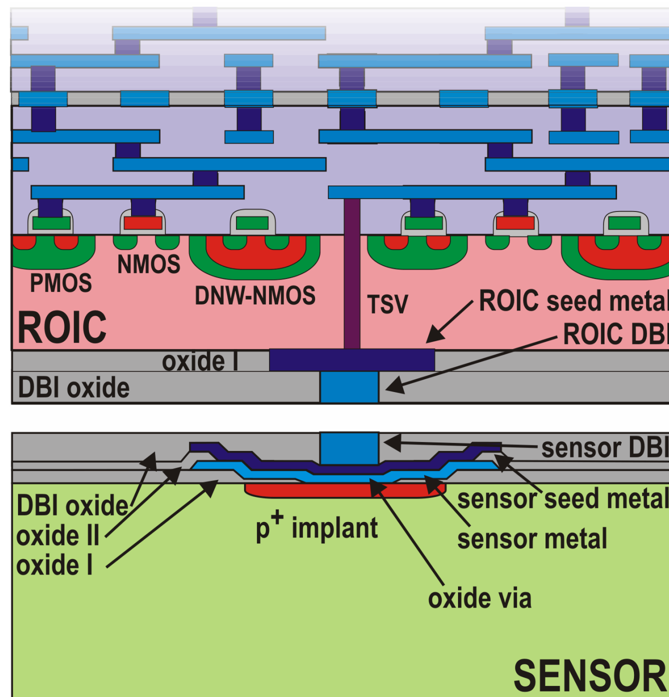

Fig. 10. Cross section of a single direct bonding node of a 3D readout chip a detector using the Ziptronix's DBI® technology.

IV. Conclusions

Fermilab has made the first steps in introducing 3D-IC technology to the applications of particle tracking and imaging of ionizing radiation in HEP and related domains. Fermilab has had an opportunity to explore freshly emerging technologies, e.g. the via last 0.18 μm FDSOI CMOS process available at MIT-LL, the via first 0.13 μm bulk CMOS process available at Tezzaron/Chartered, and the DBI® bonding process available at Ziptronix. The early Fermilab experience was translated into an International Consortium of institutions that have come together to develop 3D integrated circuits for physics applications. The access to diverse technological approaches through the very early stages of the work provides valuable knowledge on the usefulness of those approaches in achieving reliable designs. Some methods linked to the 3D-IC technology can be identified as useful to detector engineering even when tested and used without vertical stacking of wafers. As the best example, TSVs can be used for bringing pads on the opposite side of the readout chip to provide better power distribution and to facilitate bonding of readout circuits to detectors. Reliable thinning techniques may be used for reduction of total material budget and to produce detectors with thin entrance windows and uniform thicknesses of active volumes. It can be summarized that 3D-IC offers new approaches to old problems in detector development.

The five chips designed by Fermilab target a wide spectrum of applications; four of those chips are still in the process of being fabricated. The first results are expected very soon. This paper reviews some of the opportunities that are presented by 3D-IC methods. Designs of chips done at Fermilab are employed as an illustration of the gradual progress, and to explore the potential residing in the new tools. The feasibility of a 4-side buttable device, obtained by moving and distributing all connections to the side of the structure opposite the side bonded to the detector, has been demonstrated on the actual designs.

One may venture to say that another advantage of the 3D-IC technology is to slow down the pace at which designs of readout chips for radiation detectors need to utilize nano-scale processes, where challenges for example related to matching of active components must be faced [32]. It is known that a higher density of electronic circuitry per unit area is needed to provide the functionalities requested in modern systems, but nano-scale processes exhibit extreme challenges in low-noise and precise analog design.

Subject to further consideration is the possibility of using of heterogeneous wafers, i.e. wafers from different foundries or from different process families. This approach may lead to the optimization of each tier in the 3D stack for a specific function, e.g., a detector tier, an analog processing tier, a digital communication tier, etc. [33]. The mixing of heterogeneous wafers because of technological or economical reasons may be impractical directly at the foundry. The bonding of heterogeneous wafers can however can be achieved by using methods as DBI®, offered by Ziptronix, or similar approaches available elsewhere. An example of this type of wafer stacking is the attachment of detectors to readout chips as presented in this paper.

The paper is not attempting discussing of heat dissipation issues in the presented circuits. The mixed-mode nature of the discussed circuits is characterized by relatively low density of electronics, thus no heat dissipation problems are expected. On the other hand, for ultra fast digital circuits, for example involving multi-core processor units with piggy-backed multi-layers of memories, the industry is foreseeing facing the efficient evacuation of dissipated heat may be a serious issue. New methods of cooling are under investigations. An example of a study for cooling of future 3D chips is to circulate some fluids through a mesh of micro-channels that can be etched in as a part of the wafer processing [34].

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