

# The Cold Dark Matter Search Test Stand Warm Electronics Card

Bruce Hines<sup>1</sup>, Sten Hansen<sup>2</sup>, Martin Huber<sup>1</sup>, Terry Kiper<sup>2</sup>, Wolfgang Rau<sup>3</sup>, Tarek. Saab<sup>4</sup>, Dennis Seitz<sup>5</sup>, Kyle Sundqvist<sup>5</sup>, Vuk Mandic<sup>6</sup>

**A card which does the signal processing for four SQUID amplifiers and two charge sensitive channels is described. The card performs the same functions as is presently done with two custom 9U x 280mm Eurocard modules, a commercial multi-channel VME digitizer, a PCI to GPIB interface, a PCI to VME interface and a custom built linear power supply. By integrating these functions onto a single card and using the power over Ethernet standard, the infrastructure requirements for instrumenting a Cold Dark Matter Search (CDMS) detector test stand are significantly reduced.**

## I. INTRODUCTION

The CDMS[1] experiment uses germanium detectors operating at 40mK to detect interactions from putative WIMP particles. The combination of ionization and phonon readout on a single detector is used to achieve a large background rejection factor. The phonon portion of the detector uses an array of transition edge sensors (TES) operating at 40mK attached to SQUID preamplifiers operating at 600mK. The ionization readout uses a JFET input charge amplifier with the FET operating at 150K.

The room temperature portion of the phonon channels includes the biasing for the TESs and the SQUIDs, the flux lock loops for the SQUID amplifiers and all the components of the charge amplifiers excluding the feedback resistor which is cooled to 50 mK and the JFET input device. Fourteen bit 1.25 Msps ADCs digitize the phonon signals and 16 bit 2.5Msps ADCs digitize the charge signals. The ADC data is continuously streamed to a 64Mbyte memory configured as a circular buffer. With a total ADC data rate of 20Mbytes/sec, the buffer can store about three seconds of data. Triggers are derived from the digitized data. A trigger packet which includes the trigger type and the address region within the buffer where the event data is located is sent to the host over Ethernet. If the host decides the event is of sufficient interest, the relevant portion of the buffer memory is read out.

A key feature of the design is the use of a low-noise DC-DC converter, which provides multiple isolated outputs from a single 48V input. The expectation is that a card of similar design tailored to a new generation of detectors will be used

for the next generation CDMS installation planned for SNOLAB in Sudbury, Ontario.

## II. MOTIVATION

CDMS experiment currently uses readout electronics designed and built several years ago. The collaboration decided that it was both impractical and prohibitively expensive to add incrementally to the existing electronics. Advances in the components available enable the design and construction of simpler, cheaper and easier to use hardware.

The existing system uses a standard architecture of modules plugged into crates powered by external linear power supplies. The signal chain consists of an analog front end card, a filter and discriminator card for generating trigger pulses and a trigger logic card which takes discriminator outputs from the filter cards and signals from the PMT veto system to form a trigger. The analog outputs of the filter card are sent to a VME crate containing commercial digitizer cards. There are various interfaces for communication between a host computer and these crates. A set of linear supplies for generating the voltages used by the analog cards is housed in a separate chassis and cabled to the custom crates. For a single large installation this is reasonable, but for a test facility that has at most a few detectors, the overhead of setting up a complete signal chain becomes burdensome. Over the last three years, three rounds of prototypes have been built, the third of which will be produced in sufficient numbers to outfit test facilities in the US and Canada.

## III. DESIGN

The replacement electronics performs all the necessary functions on a single card called digital control and readout (DCRC). Forty-eight volts from a power over Ethernet connection (POE) is converted to analog  $\pm 5.5V$  and digital 5.5V by means of an isolated half bridge forward resonant DC-DC converter. The trigger and filter functions are performed on digitized data. A large buffer can store data for a time sufficient to send a trigger message to the host and a request for the relevant data to be issued from the host. The function of the trigger logic card is replaced by software running on the host. In addition to replicating the functions of the existing electronics, on-card diagnostic features were added to reduce the ancillary test equipment required by the facility.

The principal reason for distributing power in the manner described is to separate the signal and power grounds[1]. The present installation at the Soudan mine in Minnesota achieves reasonably low noise, at the cost of days or in some instances, weeks of work in tracking down new noise sources whenever

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1. University of Colorado at Denver.
2. Fermi National Laboratory, Batavia Illinois
3. Queens University, Kingston Ontario
4. University of Florida, Gainesville
5. University of California, Berkeley
6. University of Minnesota, Minneapolis

a change has been made to the system. By using local, isolated converters, one can separate to a degree the input signal grounds from the external environment. Obviously, the converter must achieve very low noise and ripple for this scheme to work. POE has the desirable feature that when a powered device is disconnected, the drop in current is sensed at the source, and the cable de-energized until it is re-connected. The POE standard stipulates a limit of 13 watts for each powered device. This card consumes about eight watts with a DC-DC converter efficiency of about 75% resulting in a delivered power of about six watts.

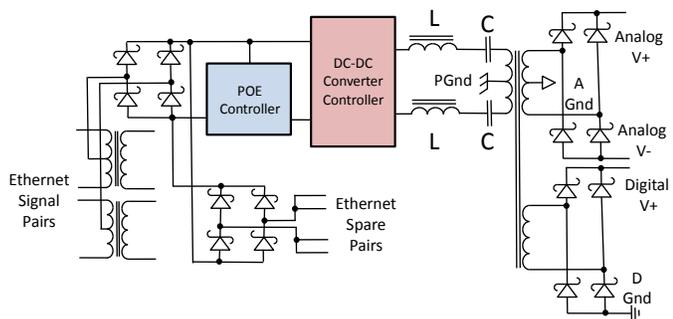


Fig. 1. Power Supply primary side block diagram. L and C form the resonant tank

### A. Power Supply

The prototype versions differed mostly in their power supply designs. The first used five push-pull converters to generate the +3.3 digital,  $\pm 5V$  and  $\pm 15V$  digital supplies. The second used three Cuk topology converters and the third a single resonant converter which generates  $\pm 5.5V$  for the analog section and +5.5V for the digital section. Secondary buck converters are used to generate the +3.3V, +1.8V and +1.2V needed by the digital section. A secondary Cuk and SEPIC converter generate the -15 and +15 volts required by the charge amplifiers and LED pulsers. These converters used coupled inductors to achieve very low ripple.

A persistent problem in the first two design iterations was the fast edges of the converter switching waveforms coupling through the inter-winding capacitance of the power transformer. To reduce this effect, the primary and secondary windings need to be placed physically separated on a multi-section bobbin. However, this increases the transformer leakage inductance which in turn causes ringing and overshoot on the switching waveforms. A solution to this problem is a resonant mode converter[2]. The transformer is part of a resonant tank that includes the transformer leakage inductance. There is very little ringing and overshoot in the power stage. The control variable is frequency rather than duty cycle. The supply is operated above the resonant frequency of the tank. Raising the frequency moves the supply further from resonance, lowering the output voltage. Lowering the frequency moves the operation toward resonance, raising the voltage. Quasi-sinusoidal current flows in the transformer windings, limiting the higher order harmonic content generated on the primary side of the transformer.

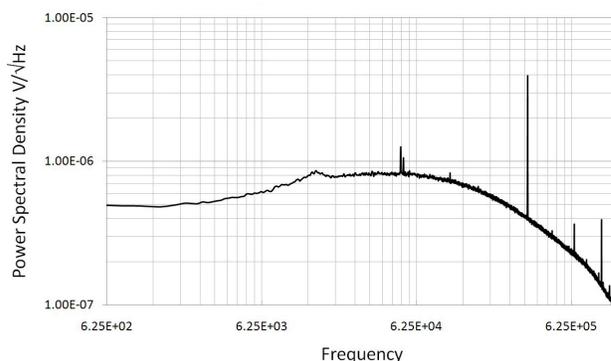


Fig. 2. ADC input referred room temperature noise spectrum of a charge channel. The RMS noise is about 0.1fC. The higher order harmonic content is small.

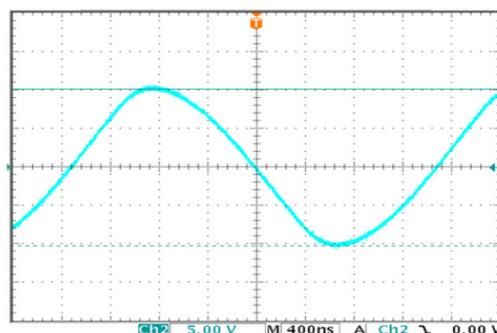


Fig. 3. Transformer primary current. The scale is approximately 680mA/Div

The drawbacks of a resonant converter include high peak currents, slow transient response, due to the Q of the tank, and the risk of having the controller frequency fall onto the wrong side of the resonance peak which results in a positive feedback condition. By operating at a relatively high frequency (330 KHz) and a relatively low Q factor ( $\sim 1$ ) the transient response is acceptable. For a supply delivering a few watts, the peak currents are not an issue. The available controller ICs have precise oscillator parameters so that the operating frequency range can be guaranteed to be on the desired side of the resonance curve. At this operating frequency Litz wire must be used in the transformer windings to mitigate copper losses.

### B. Analog Section

#### 1) Phonon Channels

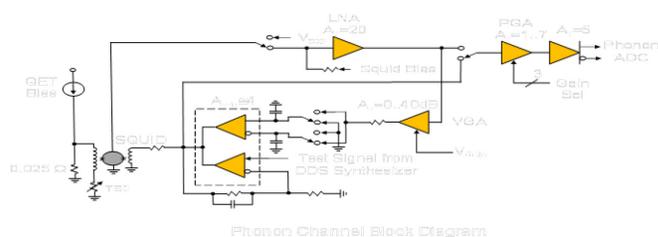


Fig. 4. Block Diagram of one Phonon Channel

The first gain stage for the TES signal is a SQUID amplifier. In response to impinging phonons, the TES changes its resistance, resulting in a current change in a coil mounted over the squid. The SQUID response to ambient flux is  $\text{Cos}^2(\Phi)$ [3], so a feedback loop is implemented to hold the total flux generated by the input and feedback coils at the device constant. SQUIDS are not mass produced and do not have the advantages of process characterization realized at high volume microelectronic fabricators. For this reason, there are several control variables implemented for each individual SQUID channel to adapt a channel to the peculiarities of any given device. These include feedback loop polarity selection and feedback loop bandwidth adjustment. SQUIDS also require “zapping”, where relatively high currents are sent through the device in order to raise their temperature above the superconducting transition to remove any trapped flux.

When the various adjustments are being made, the relevant quantity being digitized is the amplified SQUID signal. There is an on card signal generator driving (typically) a triangle wave into the feedback line of the SQUID channel as part of the “SQUID tuning” process. When in normal operation, it is the feedback signal that is digitized.

## 2) Charge Section

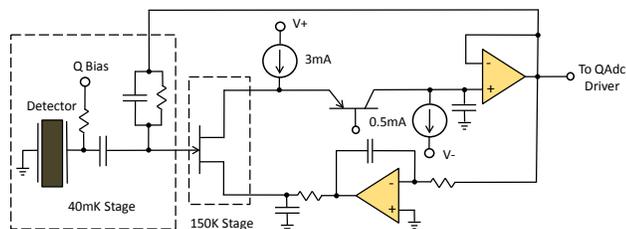


Fig. 5. Block Diagram of one Charge Channel

The ionization signal from the detectors is connected to a standard topology JFET charge amplifier. Current source biasing is used to reduce sensitivity to power supply noise. The current setting resistors in the charge amplifier biasing networks need to be large in order to keep down thermal noise currents necessitating the use of  $\pm 15\text{V}$  power supplies. To reduce low frequency noise, the feedback resistor is cooled to 40mK. To reduce device white noise, the JFET is cooled to about 150K, where there is a noise minimum. [4]

There is in addition a feedback loop used to hold the gate of the JFET at zero volts. This is done to reduce the effects of any acoustic vibration of the wires attached to the gate. The amplifier output is fed to a fixed gain post-amplifier which is in turn attached to the charge ADC.

## 3) Additional Features

The detectors are insulators when cold. As a result, charge accumulates and must be periodically neutralized with photons from LEDs mounted inside the detector towers. At these low temperatures the forward drop of the LEDs is of order 11V, so these pulsers also require 15V power. Two current mode pulse generators with programmable pulse parameters and current settings are provided.

A direct digital synthesis (DDS) chip is included on the card. The output of the chip goes to a series of switches that connect to a variety of points on the card. It can be connected to the QET bias lines or the SQUID feedback amplifier. The DDS chip is capable of performing a frequency sweep. During this sweep, amplitude and phase data are recorded in the data buffer. From this a Bode plot of the phonon channel can be made. There is no test signal connection to the charge, but stepping the charge bias line DAC generates a measurable charge signal.

## C. Digital Section

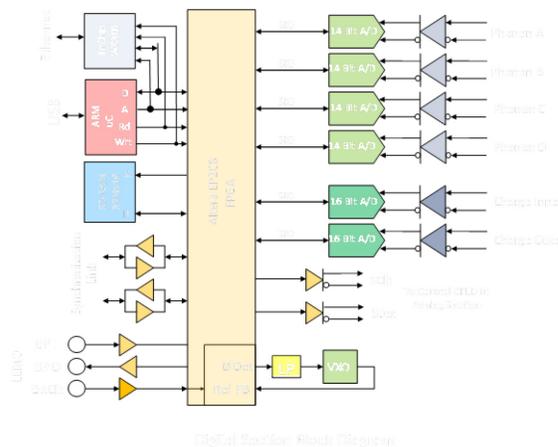


Fig. 6. Block Diagram of the digital section

The Phonon channels are connected to 14 bit digitizers running at 2.5MSPs. Two samples are averaged before being written to the data buffer at 1.25MSPs. This simplifies the design of the anti-aliasing filter at the phonon ADC inputs. The charge channels use 16 bit digitizers running at 2.5MSPs.

The data buffer consists of a 32Mx16 SDRAM. The RAM operates at 50MHz which is fast enough to simultaneously supply data to the Ethernet link and accept data streaming in from the ADCs. Within the FPGA FIFOs are used to absorb the time uncertainties of the SDRAM accesses. The buffer is logically divided into six blocks mapping onto the six physical channels. The microcontroller is an ARM architecture running at 80MHz.

The on-card trigger algorithm is fairly simple. Two running averages of ADC samples are kept for each channel. A longer average (typically 32 samples) is used to establish a baseline. A shorter average (typically 2 samples) is used as the signal sample. If the difference between the baseline and signal average exceeds a threshold value, a trigger occurs. The averages are programmable in length, with one pair of values for phonons and one for charge. There are individually programmable thresholds for each channel. If a more sophisticated trigger is desired, information from multiple boards is sent to central trigger processor. For purposes of synchronization, cards can be bussed together using standard Category 5 patch cables. The clock frequency from one card, designated as the reference source, is transmitted to the other cards on the bus and used to phase lock their system clocks. By this means, all buffer write pointers move in lock step. A

trigger from one card can be used to locate the corresponding time region on another, whether or not the local trigger on that card was satisfied.

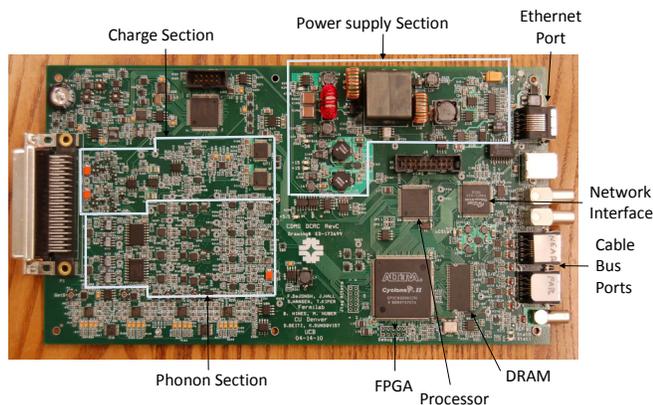


Fig. 7. Photograph of the card with the relevant sections labeled.

#### IV. STATUS

To date, the first version of the card has been in use at a detector test facility at the University of Florida in Gainesville. Evaluating the card has been complicated by the fact that the entire test stand is a new installation and it has proven difficult to separate external environmental issues from those specific to the DCRC. Nevertheless detectors are now being routinely tested. As of this writing, eight of the latest version cards have been assembled and will shortly be sent to five test stand installations around the country.

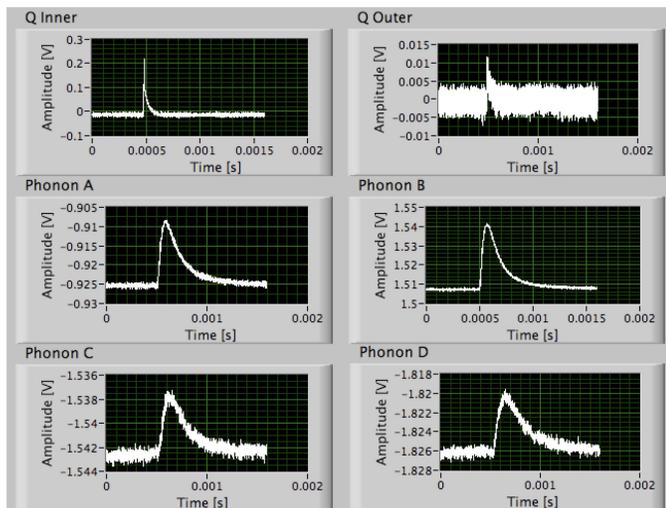


Fig. 7. Screen capture six channels responding to a transiting muon recorded at the Berkeley test facility.

#### V. FUTURE PLANS

The CDMS 100 kilogram installation at the Sudbury Neutrino Observatory will consist of 40 germanium detectors each of which will require readout of 10 phonon channels and four charge channels. A new design will be required. Recently introduced multi-channel ultrasound processing chips appear to be a promising avenue of investigation for the phonon readout for the next generation of cards.

#### REFERENCES

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