Pixel Detectors in 3D Technologies for High Energy Physics

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Abstract- This paper reports on the current status of the development of International Linear Collider vertex detector pixel readout chips based on multi-tier vertically integrated electronics. Initial testing results of the VIP2a prototype are presented. The chip is the second embodiment of the prototype data-pushed readout concept developed at Fermilab. The device was fabricated in the MIT-LL 0.15 μm fully depleted SOI process. The prototype is a three-tier design, featuring 30×30 μm^2 pixels, laid out in an array of 48×48 pixels.

I. Introduction

Three-dimensional (3D) integration techniques bring solutions to pixel-segmented integrated system problems that have been unsolved for years. Scientific instruments are typically fabricated in small volumes, but encompass special needs, like large sizes of imaging fields and tens of millions of channels. Improving power distribution, allowing dead-zone-free large area pixel sensors, allowing complex parallel, processing and optimizing attachment of the readout to the sensors are the main areas where 3D techniques offer advantages. 3D integrated circuits (3D-ICs) are formed by bonding two or more IC wafers (tiers) and interconnecting them with micron or so –size through silicon vias (TSV)

Fermilab participated in two 3D Multi-Project-Wafer (MPW) runs by MIT-LL, where three 6" SOI wafers with a 400 nm thick BOX, a 50 nm thick SOI layer, 3 routing metal layers fabricated in a 0.18 μm or 0.15 μm fully depleted SOI (FDSOI) process, were stacked using the via last approach. The thickness of the whole structure is about 700 μm while the 3 active tiers are only about 22 μm in total. Each TSV occupies effectively about 5×5 μm^2. This includes pads receiving vias on lower tiers of the stack and clearances between neighboring vias. A TSV can be a buried via, or a fully stacked pillow [1].

Two versions of a 2.5×2.5 mm^2 prototype pixel readout chip, called VIP1 and VIP2, standing for Vertically Integrated Pixel, were submitted in 2006 and 2008, respectively. The VIP chips implement the functionality required by the vertex detector at the ILC [2]. The VIP2 design branched off in two designs: the first one is VIP2a, realized in the MIT-LL process, delivered from fabrication in August 2010 and described in this paper and VIP2b is the original design migrated to the two-tier 0.13 μm Tezzaron/Chartered process. The latter is still expected from fabrication. The VIP1 and VIP2a prototypes feature a 64×64 array of 20×20 um^2 pixels and a 48×48 array of 30×30 um^2 pixels, respectively.

The paper reviews the concept of the VIP design. Section II describes implemented functionality, section III reviews achievements of VIP1 and strategy for the design of VIP2a, section IV presents preliminary results of tests of VIP2a and the discussion of technology constraints is given in the last paragraph.

II. Implemented functionality

The VIP2a is almost identical to its predecessor VIP1. The chip operates in the data sparsified (data-pushed) readout mode with the data sent off the chip between the bunch trains in synchronization with the accelerator cycle. The information provided by the chip includes digital x-y address of the pixel hit by a radiation event, digital and analog time stamping of the particle incidence time and analog samples of signals taken at the opening of the integration window and after some delay upon exceeding the discrimination threshold by the signal. Analog signals can be used for characterization of the in-pixel analog chain in tests as well as for obtaining more precise estimation of impact positions of particles. The size of the pixel of a square side between 20 and 30 μm is determined by the need of a few-micron position resolution that should be provided by the detector plane for the innermost layers of the ILC vertex detector. The functionalities, described above, translate into the transistor level architecture that is real-estate hungry. In order to fit the circuitry into the constrained space, 3D integration technology has no alternatives. The analog circuitry is on the closest to the detector top tier, and the digital is on the farthest from the detector bottom tier. The middle tier hosts the analog and digital time stamping blocks. There are about 200 transistors per pixel. The detailed description of the VIP architecture and the test results of the VIP1 prototype are given in [3]. Small prototypes of VIPs are extendable to sizes of 1024×1024 pixels, bearing the actual needs of the application. The top tier contains a gated charge integrator, a single ended AC-coupled offset corrected discriminator with capacitively injected threshold, an analog memory for reference sample, an analog memory for post discriminator sample, a pulse generator for time stamping lock and hit information lock, a receiving part of test-charge injection capacitance and a bonding pad to the detector. The intermediate tier features an analog memory cell for time stamping (distributed voltage ramp), a 7-bit SRAM-like digital time stamping memory with output enable control to read on the same lines on which time ticks in Gray code are distributed. The bottom tier hosts the sparsification system: token propagation logic, wiredOR line access logic for X-

line/Y-line of a hit pixel address generator, test-charge injection logic and a peripheral serialization and output part

III. Review of VIP1 and strategy for VIP2a design

The tests of the VIP1 chip showed that the device functioned properly, but had a very poor fabrication yield. The drop in yield was attributed in major part to the tradeoffs in performances of mixed-mode circuitry encountered in advanced deep-submicron node FDSOI processes. Various factors, like bipolar effects in transistors with floating or having resistive bulk connections (sample-and-hold circuits losing stored charges due to parasitic bipolar transistors switching on under certain bias and driving conditions), oxides impeding heat flow, straining of transistors on the BOX (dispersions in current mirrors defining polarization current for the circuitry), travel of ions through ubiquitous oxides (instabilities in characteristics of transistors), etc. were identified as possible causes of the observed performance deficiencies. Shifts of threshold voltages of transistors, of up to 200 mV, were observed on the intermediate tier as the result of 3D stacking. The intermediate tier was bonded face-to-face to the bottom tier and the handle part of the intermediate tier was removed, the top tier was face-to-back bonded to the intermediate tier. The process of preparation of the intermediate-tier-wafer for bonding requires several operations targeting flat surface for oxide-oxide bonding. The side effect of these operations was charging of the exposed BOX layer of the intermediate tier. No signs of failures of TSVs were observed on the tested chips. However, some chips were found with failures of connections, i.e. shorts between power supply rails or lack of connections between any nodes. There was at more than 10% of tested chips in which shorts and open circuits were detected. Since the functioning of the top tier does not depend on the connectivity provided by TSV, the described failures were attributed to the imperfections of the planar processing of the wafers, excluding their occurrence due to the 3D stacking. Unexpectedly, high leakage currents in active devices and soft-shorts between the nodes that were not directly connected but were used within the same circuit blocks were observed. The leakage current of the ESD-protection diodes was many orders of magnitude higher than expected a few pA levels.

The weight was put on conservatism in the VIP2a design. The architecture of the VIP1 chip was essentially preserved. A few modifications, allowing fuller testability and correcting obvious imperfections, were introduced. The main architectural modifications include: increase number of bits in digital time stamping from 5 to 7, add clearing of the sparsification circuitry from spurious hits simultaneously with arming of discriminators and reading a fixed analog voltage from the correlated double sampler in case of no hit in the pixel (for example in the test mode). The routing of the signal, used to arm discriminators, was done fully on the digital bottom tier with vertical taps connecting directly to the switches in discriminators thanks to an additional TSV between the bottom and top tier in every pixel. This way of elimination of coupling of a digital signal to a highly sensitive analog amplifier is an example of effective use of opportunities offered by 3D technologies. Another modification is abandonment of dynamic d-flip/flops to static devices. For improvement of yield, a set of self-imposed guidelines was adopted, targeting increase of yield and improved circuit operation as an outcome of the analysis of the VIP1 results and consultations with the MIT-LL experts. The original MIT-LL rules for trace routing were scaled by a factor of 1.2, resulting in wider paths and larger clearances to avoid shorts. The minimum transistor sizes, were increased ($2\times W_{min}$ and $2\div3\times L_{min}$), bringing the process to a 0.35 μm feature size equivalent in order to decrease off-state leakages and to average structural effects. Sizes of all capacitors in sample-and-hold circuits were increased at least 2 times. Selection between 3 pull-up strengths on wiredOR lines were added in the address generator of hit pixels. Source followers, outputting analog signals in VIP1, were replaced by regular buffers built with OTAs. The power and ground routings were strengthened by linking them in an extensive mesh with connections between tiers in each pixel.

IV. Preliminary results of tests of VIP2a

Tests of the VIP2a chip aim at characterization of individual blocks with emphasis on the analog front-end part, verification of ability to access circuitry on each tier and of correctness of its operation and eventually assessment of the full functionality of the chip. Test structures, featuring fully functional copies of the analog part of the pixel, were placed aside of the matrix of pixel on the top tier and they were characterized at the first step. Test charge could be injected through a 2.7 fF capacitor placed in series to the integrator input. An additional 20 fF capacitor could be added to increase the input load, mimicking connection to the detector. The analog current biases were 4.8 μA and 0.97 μA for the integrator and the discriminator, respectively. The voltages did not differ from those used in the simulation. Releasing of the integrator reset starts the integration phase and about 1 fC of charge is injected to the input of the integrator. Releasing of the discriminator reset arms the discriminator and automatically cancels offsets. Providing a voltage step across a capacitor connected to the input of the discriminator sets the threshold for triggering of the latter upon the signal from the integrator. The first analog sample is taken at the moment of arming of the discriminator. The second sample is taken after the discriminator fires and an internally set delay of about 500 ns in order to make sure that the signal has time to fully settle. The voltage signal corresponding to the integrated charge is the difference of these two samples. Very good linearity of the integrator response was measured for input signals of up to 3 fC. The response of the charge integrator to the injection of charge equal to about 1 fC is shown in Fig.1 for 0 fA and 20 fF of the input capacitance C_{in}. The gain is approximately 200 mV/fC at C_{in}=20 fF. The gain is higher for no capacitive load at the input. Low open loop gain of 32 dB of the amplifier, building the charge integrator, gives rise to this gain variation. The rise-time of the integrator signal was measured 228 ns and 120 ns at C_{in}=20 fF for active and released discriminator reset, respectively. A threshold of

0.1 fC is injected internally when the discriminator reset is released. This initial value is sufficient to maintain the discriminator in the armed state until the injection of the threshold, which should occur immediately. A threshold pulse just adds to that initial level with either positive or negative sign. An intrinsic delay of the discriminator for triggering on large signals is about 200 ns.

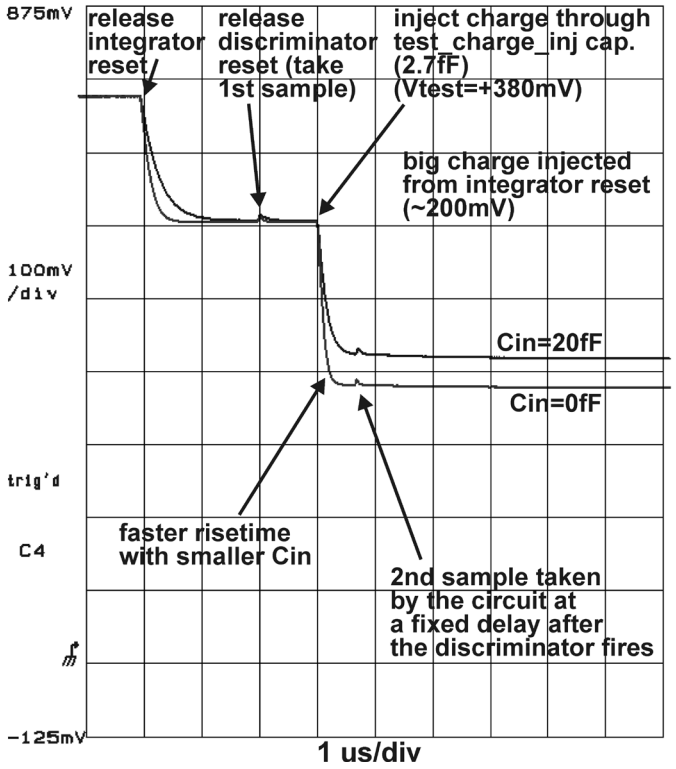

Fig. 1. Integrator response for 0fF and 20fF of input capacitance, C_{in}.

Noise of the analog front-end part was measured performing actual acquisition with a small injected charge signals. The signals were injected varying the delay after having the discriminator armed, resulting in correlated double sampling processing with different time intervals. The results of the noise characterization are given in Fig. 2.

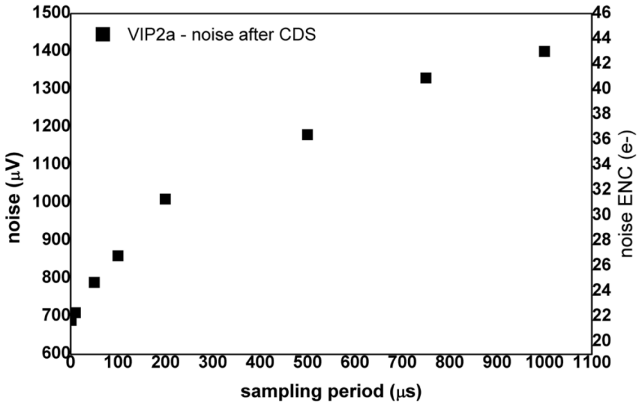

Fig. 2. Noise as a function of sampling interval for C_{in}=20fF.

The right axis gives noise values expressed in equivalent noise charge (e^-) calculated using the 200 mV/fC charge-to-voltage conversion factor. The intermediate tier hosts a generator of a voltage ramp used in the analog time stamping. An input current is divided by 10 and integrated on a 5.5 pF capacitor. The resulting voltage is buffered by a voltage follower, built with a rail-to-rail class A-B operational amplifier. The ramp voltage is distributed to all pixels in the matrix. All biases and control signals for the ramp generator are routed from the top tier. The transfer characteristics of the 10:1 current mirrors in the ramp generator are shown in Fig. 3 for two tested chips. Significant improvements of performance of current mirrors with respect to VIP1 were observed. The division ratio of the current is maintained over 3 orders of magnitude and no excessive leakage currents were detected.

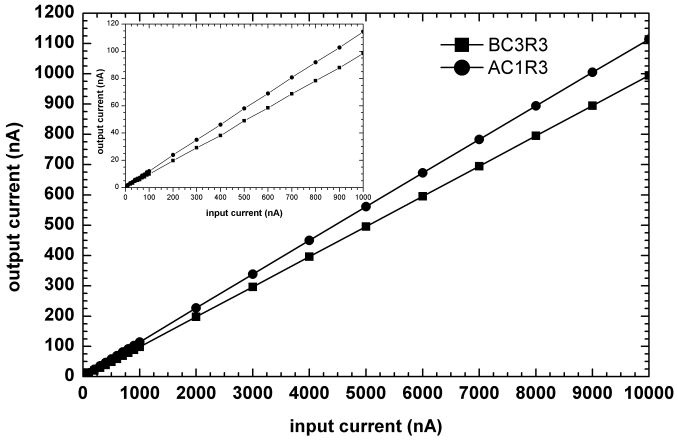

Fig. 3. Transfer characteristics of the 10:1 current mirror in the ramp generator.

The ramp generator was characterized by measuring time jitter of the ramp rise time and linearity of the ramp at constant ramp bias current. The results of measurements of time needed for the ramp voltage to rise from 200 mV from the ground rail to 200 mV below the power supply rail (thus 1.3 V in total) as a function of the ramp bias current is shown in Fig. 4 for two different VIP2a chips. The ramp could be controlled thorough the whole range, which has practical importance for the functioning in the ILC environment, i.e. from 10 μs to 1 ms. The time jitter and the linearity were measured better than 1%.

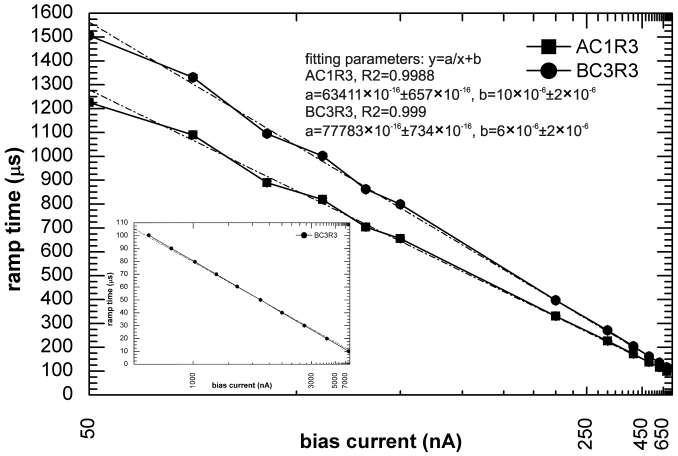

Fig. 4. Time needed for the ramp voltage to rise from 200 mV from the ground rail to 200 mV below the power supply rail as a funtion of the ramp bias current.

The input voltage offset of the operational amplifier did not exceed 10 mV.

An important test of the sparsification circuitry at the bottom tier is the verification of the integrity and measurement of the speed of the token propagation chain. At the beginning of the readout phase, the token is injected into the matrix of pixels and starts racing to find the first hit pixel. When the hit pixel is found, the first readout clock pulse releases the position and time stamp information for readout and the token can continue until it stops at the next hit pixel. The maximum readout clock frequency is determined by the token propagation delay. It must be slow enough that the readout cycle is longer than the time needed to find the next hit pixel or token exits the matrix. The tests of token propagation were done by measuring the delay time of both edges of the square pulse injected to the token input to the matrix. The matrix was emptied beforehand from any hits by performing a full readout procedure until the matrix was transparent for the token. The token propagation delay calculated per pixel for 3 different chips is shown in figure 5 as a function of the digital power supply. The propagation delay time is almost 2 times longer than it was measured for the VIP1 chip. The increase of the token propagation time is due to the increase of sizes of transistors and consequent increase of the pixel size. However, the token propagation logic functions correctly within the whole range of power supply voltages on almost all tested chips, which was not the case of the VIP1 chip.

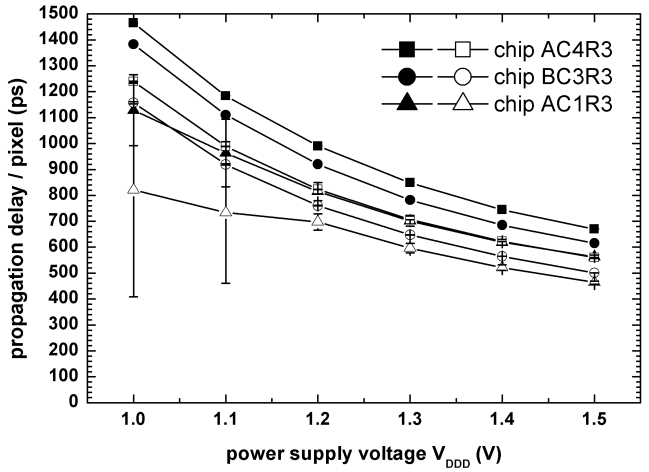

Fig. 5. Token propagation delay per pixel for different chips at different power supply voltages.

V. Technological constraints

Conclusions after the initial testing phase clearly show the effectiveness of the adopted very conservative design rules. Of the 7 VIP2a chips tested so far, only 2 devices did not work. One of these not working chips is an open circuit. At the same time, the improvement of the process should be noted, which is for example visible through a drastic reduction in leakage currents. However, the shift of threshold voltages of transistors on the intermediate tier, which is most probably the result of the 3D bonding, was measured to 150 mV with respect to the simulation models.

Although the VIP2a device shows encouraging improvements, it is rather believed, exploring also available expertise, that the FD-SOI approach has the shortcomings for mixed-mode design. The problems are even more pronounced in the 3D stacking of FD-SOI wafers, as ubiquitous oxides do not provide any possibility of shielding, making the devices vulnerable for inter-tier coupling and radiation damage due to the charging of oxides as a result of the accumulation of ionizing doses. In order to experimentally verify whether better performance can be achieved from bulk CMOS processes, the translation of the VIP1 design into the 3D integration process using bulk CMOS wafers done. The delivery of the VIP2b chip is expected in the fall 2010.

VI. Conclusions

The VIP2a chip is the second realization of the pixel readout concept for the ILC in the 3D process at Fermilab. Based on the VIP1 experience, a set of conservative design rules was adopted, targeting improvement of yield. The use of these rules translated to the larger pixel size and slower operation of the device, however the yield seems to be improved. The VIP2a chip is a 48×48 array of 30×30 μm^2 pixels. There are about 200 transistors in each pixel implemented the whole functionality of the data pushed readout. Without the 3D integration technology, enabling higher densities of electronic circuitry per unit area, implementation of the VIP2a functionality would not be possible. The size of the prototype is 2.5×2.5 mm^2, however the architecture of VIP2a allows an easy expansion to 1000×1000 pixels. The power dissipated by a full scale version of this chip is consistent with the air cooling requirements of the ILC pixel vertex detector. The support logic around the perimeter of this chip is small. In future designs, this can be reduced further.

The VIP2a chip was submitted for fabrication in the 3DM3 0.15 μm FD-SOI multi-project run at MIT-LL in October 2008 and the dice were delivered in August 2010. The tests of the VIP2a chip are underway. Some selected results were presented in the paper. The front-end part was characterized using tests structures placed aside of the matrix of pixels, verification of ability to access circuitry on each tier and of correctness of its operation was achieved. A bug, related to the timing of the clock signals in the sparsification, was found, requiring alteration of the readout protocol in order to achieve assessment of the full functionality of the chip, which is expected soon.

References

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