

Pixel Multichip Module Development at Fermilab

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Abstract

At Fermilab, there is an ongoing pixel detector R&D effort for High Energy Physics with the objective of developing high performance vertex detectors suitable for the next generation of HEP experiments. The pixel module presented here is a direct result of work undertaken for the cancelled BTeV experiment. It is a very mature piece of hardware, having many characteristics of high performance, low mass and radiation hardness driven by the requirements of the BTeV experiment.

The detector presented in this paper consists of three basic devices; the readout integrated circuit (IC) FPIX2A [2][5], the pixel sensor (TESLA p-spray) [6] and the high density interconnect (HDI) flex circuit [1][3] that is capable of supporting eight readout ICs. The characterization of the pixel multichip module prototype as well as the baseline design of the eight chip pixel module and its capabilities are presented. These prototypes were characterized for threshold and noise dispersion. The bump-bonds of the pixel module were examined using an X-ray inspection system. Furthermore, the connectivity of the bump-bonds was tested using a radioactive source (^{90}Sr), while the absolute calibration of the modules was achieved using an X-ray source. This paper provides a view of the integration of the three components that together comprise the pixel multichip module.

I. INTRODUCTION

The pixel multichip module is based on a design relying on a hybrid approach [1]. With this approach, it is possible to separately develop the readout integrated circuit (IC) and the sensor array, retaining flexibility in the development process. After both sensor and readout IC are developed, the detector module is constructed by flip-chip mating the two devices together. Once the detector module is put together, it is glued to the high density interconnect (HDI). The pads on the readout ICs are then connected through wire bonds to the correspondent pads on the HDI.

The flip-chip mating was done by VTT [7] using

solder bumps. Before flip-chip mating, the readout ICs were thinned to $200\mu\text{m}$. Another advantage of this hybrid approach is that the readout IC can be used with different types of sensors.

The pixel module presented in this paper can be used in pixel detectors employed for applications such as on-line track determination and vertex location. The pixel module presented is suitable for applications in vacuum, in very strong magnetic fields and at temperatures ranging from -10°C to 60°C . It is also designed to be radiation tolerant. The module does not have any ferromagnetic components. In addition, the multichip module components were chosen to have minimum outgassing while being irradiated. To achieve radiation hardness the readout IC was designed using $0.25\mu\text{m}$ CMOS process technology with radiation tolerant design rules. Finally, to operate in a wide range of temperatures, the materials of the packaging were chosen to minimize the mismatch between the coefficients of thermal expansion (CTE) of different materials and the readout IC.

II. PIXEL MODULE ELECTRONIC CAPABILITIES

Presently, the dimension of the pixel readout IC array is 128 rows by 22 columns and the information regarding signal pulse height is provided by an internal 3 bit ADC on every pixel. This makes the eight-chip module an array of 22,528 pixels with a density of around 5000 pixels/cm^2 .

The sensor pixel size is $400\times 50\mu\text{m}^2$ for the 20 internal columns and $600\times 50\mu\text{m}^2$ for the columns on edges of the readout IC. The pixel pitch in the 128 rows is $50\mu\text{m}$, while the pixel pitch in the 22 columns is $400\mu\text{m}$. The extension from $400\mu\text{m}$ to $600\mu\text{m}$ applies only to the sensor and not to the readout ICs.

The readout ICs can have the threshold set in a collective mode in which all chips in the module are set to the same threshold or in an individual mode in which each chip can have a separate threshold setting. The minimal collective threshold at 20°C was 2100 electrons while the minimal individual threshold at 20°C was 1900 electrons.

All tests performed were done with the chip running at a clock rate of 40MHz. The module was tested at a data rate of 320 Mbps although it can support much higher data rates. This is possible because the eight-chip module possesses 26 serial lines distributed as shown in Figure 1.

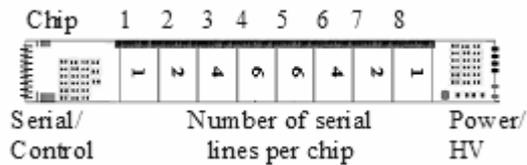


Figure 1 Pixel module serial configuration.

The module is also capable of providing information about the analog output for cell 0,0 for each chip. This information can be probed on an extended pad at the HDI. This is very useful for studying the performance of the preamplifier.

The readout IC is data-driven (does not require an external trigger) so the module is always collecting data (if it has been enabled to do so). To avoid bursts of current between periods of high activity and periods of low activity, the chip sends synchronization words on a periodic basis as shown in Figure 2.

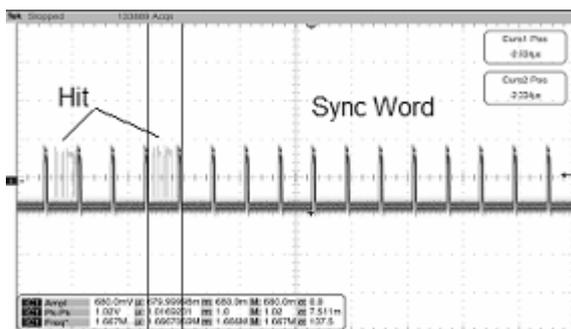


Figure 2 Serial line output.

The readout IC was tested with both analog and digital power supply voltages at 2.5V, and then with both at 2.2V.

Both configurations proved to work well. The power consumption for 2.5V was 1.86W when the chip was idle and 2.26W for the chip collecting data at 320Mps (million samples per second). Powering the chip with 2.2V provided a drop in power consumption to 1.51W when idle and 1.83W when collecting data at 320Mps. The multichip module had a slight reduction in noise and threshold dispersion when operating at 2.2V. The noise dispersion improvement was approximately 0.5 electrons while the threshold dispersion improvement was approximately 20 electrons. These improvements were constant in the temperature range between -10°C to 60°C.

III. MODULE COMPONENTS AND ASSEMBLY

The pixel multichip module prototype is composed of three layers, as illustrated in Figure 3a, 3b, and 3c. The HDI forms the bottom layer (Figure 3a). The back of the readout IC (Figure 3b) is in electrical and thermal contact with the ground plane on the top layer of the HDI, while the other side of the readout IC is flip-chip bonded to the silicon pixel sensor (Figure 3c). The clock, control, and power pad

interfaces of the readout IC extend beyond the edge of the sensor and are wire bonded to the HDI. The HDI then extends to one end of the module where a set of wire bond pads interface the HDI to the data acquisition system. At the other end, a set of pads interfaces with power and high voltage lines through wire bonds (see Figure 1). The large number of signals in this design impose space constraints and require aggressive design rules, such as 50µm trace widths, center-to-center pitch of 50µm, and via pads of 150µm. The feature sizes of the HDI can be observed in Figure 4.

This packaging requires an HDI with four layers of copper traces. The data, control and clock signals use the two inner layers. These signals are differential and the HDI lines are impedance controlled to 100Ω. Power is routed on the bottom layer, while a single ground uses the top layer. The HDI has two power traces, one analog and one digital. The decoupling capacitors in the HDI are located on both sides of the HDI as close as possible to the detector. The trace lengths and vias that connect the capacitors to the chips are minimized as much as possible to reduce the interconnection inductance.

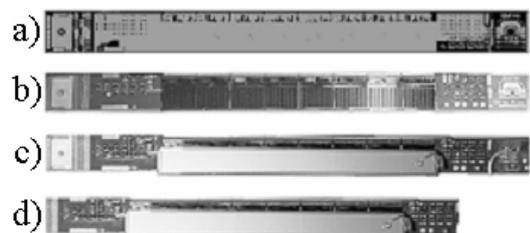


Figure 3 a) Top view of the HDI (CAD). b) Pixel module with bare dies. c) Pixel module with sensor. d) Pixel module ready to be used.

To minimize coupling between digital and analog elements, signals are grouped together into two different regions. The digital and analog traces are laid out on top of the digital and analog power supply traces, respectively. Furthermore, a ground trace runs between the analog set and the digital set of traces.

The pixel sensor is biased through the HDI providing up to 1000VDC. The high voltage trace is connected to a pad on the top layer of the HDI, which is then wired to the sensor. A high voltage capacitor and a resistor were used to filter the high voltage line.

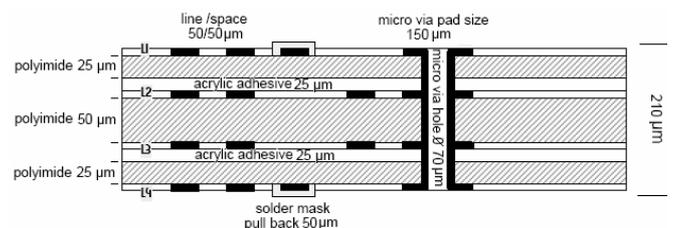


Figure 4 HDI fine features.

After the sensor is placed on the HDI, the wire bonding is done on the chips and on the HDI's tabs. The tabs are located on the edges of the HDI and they are only used during the testing of the module on the test card. After the testing the

tabs are cut off from the HDI and the module is ready to be used (Figure 3d).

Electrically conductive silver epoxy was used to connect the back of the readout ICs to the ground plane on the top layer of the HDI. The HDI wire bond pads extend 1mm beyond the readout ICs. In order to provide mechanical support to the wire bond section of the HDI, the whole module is assembled on a test board card (Figure 5).

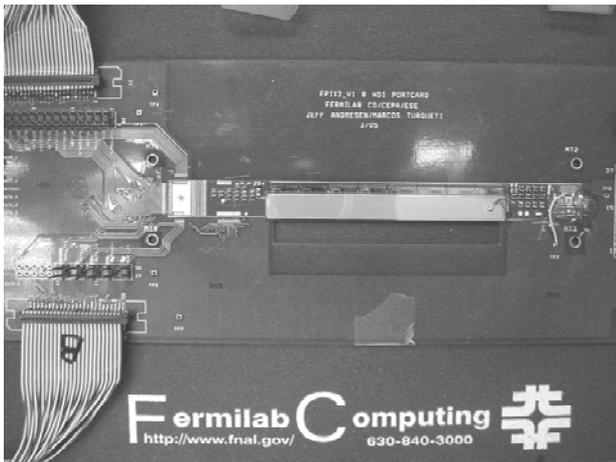


Figure 5 Module assembled on the test card.

IV. PIXEL MODULE EXPERIMENTAL RESULTS

In this section, the characterization results of one pixel multichip module are presented. The pixel module has been characterized for noise and threshold dispersion. These characteristics were measured by injecting charge in the analog front end of the readout IC with a pulse generator and reading out the hit data through a PCI based test stand developed at Fermilab. Five of the eight chips of the module with sensor were characterized for threshold noise and the hit map was also checked (the other 3 chips were tested only for functionality due time constrains).

The results of the characterization process are summarized in Table 1. It is also important to mention that these values are absolute values. The thresholds were set to just above the minimal possible effective individual value for each chip at 20°C.

		Chip 1	Chip 2	Chip 3	Chip 4	Chip 6
Threshold	μ	1900	2000	2000	2100	2000
	σ	200	195	200	205	195
Noise	μ	86.4	85.6	92	88	88
	σ	8	7.2	8.4	8.5	7

Table 1 : Performance of the pixel prototype module (in e^-).

The comparison of these results with the single bare die readout IC (without the HDI) shows little degradation in the electrical performance of the pixel module. The results with

these bare die readout ICs show a noise of $70e^-$ and a threshold dispersion of $180e^-$ [2].

The absolute calibration was carried out using an ^{241}Am source that provided five different energy peaks (Figure 6). Each peak can be selected in the source using the corresponding metal sheet that will fluoresce at the desired specific energy. To generate the curve shown on Figure 6, the source was placed over the target chip at a distance of 1 cm from the detector. A calibration program changed the threshold register of the chip every 2 minutes. During these intervals of time the chip was receiving hits and sending them to the calibration program. This process was repeated for all five chips characterized.

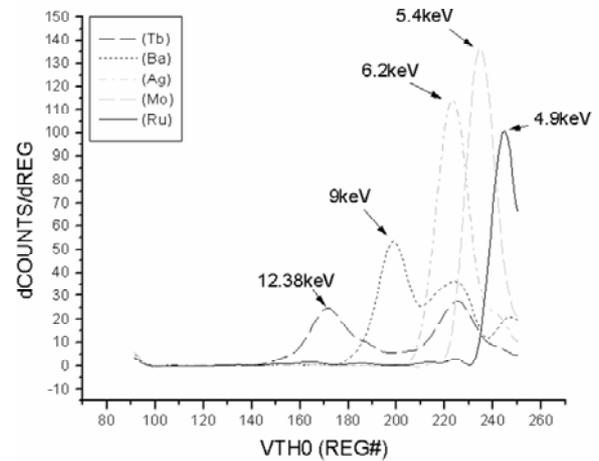


Figure 6 Absolute calibration of the chip 2.

Figure 7 shows hits on the pixel module using a radioactive source (^{90}Sr). This result was obtained by placing the radioactive source at a distance of 4 cm from the module, centred on chip 2.

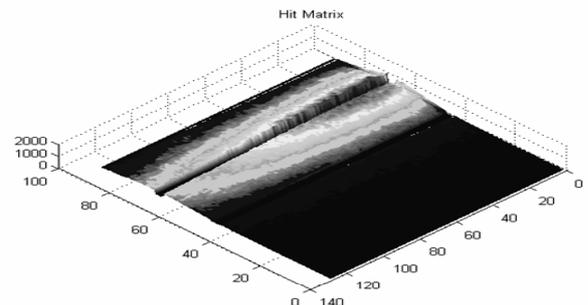


Figure 7 Beam profile of the Beta Gun (^{90}Sr).

This same process was performed to determine the hit map of the five chips analysed resulting in a total of 14080 pixels analysed. From this analysis, 21 pixels were determined to have open bump bonds while 116 other pixels were very noisy. These results show that the bump-bond connectivity is good.

The very noisy cells were the results of a mistake during the application of the silver epoxy between the HDI and the detector module. As the readout ICs are very thin, caution must be taken when applying the epoxy to the HDI because the epoxy can overflow to the sensor. That was the case in some gaps between the readout ICs. This was diagnosed using an X-ray inspection system [4] and it can be observed in Figure 8.

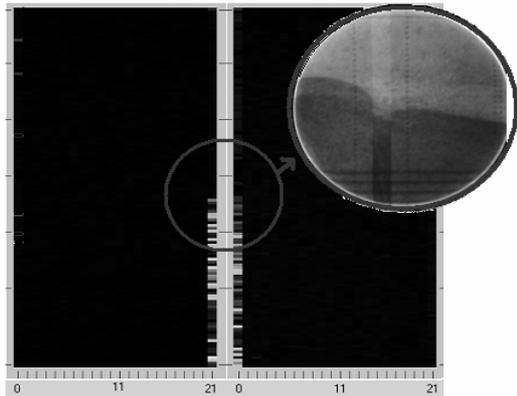


Figure 8 On the detail at the top right we can see the X-ray image of the area affected by the silver epoxy (dark area in the gap between two chips). On the main image, pixels with light color are the very noisy pixels.

V. CONCLUSIONS

In this paper we described the baseline BTeV pixel multichip module design and electronics. Furthermore, the assembly and successful testing of eight chips of the pixel multichip module prototype were presented. The details of the characterization of five chips of the module were demonstrated. The tests detected no crosstalk problems between the digital and analog sections of the readout IC and the HDI. The characterization of the prototypes showed that there is no degradation in the electrical performance of the pixel module when compared with previous prototypes. Furthermore, the pixel module showed no significant increase

in noise or threshold dispersion when compared with the single chip bare die prototypes.

VI. REFERENCES

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