

# Study of Temperature Dependence of Bump Bonding for the BTeV Pixel Detector

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*Abstract--* The pixel detector proposed for the BTeV experiment at the Fermilab Tevatron will use bump-bonding technology based on either Indium or Pb/Sn solder to connect the front-end readout chips to the silicon pixel sensors. We have studied the behavior of the bumps by visual inspection of the bumps bonding silicon sensor modules to dummy chips made out of glass. The studies were done before and after thermal cycles, exposure to intense irradiation, and with the assemblies glued to a graphite substrate. We have also carried out studies on effects of temperature changes on both types of bump bonds by observing the responses of single-chip pixel detectors to a  $^{90}\text{Sr}$  source. We report the results from these studies as well as the noise and threshold behavior of the pixel readout at various temperatures.

## I. INTRODUCTION

PIXEL detectors proposed for the new generation of hadron collider experiments will use bump-bonding technology based on either indium or Pb/Sn solder to connect the front-end readout chips to the silicon pixel sensors. One of these experiments is BTeV at the Fermilab Tevatron. The pixel module is the basic building block of the pixel detector. Each module consists of a single sensor that is bump bonded to a number of readout chips. The total active area of the BTeV pixel detector is about  $0.5\text{m}^2$  and the total number of pixels will be 23 million, each measuring  $50\ \mu\text{m} \times 400\ \mu\text{m}$ . The modules are supported by a graphite substrate that also provides cooling for the readout chips. Nominally, the pixel detector will be placed at 6 mm from the colliding beams and will be exposed to significant radiation. To keep the detectors in operation for 10 years, they will be operated at a temperature of  $-5^\circ\text{C}$  to  $-10^\circ\text{C}$ . The bump bonds provide both the electrical and mechanical connection between the sensors and the readout chips and are crucial to the assembly and operation of the pixel detector.

The bump bonding technology has to meet the following requirements:

1. Fine bump pitch of  $50\ \mu\text{m}$  in the narrow dimension
2. Small bump size, typically  $25\ \mu\text{m}$  or smaller in diameter
3. High density, about  $5000\ \text{bumps}/\text{cm}^2$

4. Low bump resistance
5. High yield ( $>99.5\%$ )
6. No thermal cycling effects
7. No loss in strength and connectivity after irradiation

We have previously reported large-scale tests of bonding yield using both indium and Pb/Sn solder bumps [1]. The conclusion is that both seem to be viable for pixel detectors. We have also carried out studies of various effects (e.g. storage over long periods, effect of heating and cooling, and radiation) on both types of bump bonds using daisy-chained parts on a small scale. The results were reported elsewhere [2]. Overall, these tests showed little changes in the integrity of the bump connections. Nevertheless, questions still remain on the long-term reliability of the bumps due to thermal cycle effects, attachment to a substrate with a different coefficient of thermal expansion (CTE), and radiation. These might alter the structural integrity of the bumps causing mechanical stress on the bumps resulting possible damage in the bumps among other effects. In section II of his report we address to these issues.

Since the pixel module will be built at room temperature ( $23^\circ\text{C}$ ), it will have to undergo a temperature variation of around  $30^\circ\text{C}$  many times during its operating life. The temperature variation can affect several parts of the multichip module packaging: CTE mismatches can cause the bump-bonds to break or the flex circuit to break off the pixel sensor.

The results presented in this paper show that the temperature variation has important effects on the pixel module performance. By studying the differences in the behavior between a bumped and bare chip, we can get useful information on the bump quality and integrity after thermal cycling.

We also present the results of tests performed to analyze the effects that temperature variation has on the pixel single-chip module performance regarding mechanical characteristics (bump bond reliability) and electrical characteristic. These tests include the measurement of the noise and threshold

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dispersion of all the cells in the pixel module. Sections III and IV are devoted to these presentations.

## II. SILICON-GLASS MODULES

In order to visually investigate the effects of temperature changes and radiation, we have had built modules composed of glass chips bump bonded to silicon sensors. Two of the modules, named AIT\_1 and AIT\_2, each have eight glass chips. They are indium bump bonded to ATLAS tile sensors [3] by AIT (Advanced Interconnect Technologies, Hong Kong). Each chip contains 2934 bumps. Three more modules, each with eight glass chips solder bump-bonded to the ATLAS sensors by MCNC (Research Triangle Park, North Carolina), are named MCNC\_2, 3, and 4. Each chip in these modules contains 3060 bumps. In both bump-bond technologies, an Under Bump Metallization (UBM) layer is first put on the sensors and the glass chips. With indium, the bumps will then be deposited on both the sensors and the chips. With solder, the bumps will be plated only on the glass chips. In the MCNC process, both parts were coated with BCB (Benzocyclobutane) for plating purpose.

We video-scanned these modules before and after every test stage they have gone through, and recorded the data on 8 mm tapes and DVDs. The coordinate information from the DAQ was superimposed onto the video image so that we could compare the images before and after any procedure. While having the ability of visually inspecting the changes taking place on these modules, it has to be noted that the bonding was between glass and silicon, and not silicon and silicon, which is the case in the real experiment. The CTE mismatch between silicon and glass, and the possible difference in adhesion of bumps to UBM and glass are to be considered in the interpretations of the results.

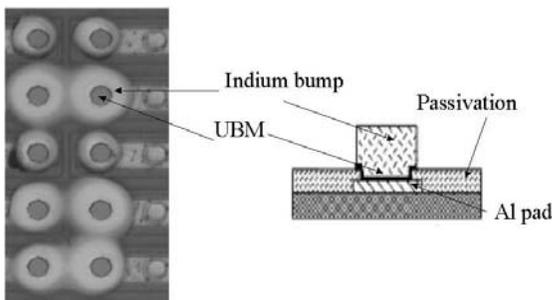


Fig. 1: Indium bumps under glass and a schematic view of a bump on a real detector

The MCNC modules have gone through the following procedures:

1. All: 6 cycles of 16 hours at  $-25^{\circ}\text{C}$  and 4 hours at room temperature,
2. 2: Irradiated to 13 MRad (using  $^{60}\text{Co}$ ),

- 3 & 4: 20 cycles of 10 hours at  $-25^{\circ}\text{C}$  and 2 hours at room temperature,
3. All: 30 cycles of 6 hours at  $-25^{\circ}\text{C}$  and 1 hour at room temperature,
4. 3 glued on a Thermal Pyrolytic Graphite (TPG) substrate. All: 105 cycles of 1 hour at  $-10^{\circ}\text{C}$  and 1 minute at room temperature (Rapid Thermal Cycling)

The AIT modules have gone through the following test procedures:

1. Both: 5 cycles of 10 hours at  $-10^{\circ}\text{C}$  and 4 hours at room temperature,
2. AIT\_2 glued on TPG. Both: 105 cycles of 1 hour at  $-10^{\circ}\text{C}$  and 1 minute at room temperature.

### A. AIT Modules with Indium Bumps

Fig. 1 shows a view of the indium bumps seen from the bottom through the glass and a schematic view of an indium bump on a pixel detector for comparison. The dark circle in the center is the UBM. The indium bump, which is a cylindrical solid shell, appears as a light ring adhered to the glass. In these modules, the glass was coated with ITO (Indium Tin Oxide). The image we observed is complicated because of multiple reflections amongst the different layers. We observed the indium on some of the bumps deformed during thermal cycling. Fig. 2 shows two such bumps before and after the thermal cycles. In one bump deformation progressed from one cycle to another. Table I lists the count of deformed bumps before and after each cycle. About 1% of the bumps had this deformation before any thermal cycling. An additional 0.5% was deformed during thermal cycling. We have no easy means of checking whether these bumps remain intact. Nevertheless, this deformation of the bumps might cause a change in the bump resistance and in the capacitance of the corresponding electronics channel resulting in a noisy readout. We did not observe on one module that was glued to the TPG any shift of the glass chips or any effect due to thermal cycling.

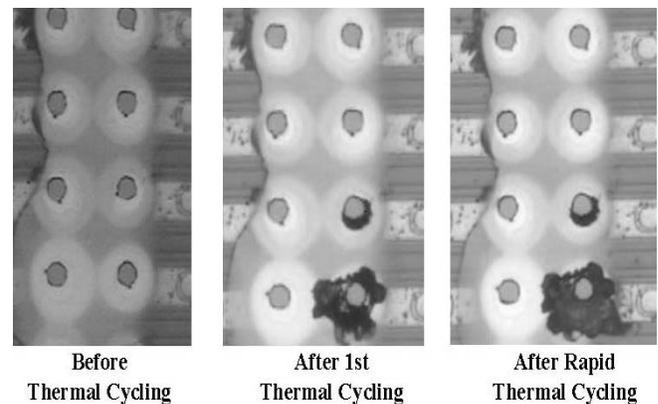


Fig. 2: Deformation at indium bumps.

TABLE I COUNT OF DEFORMED INDIUM BUMPS

	Existed Before T-Cycling	Created During 1 <sup>st</sup> T-Cycling	Created During Rapid T-Cycling
AIT_1	225 (0.96%)	23(0.10%)	95(0.41%)
AIT_2	255 (1.09%)	28(0.12%)	69(0.29%)

### B. MCNC Modules with Solder Bumps

Fig. 3 shows a group of solder bumps seen through the glass from the bottom and a schematic view of a solder bump on an actual detector for comparison. The manufacturer used the chemical product BCB mentioned earlier for plating and it remained over the UBM. The UBM and the BCB cover the center and the walls of the via and extends over the flat passivation layer. At the center of the via, the light is reflected up, but not on the walls of the via. This forms the bright circle in the middle and the first dark ring. The light is reflected on the flat part of the UBM again, forming the bright ring. The last dark ring is the solder bump, which is a cylindrical shell.

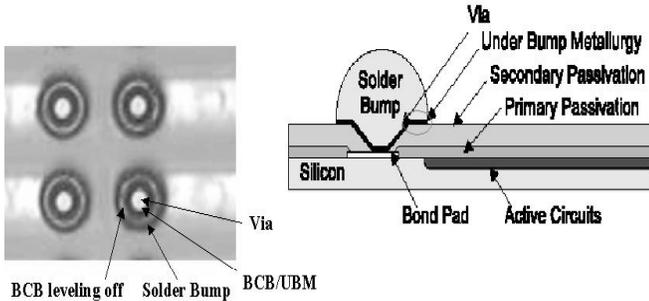


Fig. 3: Solder bumps under glass and a schematic view of a bump on a real detector.

We observed in some of these bumps that the first dark ring changed color to blend into the bright circle at the center. Fig. 4 illustrates this color blending. It occurred on ~2% of the bumps as received, mostly on the chip edges. The new occurrences appeared with the second thermal cycling and the irradiation processes. One disappeared during the rapid thermal cycling. Table II shows the counts of new occurrences after each step. We have no good explanation about the differences in the results amongst the three modules other than fluctuation in the processing and handling afterwards.

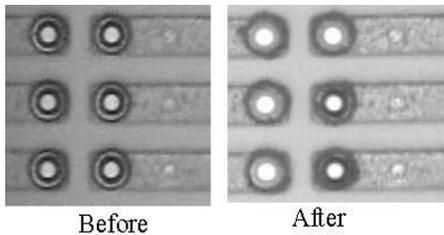


Fig. 4: Color blending of first dark ring.

TABLE II COUNT OF NEW OCCURRENCES OF FIRST RING COLOR BLENDING

MCNC Module	After 1 <sup>st</sup> Cycling	After Radiation	After 2 <sup>nd</sup> Cycling	After 3 <sup>rd</sup> Cycling	After Rapid Cycling
2	0	124	N/A	0	7
3	0	N/A	93	16	99
4	0	N/A	0	3	-1

A possible explanation to this observed change is as follows: the BCB is lifting off on the walls of the via (because of change in temperature) and partially reflecting the light causing the color blending. In one case, the BCB shrinks back to re-create the dark ring. This phenomenon, occurring on the electrically insensitive part of the bump, should not cause any problem to the electrical characteristics of the bump.

The other phenomenon that we observed in some of the bumps is the development of dark extrusions shown in Fig. 5. These also began to appear during the second thermal cycling and after the irradiation processes, at a rate of ~ 0.2% per module. They seem to be on the surface (glass side) and mostly on the edge bumps of the chips. The vendor suggested they might be due to ionic contamination (BCB originated), not completely removed during final cleaning. Since they appear to be surrounding the bumps, not in between the bumps and the glass, they would have no effect on the electrical behavior of the bumps.

We are still investigating with the vendors the causes of the observed changes. While the bonds seem to remain intact despite these changes, we will do a pull test to study these bumps. By inspecting the pulled parts optically, we can get an idea as to whether the electrical performance will be affected by the deformed pumps. We did not observe on these modules any shift of the glass chips due to thermal cycling or any effect after gluing to the TPG.

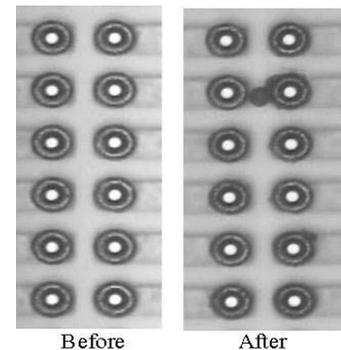


Fig. 5: Extrusion developing at the solder bumps.

### III. SINGLE CHIP HYBRID

We studied the temperature dependence of the operation al characteristics of the pixel detector at temperatures below and above room temperatures. For this study, we used an earlier

version of the pixel readout chip developed at Fermilab (FPIX1) [4]. The motivation for this test is that the pixel module will be subjected to temperature variations in the range of  $-10^{\circ}\text{C}$  to  $50^{\circ}\text{C}$  during its operational life.

Two different detectors were tested in a thermal cycle. The first one was assembled on a HDI flex circuit [5] that provide power and data connections to the readout chip and had a p-stop sensor from SINTEF (Oslo, Norway) [6] mated to an FPIX1 chip by indium bumps. A schematic view of the assembly is shown in Fig. 6. In this assembly, the flex circuit is sitting over the sensor without touching it, and is supported by two mechanical supports. The sensor is bump bonded to the readout chip and the bump bonds are the only support of the sensor. The readout chip is wire bonded to the flex circuit. A PCB (printed circuit board) with thermal vias is used to give mechanical support to the assembly and a Peltier device (thermoelectric cooler) is attached to the PCB board to control the assembly temperature. The sensor has the HV connection glued with conductive epoxy to the flex circuit HV pad. The flex circuit has a connector that is used as interface for data and power.

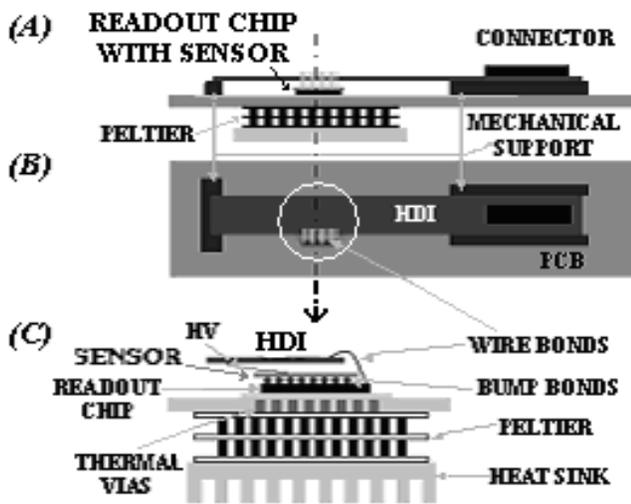


Fig. 6: Schematic view of the detector assembly using a HDI (setup I). (A) side view, (B) top view and (C) cut view of the assembly.

The second detector uses solder bumps and was assembled on a PCB that provides power and data connections to the readout chip. This setup is shown in Fig. 7. To vary the temperature, we used a Peltier device on the bottom of the PCB. A LabView program controlled the temperature settings and duration of the runs automatically.

The main goal of this thermal cycle test was to verify the effect of temperature changes on the bump-bond connections as well as on the noise and the threshold characteristics of the readout chips. To measure these characteristics, a charge-injection test was performed. In this test, a known test charge pulse was injected in to the front-end and from the response of

the chip, the threshold and noise of the detector could be extracted. It is important to note that all threshold measurements showed in this paper are relative measurements. This means that instead of doing an absolute calibration with an x-ray source to determine the value of the calibration capacitor, we just took the theoretical value of 6fF from the circuit simulation.

The first test to be performed was a fast thermal cycle with both the indium bump and the solder bump detectors. This thermal cycle was performed in the temperature range from  $5^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  on setup 1. The total duration of this thermal cycle was 120 minutes and it was composed of two steps. The first step took 60 minutes and the temperature was changed from  $5^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  with temperature rising at a rate of approximately  $1^{\circ}\text{C}$  per minute.

In the second step, the temperature was changed from  $70^{\circ}\text{C}$  to  $5^{\circ}\text{C}$  with a fall rate of around  $1^{\circ}\text{C}$  per minute. The relative humidity during this test was controlled and kept at 15%. In the first test, we measured the number of pixels responding to a given charge injection before and after the thermal cycle.

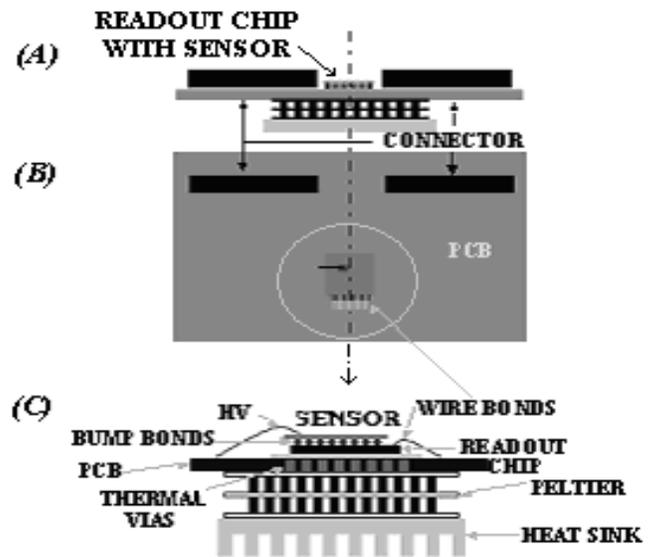


Fig. 7: Schematic view of the detector assembly using a PCB (setup II). (A) side view, (B) top view and (C) cut view of the assembly.

In Fig. 8, we show the result of the charge-injection test for both the indium and solder-bumped detectors. It can be seen that the threshold and noise of the detectors do not change significantly with thermal cycling. This is a good indication that the bump-bonds did not suffer from thermal cycling effects.

The second test performed was a hit map of the detector using a beta gun ( $^{90}\text{Sr}$ ) radioactive source. All hit map tests had duration of 5 minutes. The beta gun was pointed orthogonal to the detector at the distance of 10 cm and directed to the center of the detector.

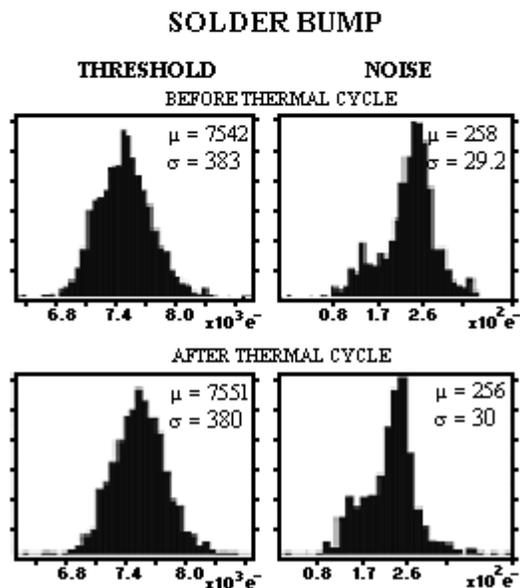
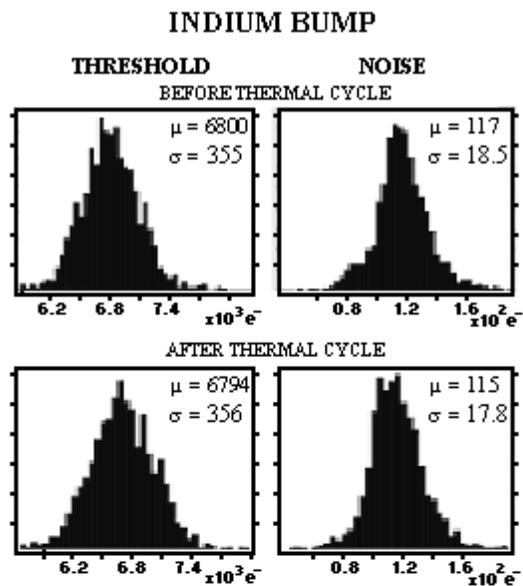


Fig. 8: Indium bump-bond and solder-bump bond after and before thermal cycle.

In Fig. 9, we show the hit map for the indium-bump detector before and after the test. In Fig. 10 we show the same for the solder-bump detector. There are some cells that do not respond to the beta gun exposition due to either problem in the bump-bonds (white cells), or due to problem on the sensor.

The different gray scales in the remaining cells indicate different number of hits. This is caused by the fact that each cells has its own threshold and that the illumination by the source is not homogeneous.

The hit map test showed that the number of cells responding before the thermal cycle is the same as after,

reinforcing the assertion that we are not losing bump bonds due to the thermal cycle.

Both detectors were also submitted to a long thermal cycle (LTC). The LTC had a total duration of 1080 minutes. The results of the long thermal cycle can be seen in Table III and Table IV. To avoid the lower edge of the readout chip, we analyzed only 900 cells from column 1 to 15 and from row 1 to 60.

Listed in the tables are the number of working, not responding, and noisy channels before and after LTC. Again we had a good performance form both types of the detectors and the small variations detected are within the statistical variation expected.

From these data, we conclude that the detector with indium bumps shows no noticeable difference from the solder bumps detector regarding possible bonds degradation at a thermal cycle. Both detectors seem to maintain their integrity during the short and the long thermal cycles.

#### IV. ELECTRICAL PERFORMANCE

While we have demonstrated that the connectivity of the bumps do not suffer from thermal cycling effects, there could be permanent changes in the noise and threshold performance of the readout chip as a function of temperature. We have done tests to study these possible variations.

These tests were performed for three different devices: the first one was a p-stop SINTEF sensor bump-bonded with indium to a FPIX1 readout chip, the second one was a p-stop SINTEF sensor bump-bonded with solder bumps to a FPIX1 readout chip, and the third one was a bare die FPIX readout chip.

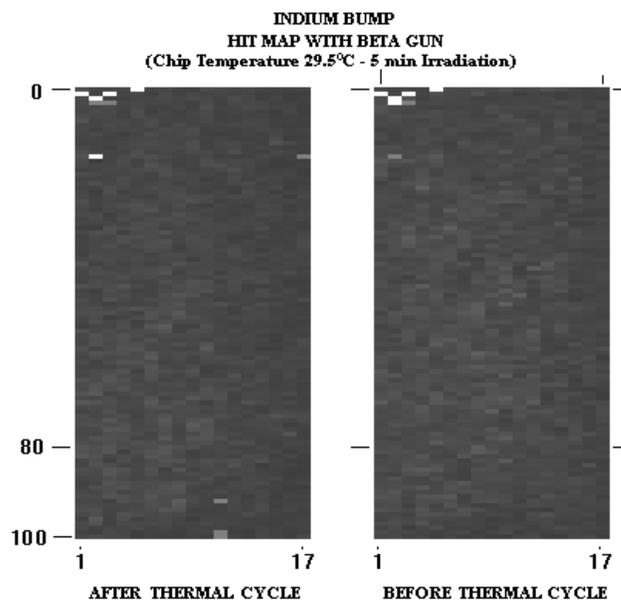


Fig. 9: Hit map of the indium-bump detector after and before the thermal cycle (using beta gun source).

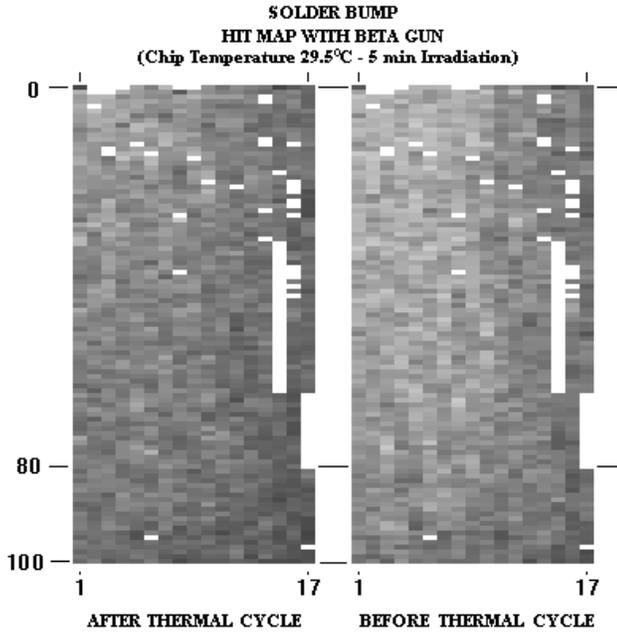


Fig. 10: Hit map of the solder-bump detector after and before the thermal cycle (using beta gun source).

TABLE III INDIUM BUMP TEST (BETA GUN)

Before LTC	At 7°C	At 42°C
Working	868	865
Not responding	29	29
Very noisy	3	6
After LTC	At 7°C	At 69°C
Working	865	865
Not responding	30	27
Very noisy	5	8

TABLE IV SOLDER BUMP TEST (BETA GUN)

Before LTC	At 7°C	At 42°C
Working	887	879
Not responding	9	9
Very noisy	4	12
After LTC	At 7°C	At 42°C
Working	886	880
Not responding	9	7
Very noisy	5	13

This test was performed by injecting charge to all cells on the chip using a pulse generator. The pulses inject started at 0.20V (corresponds to 2250 electrons) and was ramped up to 1.00V (~11250 e<sup>-</sup>). A complete scan of the chip was done. The threshold of the comparator was set to 2.00V (around 5500 electrons) and the sensors were biased at -200V.

From Fig. 11, we can see that the threshold rises with temperature, and it is similar on all three devices under test. It

is important to note that in the range from 5°C to -5°C (roughly the planned operating range for the detector in the experiment), the threshold is constant for the bare chip. It starts to rise only after 5°C. We have checked and verified that for the detectors the threshold mean is also constant in the same temperature range.

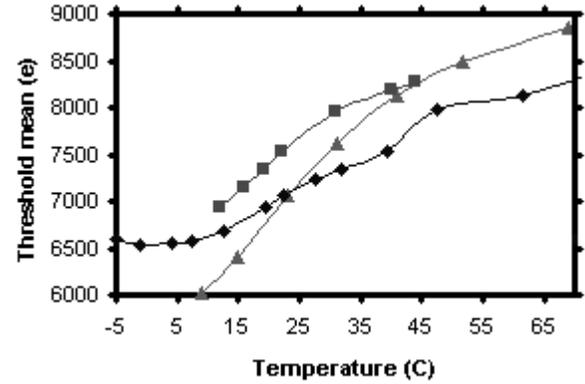


Fig. 11: Threshold mean versus temperature (°C). Diamond is the bare die chip, triangle is the indium bump detector and square the solder bump detector.

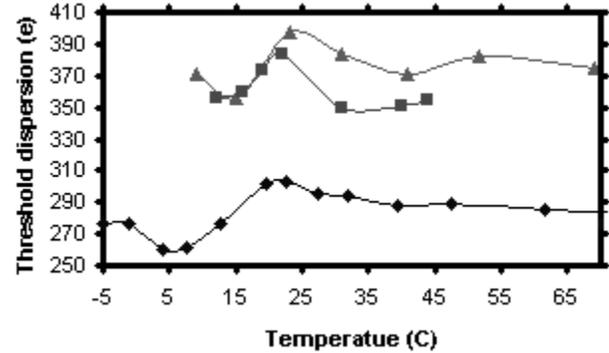


Fig. 12: Threshold dispersion versus temperature (°C). Diamond is the bare die chip, triangle is the indium bump detector and square the solder bump detector.

We can extract the threshold dispersion from the charge injection scan performed. As can be seen in Fig. 12, the threshold dispersion for the bonded detectors is about 100 electrons higher than for the bare die. For all devices, the threshold dispersion rises at first with temperature up to about 20°C, then falls and becomes rather stable from 40°C on.

Fig. 13 shows the noise mean as a function of temperature. It is similar to the threshold dispersion behavior; again the noise mean is pretty stable when the temperature is below 5°C, rises to a peak at 20°C before coming down and settling to a stable value after 40°C. The bare die has a noise mean of approximately 100 electrons less than the bonded detectors.

The last analysis that was done was on noise dispersion and the results of this analysis can be seen in Fig. 14. The average difference between the noise dispersion for the bonded detectors and for the bare die readout chip is around 20 electrons.

In all analysis done we did not observe in the detector noise and threshold characteristics significant variations before

and after a thermal cycle, meaning that the detectors did not suffer a significant degradation.

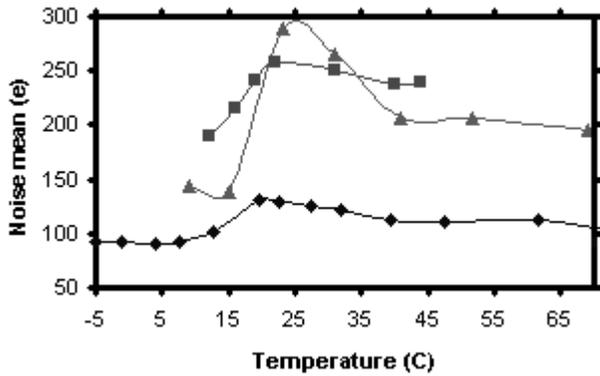


Fig. 13: Noise mean versus temperature (°C). Diamond is the bare die chip, triangle is the indium bump detector and square the solder bump detector.

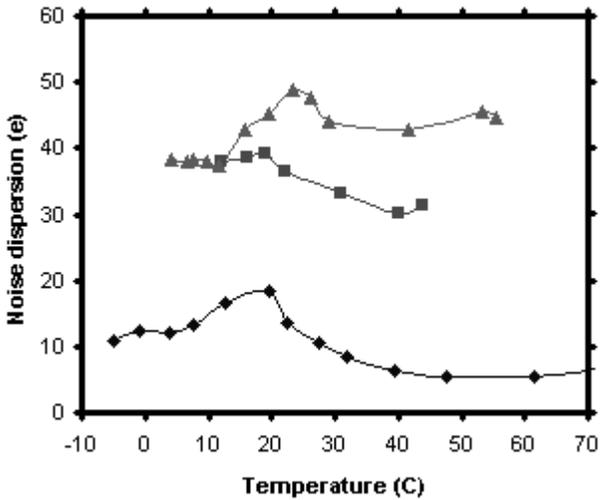


Fig. 14: Noise dispersion versus temperature (°C). Diamond is the bare die chip, triangle is the indium bump detector and square the solder bump detector.

We can also conclude from figures 11, 12, 13, and 14 that there are clear differences in noise and threshold performance of a bare die readout chip and a bump bonded one. This difference can be used to detect if we are having problems with the bump bonds after a process like a thermal cycle.

## V CONCLUSION

The bump bonding technologies with indium and solder are both viable for pixel detectors. The indium bumps look somewhat more susceptible to temperature variations. We visually observed the deformation of these bumps at cold temperatures. The solder bumps on the other hand, were not affected by temperature changes or by radiation. The visual changes we observed on the solder bumps are superficial in origin and are not expected to cause any operational problems. The CTE mismatch between the TPG and silicon seems to have no effect on the structural integrity of the bump bonds of either kind. No degradation in the noise or threshold performance due to thermal cycling was observed. Both bump bonds had roughly the same noise and threshold performance. There was no loss in bump bond connections during thermal cycles in the chips tested. This work shows that the pixel module suffers no performance degradation due to thermal cycling.

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