

THE RUN IIB UPGRADE OF THE CDF SILICON DETECTORS

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A substantial portion of the RunIIa silicon detectors of the CDF experiment will not perform adequately for the duration of Run IIB (15 fb^{-1}) because of radiation damage. The Silicon Vertex Detector (SVX-II) and Layer 00 will be fully replaced at the end of Run IIa. The Run IIB silicon tracker has a baseline design that safely achieves the required radiation tolerance by using single sided sensors that are actively cooled. The new Run IIB castellated layout contains more silicon surface area and has a more uniform radial distribution. It minimizes the number of hybrid and sensor varieties providing quick construction and assembly. The total mass in the tracking volume is reduced by eliminating unnecessary the passive material from the CDF volume.

1 Introduction

A successful Run II *engineering run* in 2000 established the 36×36 bunch $p\bar{p}$ operation at a center-of-mass energy of 1.96 TeV at the Fermilab Tevatron and produced $(58 \pm 17) \text{ nb}^{-1}$ of integrated luminosity for the comissioning of the CDF detector. Run II officially began in March 2001, and luminosity is currently being delivered to both the CDF and $D\bar{0}$ experiments which have started to carry out their ambitious physics programs ¹.

Run II is divided into two distinct stages: Run IIa will collide proton on antiproton bunches with a bunch spacing of 396 ns switching to 132 ns bunch spacing at $2 \cdot 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ of instantaneous luminosity, and Run IIb will maintain the bunch spacing at 132 ns. The number of superimposed interactions per beam crossing ^a must be kept low enough to allow a comprehensive event reconstruction by the collider detectors.

The latest prospects of the Run IIa luminosity levels are an integrated luminosity of 2 fb^{-1} and a peak value in the instantaneous luminosity of $2 \cdot 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$.

The transition from Run IIa to IIb in the begining of 2005 will require a shutdown of approximately 6 months, primarily to replace the radiation dam-

^aThis magnitude obeys a Poisson distribution whose mean is a linear function of the instantaneous luminosity with a positive slope dependent on the number of bunches in the proton and \bar{p} beam

aged components of the silicon detectors of the CDF and DØ^b experiments.

The goal for the three year Run IIb period (2005-2007) together with Run IIa is to accumulate 15 fb^{-1} by increasing the instantaneous luminosity to $5 \cdot 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$. One of the major efforts is focussed on increasing the number of antiprotons per bunch in the collider by a factor of 2-3 over the Run IIa value of $3.0 \cdot 10^{10}$ in 2 to 3 years without a major interruption to the Run IIa program. The upgrades in the accelerator system for \bar{p} production, collection, handling and accumulation are well described elsewhere³.

1.1 Radiation damage in the RunIIa silicon systems

The capabilities of the CDF experiment for the total integrated luminosity expected in Run II are limited by the radiation damage to the Run IIa silicon tracker^c, which is estimated to survive to approximately 5 fb^{-1} . This radiation damage will affect both the silicon sensors and the readout electronics.

The silicon sensors of the Run IIa silicon tracker will suffer a deterioration in performance primarily due to radiation damage to the bulk silicon, through displacements of silicon or impurity atoms from their lattice sites. One effect is an increase in the leakage current that degrades the ratio of signal to noise. A second effect is a change in the dopant concentration of the silicon which leads to an increase in the depletion voltage.

The SVX-II sensors are double sided and must be operated fully depleted, otherwise the strips on the ohmic side would remain effectively shorted together. These sensors are inherently limited in the bias voltage that they can sustain: the electronics on both sides of the sensors are referenced to a common ground and the applied bias voltage must be held off by coupling capacitors that can withstand ~ 100 volts. The increased depletion voltage will be the dominant mechanism leading to the demise of the SVX-II layers with double sided sensors that combine axial and small angle stereo manufactured by Micron (layers 2 and 4). The same mechanism will be dominant in the case of the single sided Layer 00 sensors. The SVX-II layers with double sided axial and 90° stereo sensors manufactured by Hamamatsu (layers 0, 1 and 3) will die as a result of the combination of both bulk damage effects.

The integrated luminosities that can not be exceeded in order to maintain reasonable detector performance were evaluated for the different components of the Run IIa silicon tracker⁵. These limits were under 15 fb^{-1} for Layer 00 and Layers 0,1,2, and 4 of the SVX-II. Other SVX-II components like

^bSee² for a complete description of the Run IIb upgrade of the DØ silicon tracker.

^cSee reference⁴ for a complete description of the RunIIa silicon tracker of the CDF experiment.

the Port-Cards ^{6,4,7}, that generate the control signals for the SVX3 readout chip, and the electronic components of the DOIMS (Dense Optical Interface Modules) connecting the Port-Cards with the front end electronics, are not expected to survive 5 fb^{-1} .

All the layers of the ISL (Intermediate Silicon Layers) ⁴ will survive Run I Ib and will not need to be replaced. For mechanical reasons and the tight schedule for this upgrade programme a full replacement scenario of the SVX-II and Layer 00 systems was approved.

2 The baseline design for the Run I Ib replacement detector.

2.1 Comparison of the Run I Ia and Run I Ib silicon systems.

The baseline design of the replacement detector ^{8,9} has been developed to accomplish several goals.

In order to achieve the required radiation tolerance, single-sided high-bias-voltage sensors will be used instead of the double sided sensors used in SVX-II detector. Therefore to retain or improve the tracking capabilities of the Run I Ia silicon tracker at least twice as many sensors as in the current Run I Ia detector will be needed. The current SVX3 chip will be replaced by a new rad-hard SVX4 chip.

The new Run I Ib castellated layout (see figure 1) takes advantage of the entire volume between the beam pipe and the ISL space frame from 2 to 18.5 cm in radius. There is more silicon detector area given that the outer instrumented layers are located at larger radii in the Run I Ib design (see table 1). The mass distribution is better because the radial gap in the Run I Ia detector between the ISL and the SVX-II which was occupied by passive material such as cables and Port-Cards (see section 2.3), has been eliminated.

The wedge structure of the Run I Ia detector, that maintained the same 12-fold ϕ segmentation for all the layers, is abandoned in Run I Ib in favour of minimizing the number of hybrid and sensor varieties. This is required for the quick construction and assembly, and reduces the overall cost. Layers 2 through 6 (90% of the detector) have a uniform stave design and only 3 sensor types while SVX-II had 5 sensor types. There will be only 4 types of hybrids while SVX-II and Layer 00 have 12 hybrid types. The layers 0 and 1 together have 2 types of sensors, in comparison with the 2 types of sensors for Layer 00 alone in Run I Ia.

All the layers will use intermediate strips between the readout strips allowing smaller pitch and better hit resolution while keeping the channel count low. The total increase in the number of sensors from I Ia to I Ib is $\sim 250\%$

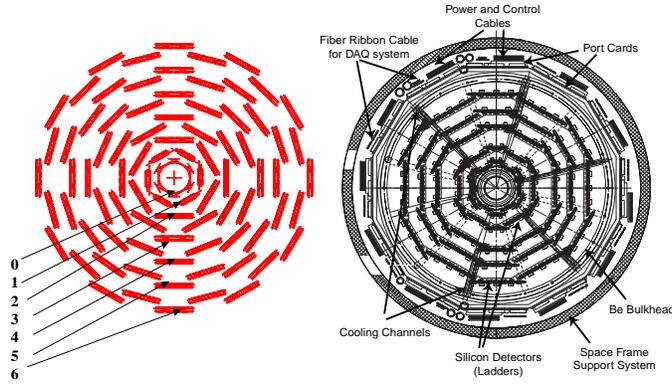


Figure 1. Run IIb silicon tracker r - ϕ inner layout versus end view of SVX-II detector at the same scale. ISL detector is not included.

Table 1. The Run IIb silicon tracker baseline design in comparison with the Run IIa SVX-II and Layer 00 detectors.

IIb Layer	IIb axial R(cm)	IIb stereo R(cm)	IIb ϕ segm.	IIa Layer	IIa R(cm)	IIa ϕ segm.
L0 inner	1.95		12	L00a	1.3	12
L0 outer	2.35		12	L00b	1.85	12
L1	3.35	3.00 (90 ⁰)	6	L0a	2.45 (90 ⁰)	12
L2	4.55	4.90 (90 ⁰)	6	L0b	2.99 (90 ⁰)	12
L3 inner	6.45	6.10 (90 ⁰)	12	L1a	4.12 (90 ⁰)	12
L3 outer	7.70	7.35 (90 ⁰)	12	L1b	4.57 (90 ⁰)	12
L4 inner	9.50	9.15 (2.5 ⁰)	16	L2a	6.52 (1.2 ⁰)	12
L4 outer	10.6	10.25 (2.5 ⁰)	16	L2b	7.02 (1.2 ⁰)	12
L5 inner	12.5	12.15 (2.5 ⁰)	20	L3a	8.22 (90 ⁰)	12
L5 outer	13.6	13.25 (2.5 ⁰)	20	L3b	8.72 (90 ⁰)	12
L6 inner	15.5	15.15 (90 ⁰)	24	L4a	10.09 (1.2 ⁰)	12
L6 outer	16.6	16.25 (90 ⁰)	24	L4b	10.64 (1.2 ⁰)	12

while the increase in the number of chips and readout channels increases by only $\sim 24\%$.

2.2 The silicon detectors

The silicon sensors for the Run IIb detector have been chosen with regard to the existing and tested radiation hard technologies needed for the LHC: single sided sensors designed to be operated with high bias voltages to cover an increase in the depletion voltage due to bulk damage in the silicon. The sensors will be actively cooled to be operated at a lower temperature in order to survive higher radiation doses. The single sided sensors are also easier to manufacture, test and handle, avoiding problems during the detector construction.

For the innermost layer the sensors will be identical to the Layer 00 sensors. For all the outer axial layers and outer 90° stereo layers the strip(readout) pitch is 44(88) μm . The outer 2.5° stereo layers has a strip(readout) pitch of 45.75(91.5) μm . The axial layers 0 and 1 have a strip(readout) pitch of 25(50) μm . The 90° stereo layer 1 sensors have a strip(readout) pitch of 47.5(95) μm . The 90° stereo sensors use well established “double metal” technology¹⁰ to simplify readout by providing axial readout strips orthogonal to the implants. Consequently the level of noise will be higher in the 90° sensors, but still within the 40 pF limit for good performance with the SVX4 chip.

2.3 The data acquisition system.

The stave is the basic structural unit of layers 1-6. The 156 staves of the outer 5 layers use a uniform design. Each stave is 60 cm long and it is supported at $z=0$ and ± 60 cm. The z segmentation of a given layer consists of two staves, 6 readout modules and 12 silicon sensors. The stave for layer 1 is similar in concept to the stave of the outer 5 layers but both narrower and shorter. Each stave has built-in electrical bus cables and cooling tubes which are sandwiched between six axial sensors in the upper face and six stereo sensors in the bottom face. The electrical bus is a copper-kapton flex cable which is laminated to the carbon fiber surfaces of the stave. The sensors are glued on top of the cable.

The core of the stave is fabricated of carbon fiber and rohacell, with integrated 2×6 mm PEEK cooling tubes to cool the sensors, the hybrids and the Mini Port-Card. The polyetheretherketone plastic (PEEK) was selected for radiation hardness and mechanical stability.

A readout module is made up of two sensors wirebonded together and a readout hybrid, circuit board holding the SVX4 readout chips and related components.

The hybrids are glued onto the silicon surface at one end of the silicon

sensor in all layers except the innermost (see section 2.4). Four-chip hybrids are used for the outer 5 layers, three-chip hybrids for layer 1 and two-chip hybrids for layer 0. They are wirebonded to the bus cables to provide a connection to the cables coming from the Mini Port-Card.

The SVX4 readout chip integrates and digitizes the silicon signals and replaces the SVX3 chip used in the Run IIa silicon detector. It will provide a lower noise and faster rise-time amplification, which allows for larger detector capacitances. It uses standard $0.25 \mu m$ deep sub-micron technology, which is very tolerant to high radiation. The signal-to-noise ratio is expected to be 30% better. Some radiation tests in progress suggest this chip will survive more than 30 fb^{-1} .

The Mini Port-Card (MPC) is a simplified version of the Run IIa Port-Card (PC) ^d that uses five Run IIa transceiver chips to regenerate the control signals for the SVX4 chips, but eliminates the complication of optical readout. The MPC will be glued to the end of a stave and electrically connected to the end of the stave bus with wire bonds. The rest of the components of the Run IIa PC not present in the Run IIb MPC have been moved to the new Junction Port-Card (JPC) ^e in order to reduce the mass and the required cooling. The JPC will be moved outside the tracking volume to the face of the central calorimeter location where the cooling required by the active components is available.

2.4 The innermost layer.

The layer 0 configuration is axially 12-fold symmetric. The carbon fiber support structure with integrated cooling tubes will be mounted on the beampipe to support the silicon. A readout module in layer 0 consists of 2 sensors glued and bonded together. All Run IIb layer 0 sensors are 2 chips wide while Layer 00 has alternating 1 and 2 chip wide sensors. There is only one type of sensor and hybrid which are almost identical to the Layer 00 ¹¹ two-chip hybrids. Lightweight cables connect the sensors to the hybrids which are located outside the tracking region ($|z| > 50\text{cm}$) avoiding the problem of fitting hybrids on narrow inner sensors and reducing significantly the material and cooling requirements. The use of these cables causes a degradation in the signal to noise ratio by the noise pickup and a higher readout capacitance, and thus they are only used on layer 0.

^dSee reference ^{6,7} for more details about the Run IIa Port-Card.

^eSee ⁸ for more details about the Run IIb Junction-Port-Card.

3 Conclusions.

The CDF Run IIb silicon tracker, which will replace the Run IIa detector because of radiation damage, has a baseline design which is comparable in performance and has many structural advantages. We have discussed this basic design and the components from which it will be built. The design includes 90° layers for precision tracking in 3 dimensions. We look forward to the physics this device will provide in Run IIb.

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