



The effect of dead-timeless silicon strip readout at CDF II^{*}

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Abstract

The Run IIa CDF Silicon Upgrade has recently finished installation. The detector uses revision D of the SVX3 readout IC. This final revision incorporated new features in order to improve the potential of dead-timeless operation. This paper describes measurements of dead-timeless effects on silicon strip readout on the test bench. This paper also describes tests of the dynamic pedestal subtraction circuitry, which is shown to improve greatly the dead-timeless performance of the silicon systems.

Key words: SVX3D, silicon strip, dead-timeless, pedestal subtraction

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1 Introduction

The Collider Detector at Fermilab (CDF) [1] has finished a significant upgrade and has begun a new data run March 2001. The goal of dead-timeless data acquisition with the new upgrade along with the higher trigger rates has led to the design architecture of the SVX3D IC [2,3]. The SVX3D is a mixed signal integrated circuit which instruments the 722,432 channels of the CDF Run IIa silicon upgrade. The SVX3D contains 128 parallel charge sensitive

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preamplifiers with an analog pipeline, a Wilkinson ADC, and 9 differential data drivers in a single package. This paper focuses on the effects of dead-timeless operation on the silicon upgrades and circuitry used to improve its dead-timeless performance.

2 Dead-timeless Operation

Dead-timeless operation refers to the continuous analog acquisition of data, while previously acquired data is being digitized or transmitted (readout). Digital switching can couple to analog circuitry in a mixed signal IC. Normally, digital switching can be fixed in phase relative to the analog acquisition, leading to constant pedestal offsets. In dead-timeless operation though, such synchronization is not possible, as the digital switching controlling the digitization and transmission of data occur only when needed. In addition, the data transmitted has varying values which cannot be known in advance. In order to minimize the dead-timeless effects on the analog circuitry, one isolates the digital and analog functions of the system. The coupling can occur through the three media present: the SVX3D IC, the readout hybrid package, or through the silicon sensor. In [5], the efforts to isolate the digital and analog circuitry within the SVX3D IC and the readout hybrid package are described. The silicon sensors are sensitive antennae which can pick up fluctuating electromagnetic fields which are too weak to affect the IC directly. This sensitivity can couple digital signals directly to the analog pre-amplifier's inputs. Fortunately, this mechanism can be studied independently of the coupling within the integrated circuit or readout hybrid by connecting or not connecting the analog inputs of the IC to the silicon sensor.

In order to minimize readout times and data volume, only channels with signal (and their nearest neighbors) are readout. This sparsification is determined by a programmable fixed threshold for each chip. This single threshold places a premium on pedestal stability of the system, as fluctuation in the pedestal will lead to increased noise occupancy (on upward fluctuations) and decreased signal efficiency (on downward fluctuations).

The dead-timeless effects on the pedestal stability are measured using a 'pedestal map'. Two triggers are given, with the second trigger spaced a chosen number of integration cycles, in this paper denoted buckets, after the first trigger. The second trigger is used to probe the state of the chip while the first trigger's data is digitized or readout. By stepping the second trigger through the fixed pattern, a map of the chip's state as a function of the position in the digitization and readout cycles can be made. Each step was measured 40 times in order to discriminate between systematic pedestal variations and random noise.

3 Performance of Readout Hybrid Package

The pedestal stability of the SVX3D IC on the readout hybrid package was studied using a production Intermediate Silicon Layers (ISL) hybrid[4]. It consists of a double-sided aluminum nitride hybrid with 4 SVX3D chips on each side. The readout hybrid houses bypassing and filtering capacitors. Figure 1 shows the pedestal map for a chip on the hybrid; all chips have the same pedestal map. The first 21 buckets are in 'acquire' mode, where no digital operations are underway. During buckets 22-79, the dummy trigger's data is being digitized. Between buckets 80-102, the dummy trigger's data is readout. The pedestal is stable at the less than 1 ADC count level (≈ 650 electrons). The most-likely charge from a minimum-ionizing particle is approximately 33 ADC counts. With the precautions taken, the digital-to-analog coupling problem in the SVX3D and readout hybrid have been solved.

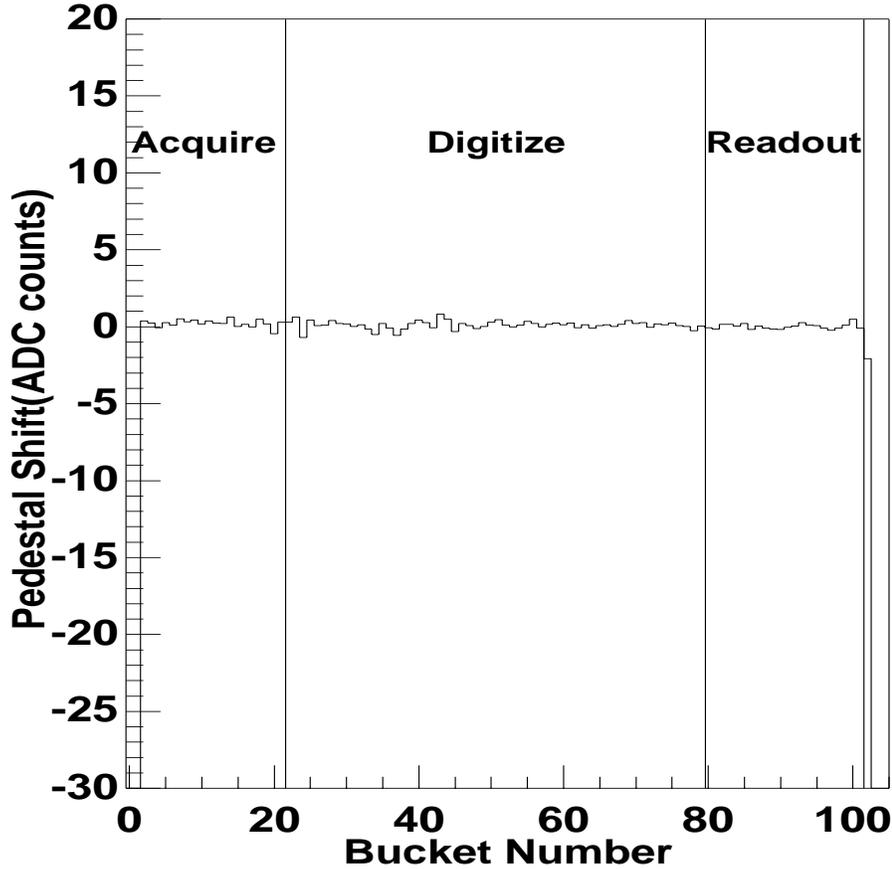


Fig. 1. Pedestal map for a SVX3D IC mounted on an ISL readout hybrid. The vertical axis is the shift of the pedestal relative to the reference bucket at 0. Each point of the pedestal map is the average of 20 samples over the 128 channels of the chip. The vertical scale is in ADC counts, which corresponds to approximately 650 electrons of input charge.

4 Performance of ISL Module

Environmental pickup through the silicon sensors was studied using an ISL module. The module consists of an ISL hybrid connected to 3 double-side silicon sensors held by a carbon fiber support structure. The module was supported in a grounded box with the module held more than 1.5 inches from any metal surface. The box effectively shielded the module from outside signals, allowing for a careful measurement of self-coupling of the module's silicon sensors to the readout hybrid.

Figure 2 shows the pedestal map of the ISL module. Clear pedestal shifts are seen during the digitization and readout cycles. Each of the 5V (CMOS) single-ended external command signals, which control chip state and pipeline logic, are one source of pedestal shifts. These signals occur in buckets 41, 45, 71, 73, 205, 209, and 213 (shown by dark gray arrows in figure 2). Differential 3V external command signal, which controls the Wilkinson ADC, also cause pedestal shifts. These signals occur in the buckets 45, 47, and 69 (indicated by the black arrows in the figure).

Two periods which do not correspond to external command signals were identified which have large pedestal shifts. Both corresponds to time periods of increased digital current drawn by the SVX3D IC. The first period occurs during the digitization cycle in bucket 51–62 in figure 2. The beginning of this period occurs when a comparator in the ADC changes state and ends when the sparsification of data finishes. The digital circuitry draws a varying digital current during this time period. The second period occurs within the readout cycle in buckets 71, 106, 138, and 171. These buckets corresponds to time period in which the individual chip's data drivers draw current in order to begin to output its data. Additional small level pedestal shifts (less than 1 ADC counts) are measured during the readout of data. These shifts are due to activity on the output data bus lines.

An estimate of the noise occupancy and additional signal inefficiency as a function of pedestal shift is shown in figure 3. These estimates assumes a sparsification threshold of 2.5 times the average single channel noise, which was the threshold used for two strip clusters in the original SVX detector [6]. The signal inefficiency was estimated using a parameterization based on clustering studies using a ^{106}Ru β source. Some pedestal shifts are large enough to cause a 50% noise occupancy or over 20% signal inefficiency in the given bucket. Most buckets are within 1 ADC count of the dummy trigger's data. On the bench, the dead-timeless performance of the ISL modules meets specifications. The actual geometry is much more complex and has the potential to have larger dead-timeless effects. The final dead-timeless performance can only be determined after the detector is fully commissioned.

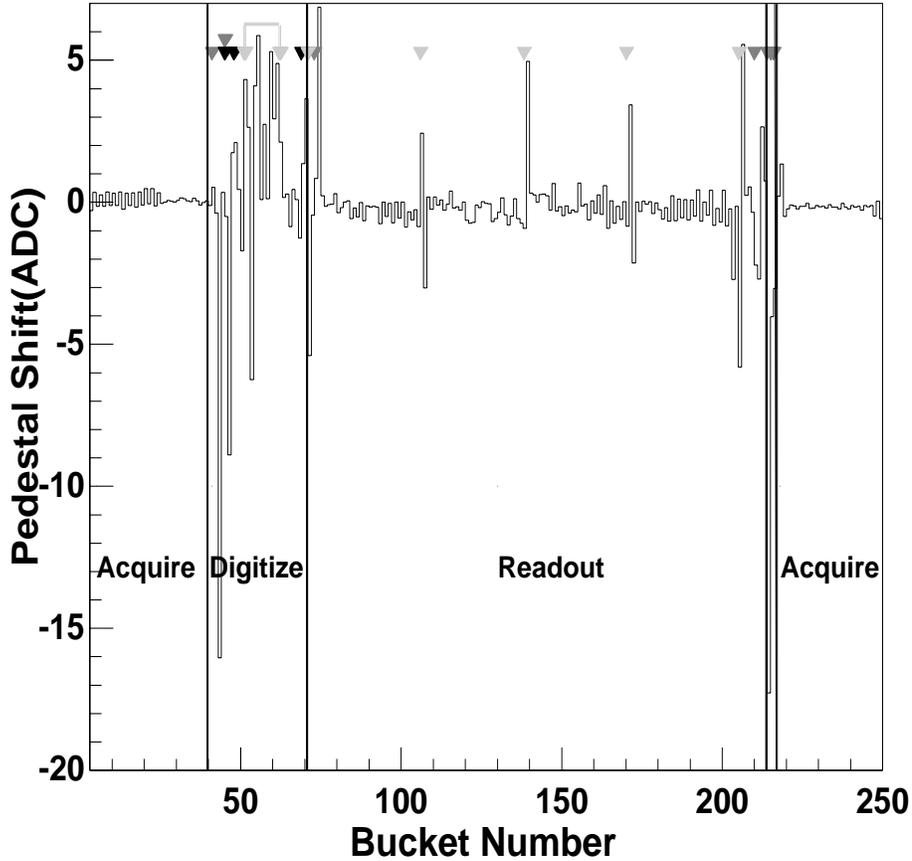


Fig. 2. Pedestal map for an ISL module. The vertical lines separate the various phases of dead-timeless operation. The light gray arrows indicate the periods of change of digital current consumption within the SVX3D IC. The dark gray arrows indicate timing of 5V AC command signals for chip state and pipeline control. The black arrows indicate timing of 3V AC differential command signals which control the Wilkinson ADC.

5 Dynamic Pedestal Subtraction

The safety margin for environmental pickup is improved greatly by the dynamic pedestal subtraction circuitry, described in detail in [5,7]. The circuitry determines the pedestal on an event-by-event basis for each chip and subtracts it from every channel. Thus channels without a hit will always read zero ADC counts as long as the pedestal is uniform within a chip. Since the zero of the ADC moves along with the pickup on a event-by-event basis, the DPS circuitry should remove all common-mode pedestal shifts due to dead-timeless operation. This assumes that the pickup is uniform over all channels in a given SVX3D chip. The effectiveness of the DPS circuitry was tested using the same ISL module with the DPS circuitry enabled (which is settable during initialization). Since channels at pedestal will be 'by definition' at zero ADC, the

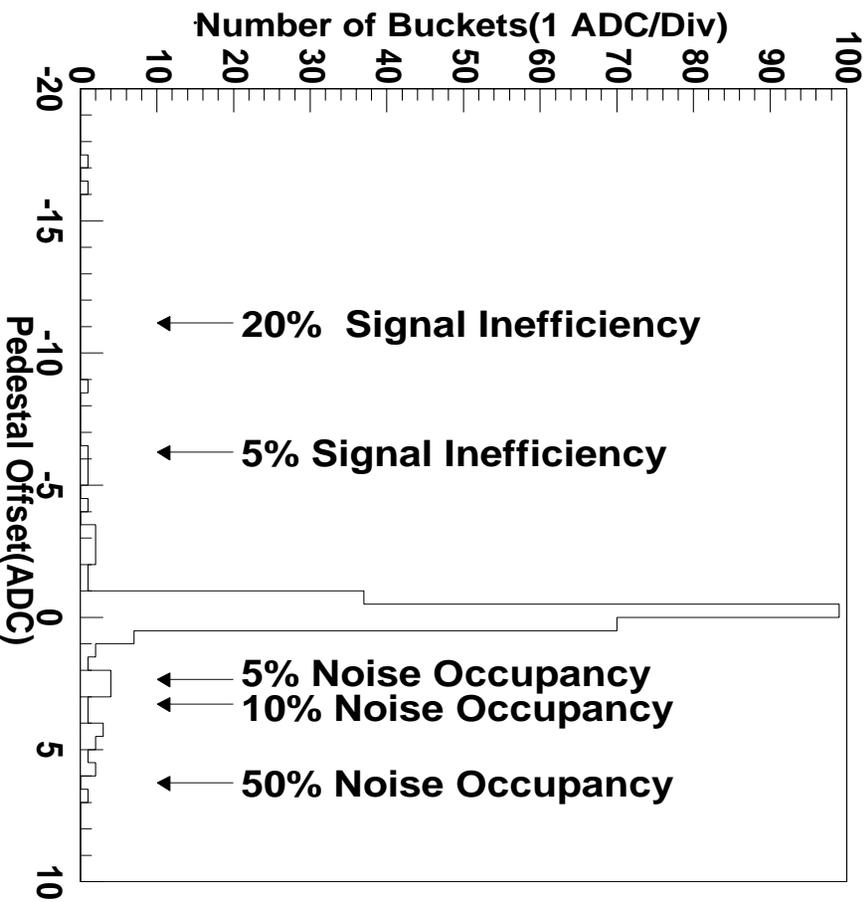


Fig. 3. Projection of figure 2 pedestal map for an ISL module. The arrows indicate the additional noise occupancy or signal inefficiency due to the pedestal shifts.

dead-timeless effects were measured on a channel where charge was injected into every bucket using the calibration circuitry. Figure 4 shows the pedestal map for the calibration charge injected channel using DPS. The pedestal shifts due to environmental effects are reduce to less than the 1 ADC count level using DPS, greatly improving the dead-timeless performance.

6 Conclusions

The SVXX3D IC, used in the CDF Run IIa silicon upgrades, is a mixed digital-analog device. The features added to the SVXX3D and readout hybrid design have effectively minimized the effects of dead-timeless acquisition. The pre-dominant effects of dead-timeless operation are environmental coupling of the digital and analog circuitry through the silicon sensor. The environmental pickup is caused by both the 5V single-ended and 3V differential command signal, as well as the internal changes of chip state that cause fluctuations in the current consumption of the digital circuitry. The SVXX3D's dynamic

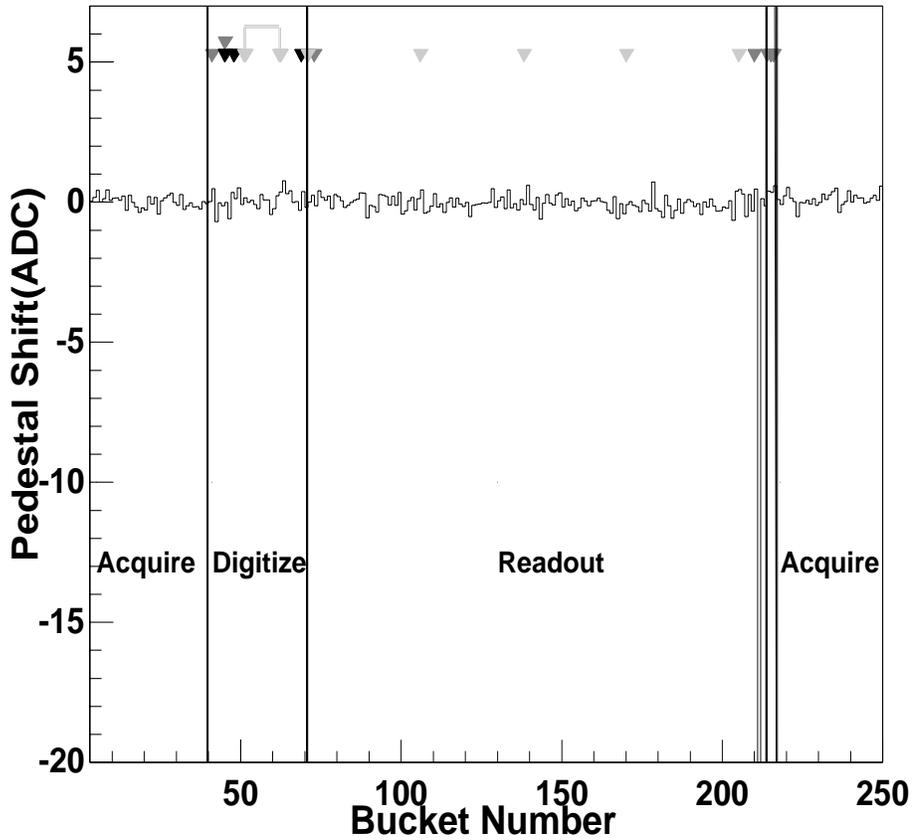


Fig. 4. Pedestal map for an ISL module with the dynamic pedestal subtraction(DPS) circuitry enabled. The solid line is for a channel with a constant calibration injection applied in every sample. With DPS enabled, channels without a laser pulse will be 'by definition' be at zero counts. Bucket 212 is empty due to a pipeline reset operation which invalidates the data. During collision data taking, this reset will only occur in periods of beam-gaps.

pedestal subtraction circuitry removes this environmental pickup, and thus meet the dead-timeless performance specifications for the silicon upgrade of CDF Run IIa.

Acknowledgements

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