



A Two-Level Fanout System for the CDF Silicon Vertex Tracker

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Abstract— The Fanout system is part of the Silicon Vertex Tracker, a new trigger processor designed to reconstruct charged particle trajectories at Level 2 of the CDF trigger, with a latency of 10 μ s and an event rate up to 100 kHz. The core of SVT is organized as 12 identical slices, which process in parallel the data from the 12 independent azimuthal wedges of the Silicon Vertex Detector (SVXII). Each SVT slice links the digitized pulse heights found within one SVXII wedge to the tracks reconstructed by the Level 1 fast track finder (XFT) in the corresponding 30° angular region of the Central Outer Tracker. Since the XFT tracks are transmitted to SVT as a single data stream, their distribution to the proper SVT slices requires dedicated fanout logic. The Fanout system has been implemented as a multi-board project running on a common 20 MHz clock. Track fanout is performed in two steps by one “Fanout A” and two “Fanout B” boards. The architecture, design, and implementation of this system are described.

I. INTRODUCTION

The main functional blocks of each Silicon Vertex Tracker slice are the Hit Finders, the Associative Memory system, the Hit Buffer and the Track Fitter [1] [2]. Every time an event is accepted by the Level 1 trigger, the digitized pulse heights in the Silicon Vertex Detector [3] are sent to the Hit Finders which calculate hit positions. The hits found by the Hit Finders and the raw tracks found in the Central Outer tracker by the Level 1 Fast Track finder [4] are then fed to both the Associative Memory system and to the Hit Buffer [5]. The Associative Memory system performs pattern recognition by selecting for further processing the combinations of XFT tracks and SVXII hits that represent good track candidates. This is done by comparing the input data with a stored set of patterns in a completely parallel way, using a dedicated custom VLSI chip (AM chip [6]). The AM system outputs a list of Roads. Each Road is defined as a combination of SuperStrips on five different detector layers that can be traversed by a single track. The SuperStrips used to define the Roads correspond to the hit positions on four silicon layers, while the fifth SuperStrip is a function of the track parameters reconstructed by the XFT (track curvature and azimuthal

angle measured at the sixth superlayer of the COT at 106 cm from the beamline). To reduce the amount of required memory this pattern recognition process is carried out at a coarser resolution than the full available resolution. The Roads found by the AM system are sent to the Hit Buffer, that retrieves the original full-resolution silicon hit coordinates and the XFT track associated to each Road and delivers them to the Track Fitter system for full-precision computation of track parameters.

The Fanout system has two main functions: performing the distribution of the XFT tracks to the proper SVT slices and mapping the two XFT track parameters to a single coordinate which is binned in SuperStrips and is used by the AM system. Simulation studies have shown that the most efficient use of the Associative Memory is obtained by using as SuperStrip the azimuthal angle of the XFT track extrapolated to a distance of about 10 cm from the beamline and a SuperStrip size of 25 mrad. For each XFT track received in input, the Fanout outputs a two word packet: the first word contains the SuperStrip number used by the AM system, while the second word is a copy of the input word and is used by the Track Fitter for the full-precision reconstruction of the track. For each event the Fanout receives also from the Global Level 1 trigger the information of which among the 64 CDF Level 1 triggers were fired. This information is summarized and output from the Fanout as two bits in the special word used within the SVT system to mark the end of each event and to record diagnostic information (End Event word).

II. ARCHITECTURE AND DATA FORMAT

The Fanout system is organized as a set of three (one of type “A” and two of type “B”) 9U \times 400 VME boards. Communication between the Fanout A and the two Fanout B boards takes place through a customized P3 backplane, with data flowing from A to B. All the input streams to the Fanout system are received by the A board through three connectors placed on its front panel. One stream carries the XFT tracks and two carry the L1 trigger decisions. Data to the rest of the SVT are output only from the Fanout B boards. Each Fanout B has 6 output connectors on the front panel and feeds 6 SVT slices.

Both the XFT data and the data output from the B boards conform to the standard SVT data format while L1 trigger data have a different format. SVT and XFT data occupy 25 bit words. In each word there are 21 data bits (the 21 least significant bits), an End Packet (EP), an End Event (EE), a Data Strobe (DS) and a Hold (HD) signal

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(Table I). The EP bit specifies if the same data packet occupies only one or more words. Its value is set to 1 for the XFT tracks since each packet (track) occupies one single word. The EE bit marks the end of data corresponding to one event. The Hold and Data Strobe are used for the communication protocol among boards. The DS signal is driven by the source board and indicates when the data become valid and can be latched by the destination board. The Hold signal is driven by the destination board. When the destination board does not keep up with the incoming data rate, the Hold signal is set active and the source responds by suspending the data flow, which is resumed as soon as the Hold goes out. This protocol is uniform among all the SVT boards. The word with the EE bit set to 1 is called End Event word (EE word), its data field contains no information related to tracks but it is used to keep track of possible errors occurred during data transmission or processing and to record global information on the event.

TABLE I
SVT DATA WORD FORMAT

24	23	22	21	20...0
HD	DS	EE	EP	Data field

The data field of the XFT word contains 12 bits specifying the azimuthal angle, 6 the curvature and 1 respectively the charge, the isolation and the pseudorapidity of the track. The data field in the End Event word contains the Event Tag (8 bits), the Parity (PA) of the event (1 bit), the Error Flags (8 bits), the L1 Trigger information (L1T) generated by the Fanout system (2 bits) and the Level 2 Buffer number (L2B) assigned to the event by the Trigger Supervisor (2 bits) [8]. The format of the End Event word data field is reported in Table II, where the additional EP, EE (both set to 1), DS and HD signals are omitted. The meaning of the information recorded in the End Event word relevant to the Fanout system will be discussed in Sec. II-A.1.

TABLE II
END EVENT DATA FIELD FORMAT

20...19	18...17	16...9	8	7...0
L2B	L1T	Error Flags	PA	Event Tag

Two streams from the Global Level 1 trigger carry the 64 Level 1 trigger decisions to the Fanout A board. This information is transmitted using one word per stream per event. The format of data is the same in both streams and uses a 33 bit data field with a DS signal to indicate when data become valid. No End Packet, End Event and Hold signal are present. The data field contains 32 trigger decisions (the 32 least significant bits) and 1 bit of the Level 2 Buffer number (Table 3). The combination of the two L2B bits from the two streams must match the L2B number recorded in the EE word of the XFT data.

TABLE III
GLOBAL LEVEL 1 TRIGGER WORD FORMAT

33	32	31...0
DS	L2B	L1 Trigger decisions

For each XFT track received in input, the Fanout system outputs a two word packet through the B boards to the proper SVT slices, depending on the azimuthal angle of the track. The first word of the packet is used by the AM system while the second one by the Track Fitter. The format of the two output words is the standard SVT data format. In the word used by the AM system only 15 out of the available 21 bits of the data field are actually used: 12 bits contain the SuperStrip number, 3 bits the Layer number (set to 5) associated to the XFT tracks. The remaining 6 bits of the data field are spare. The word used by the Track Fitter is a copy of the XFT input word. Since in this case one data packet is logically made of two words, the EP bit is set to 0 in the first word and to 1 in the second one. The end of the output event is marked by the EE word, which is sent simultaneously to all the SVT slices. All the 12 End Event words are identical except for the Parity bit which can change from stream to stream because different streams transmit different data sets (Sec. II-B).

A. Fanout A board

The Fanout A board performs the entire data handling within the Fanout system. It receives and processes all the input streams and constructs the output data packets as well as the output End Event word (Sec. II-A.1). The B boards perform simply the fanout function.

XFT tracks and L1 trigger bits are received asynchronously and are stored on three sets (1 for the XFT tracks and 2 for the L1 Trigger bits) of two $4K \times 18$ bit FiFos each. The set of FiFos receiving XFT tracks provides an Almost Full signal that is sent back to the source meaning Hold. If the Fanout A does not keep up with the incoming data rate, the FiFos become Almost Full and the Hold signal is asserted. The signal is active while the amount of unread data in the FiFos remains above the Almost Full threshold. Although this communication protocol is uniform among all the SVT modules, no handshake is implemented with the Global Level 1 trigger. This is allowed by the fact that the Level 1 trigger information is received at a much lower rate (one word per stream per event) than the XFT tracks.

The Fanout A board transmits data to the B board through a customized P3 backplane. The data stream contains one standard SVT format word (21 bit data field plus EP, EE, DS and HD bits), 12 “enable” bits, used by the B boards to select which SVT slices (one or more) must receive the word, and 2 clock lines routed on the backplane to have each B board receiving one line (Sec. IV). When the Data Strobe bit is active, the B boards receive one word for each clock cycle, validated at the positive edge. The Hold line is driven and is common to both the B boards. It is implemented as a wired-or chain. When the Hold line

is active, the Fanout A stops reading new data from the FiFos.

The SuperStrip number (12 bits) inserted in the word used by the AM system and the list of 12 enable bits associated to each XFT track are determined using a Look Up Table. The Look Up Table is implemented as a set of 6 (512K \times 8 bit) static RAMs where 20 bits summarizing the XFT track parameters are used as an address and the SuperStrip number and the list of enables are stored in each location. To obtain a 1M \times 24 bit Look Up table, the 6 memories are organized as two blocks of 3 units, with bit 20 of the XFT parameters actually used as a chip select to enable either the first or the second block of RAMs.

The 2 L1T bits are generated by the A board as a programmable combinatorial function of the 64 Level 1 Trigger decisions. The logic of the board is implemented on seven 240 pin FLEX10K20 FPGAs from ALTERA. The firmware is fully reconfigurable on board.

A.1 Error handling and data flow monitoring

There is a number of error conditions that can be detected by SVT while processing data, for example something can go wrong in the data transfer and the input FiFo on one board can become full, or some of the data received in input by one board are outside the valid range. The system can both set error flags in the VME register of the single board and propagate error flags in the data stream setting appropriate error bits on the End Event word [7]. The Fanout A can detect 4 out of the 8 possible SVT error conditions: the Parity Error (if the parity of the input XFT data does not match the Parity bit of the XFT End Event word), the Lost Synch (if the L2B of the XFT End Event word does not match the L2B of the L1 Trigger words), the FiFo Overflow (if one input FiFo gets full) and the Invalid Data (if the parameters of one XFT track are outside the valid address range of the Look Up Table). When the A board detects one of these conditions, it sets the corresponding error flag in the output End Event word. If one error bit is already asserted in the input EE word, it is propagated in the output EE word.

The SVT boards have also a system for data flow monitoring. The input and the output data streams from the boards are continuously copied to circular memories called Spy Buffers. In the Fanout A board these memories are 128K static RAMs for the XFT data and 64K both for the L1 Trigger data and for the output Spy Buffer, which spies data flowing to the P3 connector. These buffers act as built-in logic state analyzers and help system monitoring and diagnostics. As a consequence of error conditions these buffers can be frozen and read from VME with no interruption of the normal data flow.

B. Fanout B board

There are two identical Fanout B boards whose identity is set by an onboard switch. Their function is to receive the data from the Fanout A board through the P3 backplane and to distribute the 23 data bits to the proper SVT wedges according to the list of enable bits. They have also the

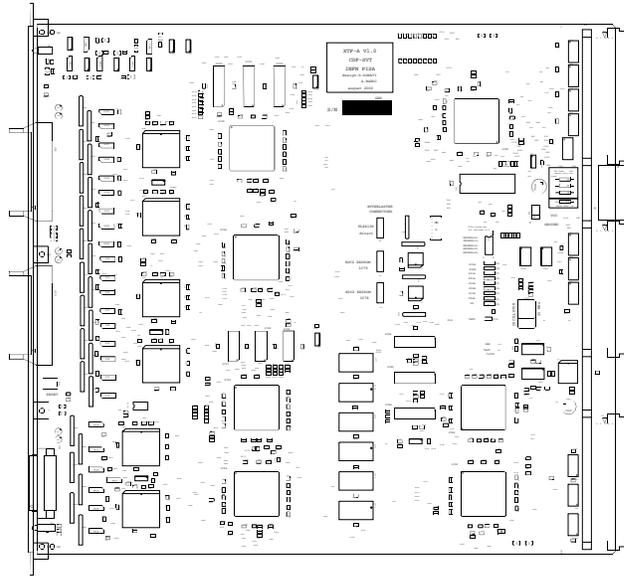


Fig. 1. PCB drawing of the Fanout A board. Left side is front panel side, right side is VME connectors side.

function to set the Parity bit in the End Event words sent to the 12 outputs. The Parity of each stream is computed by the A board and is transmitted to the B boards: when the EE word is sent from A to B, the 12 enable bits have a special meaning, each of them is the parity bit of the corresponding output stream. The B boards insert each PA bit in the EE word sent to the corresponding output stream.

In addition the B boards control the Hold and Data Strobe bits of each output stream. Data flow out of each Fanout B board through the 6 connectors on the front panel. If the Hold signal is received from any output, the line on the P3 backplane meaning Hold is set active and the Fanout A stops reading new data. Each Fanout B receives the clock from the Fanout A board through the P3 backplane and its logical functions are implemented on one 240 pin FLEX10K20 FPGA from Altera. For simplicity this board has no Spy Buffers and no VME interface.

III. OPERATION MODES

The Fanout system has two different operation modes: running mode and VME mode. In running mode it processes the data received through the input connectors and outputs the proper data to each SVT wedge. The VME mode is used to write the content of the Look Up Table used to map the XFT tracks into SuperStrips and for testing purposes. In particular in VME mode the content of any Spy Buffer can be written from the VME interface and the board can be forced to process these data as if they were the actual input streams. In this operating mode data contained in the input FiFos are disregarded. This can be done for both the input streams simultaneously as well as for only one. This allows an almost complete test

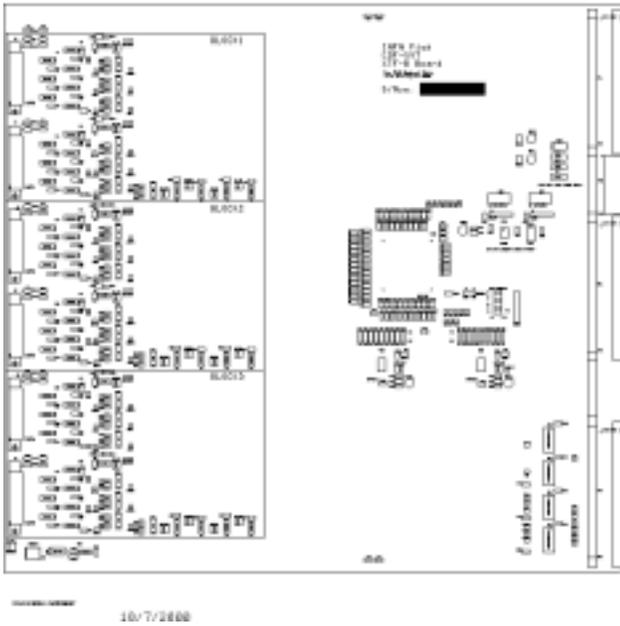


Fig. 2. PCB drawing of the Fanout B board. The orientation of the picture is as in Fig. 1.

of the system in absence of one or both the real input data sources.

IV. CLOCK DISTRIBUTION

Clock signals are generated on the Fanout A board and are distributed to the two Fanout B boards through two dedicated lines of the P3 backplane. Each Fanout B board receives one clock line. Clock generation on the Fanout A is accomplished by using one quartz oscillator connected to one PLL based clock buffer from Quicklogic (“Roboclock”). The Roboclock produces eight outputs with 4 adjustable phase shifts with respect to the input clock, also allowing zero or negative delays. The timing of each phase is adjusted by controlling the individual programmable delays of the Roboclock, in steps of about 1 ns. Each of the three Spy Buffers uses one Roboclock output to generate the write enable signals to the RAMs. Two Roboclock outputs are sent to the Fanout B boards and one is sent to a set of two PLL logic fanout chips which provide clock signals to the input FiFos and to the Altera FPGAs on the Fanout A.

Each Fanout B board is equipped with a system of two Roboclocks which receive in parallel the clock line from the Fanout A board. One Roboclock output is used by the Altera programmable chip. Each of the six output channels from the board uses one Roboclock output to generate the Data Strobe signal on the cable. This allows adjusting the Data Strobe timing with respect to the data bits.

V. PCB DESIGN

The Fanout A and B boards have been implemented as a six layers Eurocard 9U PCB. Critical lines have controlled impedance. The placement of components and routing

have been optimized for the maximum symmetry among similar functional blocks.

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