Radiation tolerant circuits designed in 2 commercial 0.25μ CMOS processes

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Abstract—**Characterization of simple devices as well as complex circuits, in two commercial 0.25μ processes, demonstrates a high level (up to 58Mrad) radiation tolerance of these technologies. They are also very likely to be immune to single event gate damage according to our results from 200MeV-protons irradiation.**

I. Introduction

The FPIX project is an effort underway at Fermilab to develop a pixel detector readout ASIC appropriate for use in the BTeV experiment. The detector is to be placed at about 6mm from the interaction point of the proton-antiproton beams. The estimated radiation levels at the edge of the detector are about 3Mrad/year and $0.6x10^{14}$ n/cm2/year. To address the high radiation problem, the choice has been made to exploit the inherent radiation tolerance of deep submicron processes with radiation tolerant layout technique [1]. Besides the radiation tolerance, these processes offer higher integration density, better performance and lower cost than special radhard processes. Because of their commercial nature we would also expect these technologies to be superior in term of reliability and yield. The density and functionality we achieved in our pixel cell would have been impossible in any available radhard process we know of.

We had two 0.25μ processes available to us: the TSMC 0.25μ process (process A) offered, through the MOSIS service, by the Taiwan Semiconductor Manufacturing Company, and the one chosen by CERN for the LHC (process B). After some comparison of the two technologies, we decided to design our circuit such that it would meet the specifications independent of which of these two processes were used. In this paper we will summarize our findings regarding the radiation tolerance of these two processes to total dose and bulk damage.

Throughout the paper rad implies rad(SiO_2).

II. Total Dose Effects on Transistors

We have irradiated samples from process A and B with a Co^{60} source under the same conditions. The irradiation took place at the Co^{60} irradiation facility of the Argonne National Lab. The dosimetry was performed using cobalt activated glass films and is known to be accurate to 20 percent. No filter for low energy particles was used, so any dose enhancement phenomenon was not taken into account. The estimated average rate was about 500 and 323 krad(SiO_2)/hr, for biased and unbiased transistors from process A. Transistors from process B were irradiated at about 420krad(SiO_2)/hr. We have irradiated several geometries, but the results presented here will be limited to NMOS transistors of a W/L of 10/0.28. More results and analysis will be presented at the conference.

Figure 1 shows the radiation induced voltage shifts. The maximum shift is less than 30 mV for all transistors. For Biased transistors from process, the shift is less than 20 mV even after 58 Mrad. After 2 days of annealing at 100°C the shift remained constant or decreased by less than 10mV.

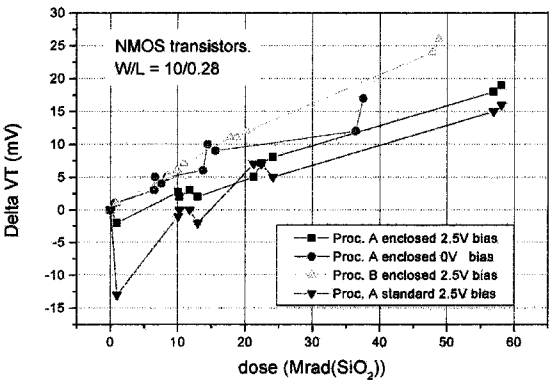

Figure 1. Radiation induced Vt shifts for NMOS devices in process A and B.

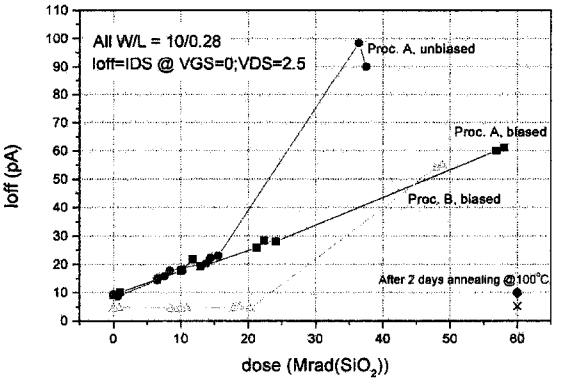

Figure 2. Leakage current versus dose for enclosed NMOS.

Leakage current is the most important degradation that an NMOS transistor incurs due to the activation of parasitic lateral devices. Edgeless (enclosed) transistors are expected to deal with this problem by suppressing the leakage path [1]. Figure 2 depicts the measured leakage

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current of 3 enclosed transistors. The maximum increase (from 10pA to 100pA) is observed for the unbiased transistor from process A. The leakage of all transistors returned to its pre-irradiation value after annealing.

Figure 3 depicts the leakage current of a standard (open) transistor. A very large increase is seen at the beginning, and a gradual decrease is seen afterwards. The "oscillations" seen might be the result of some annealing taking place during the measurement periods where the source was off. Interestingly even for the standard transistor the leakage returns to its initial value after annealing. Transistors from process B behaved the same way.

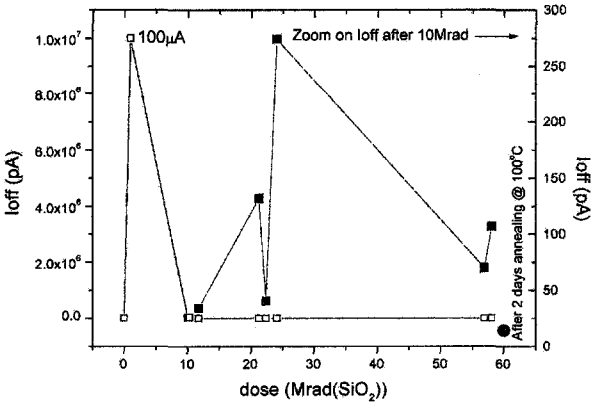

Figure 3. Leakage current of a standard NMOS transistor.

III. 33 MRAD(SI02) TOTAL DOSE EFFECTS ON THE PREFPIX2T PIXEL READOUT CIRCUIT

preFPIX2T is a 2X160 array of readout pixel cells fabricated in process A. Each cell contains an analog front end, 3 bit FADC, and the necessary control logic. The block diagram of the cell is shown in Figure 4. A complete description of the cell and the readout architecture can be found in [2]. The cell contains about 550 transistors. PreFPIX2T does not contain the associated end-of-column logic; it is implemented off chip. Our main objectives are to assess the threshold mismatch, noise distribution, systematic effects due to power distribution across the long columns and the radiation hardness of the design. The circuit has been tested both before and after exposure to 33 Mrad of Co^{60} ionizing radiation. The circuit was exposed at 285 Krad/hr. All the results shown are after 1 to 7 days of annealing at room temperature. During irradiation, the chip was biased as in a normal operation. The exact same bias settings were used for the before and after measurements.

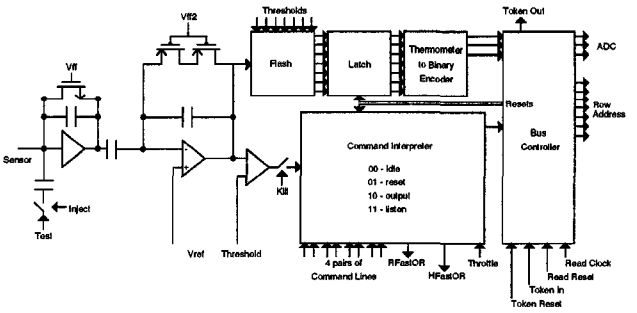

Figure 4. Bloc diagram of the pixel cell.

After 33 Mrad, the chip was fully functional with no degradation in speed (as inferred from the operation of along shift register). We observed less than 10 percent change in "analog" power. Power was less after irradiation, which is understandable from circuit point of view and is due to small Vt change in the PMOS. The current consumption of the ADC comparators depends on the PMOS threshold voltage.

Figure 5 shows the amplifier output pulse before and after 33 Mrad. The output pulse is measured at the output of a simple buffer amplifier placed at the output of the second stage.

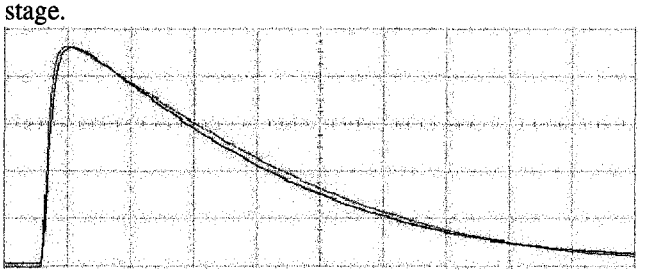

Figure 5. Buffered output of the analog FE before and after 33 Mrad. Vertical scale: 50mV/div. Horizontal scale: 500ns/div.

We observe less than 5 percent change in both the fall and rise times. A 3mV DC shift is also observed. Small signal linearity characteristics are shown in Figure 6. A maximum 7 percent gain degradation is incurred after irradiation. This is believed to be due to the simple output buffer (which is not part of the pixel cell). There are indications that even these small changes would disappear after proper annealing. As stated earlier, the two important parameters that we wanted to monitor are the threshold and noise distribution across the chip. Figure 7 shows the threshold distribution both before and after irradiation for the 320 cells A decrease in the mean threshold of less than 200e- is seen while the sigma is practically unchanged. For the noise, the mean ENC has increased by only 3e- (from 67e- rms before irradiation), while the sigma did not change.

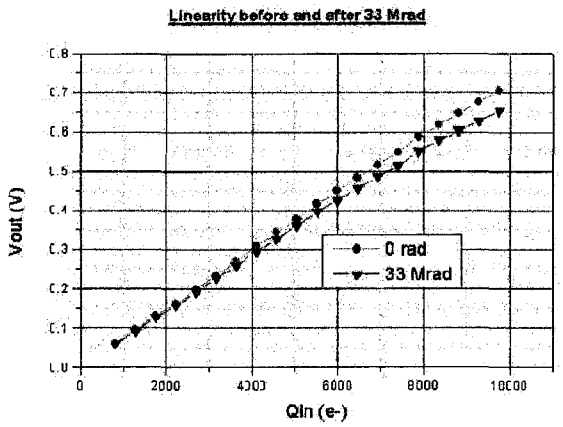

Figure 6. Small signal linearity before and after irradiation.

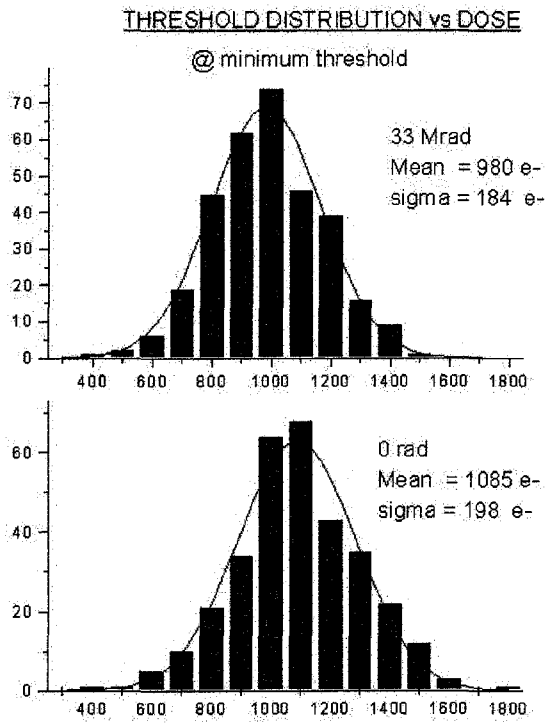

Figure 7. Radiation effects on the threshold distribution.

IV. Effects of 200 MeV proton fluence of $4.4x10^{14}$ p/cm2 on the PREFPIX2_I pixel readout circuit

PreFPIX2_I is a 18X32 pixel array with a complete trigger-less readout system, fabricated in process B. The chip contains about 500k transistors. We have irradiated 4 test boards with 200 MeV protons at the Indiana University cyclotron facility. The objectives were to assess the bulk damage, confirm the total dose tolerance and make sure that no gate rupture (or unexpected phenomena) is taking place. A total of about 2 millions transistors are involved in this test.

The boards were irradiated at a flux of $2.36x10^{13}$ p/cm^2/hr (1.97 krad/hr) resulting in a fluence of $4.43x10^{14}$ p/cm^2 (26 Mrad). The circuits were powered and biased as they would have been in their real environment.

After irradiation, all four boards were found to work properly with no major degradation, and they all suffered the same minor effects. Below is a brief summary of the results from one board only.

At this point it is worth mentioning that we have inferred an average, radiation induced, threshold shifts of –6mV and –105mV for the NMOS and PMOS respectively. The primary effect we have observed is a 100mV shift in the DC level of the second stage of the front-end. This is believed to be due to the shift in the PMOS threshold voltage and a slight increase in the parasitic junction leakage. The second stage uses a structure of two PMOS transistors in series, from input to output. The nwell of the two transistors is tied to the middle node and presents an N-P parasitic diode to the substrate. We believe it is an increase in the leakage of this diode, flowing from the output through the very high resistance of the first PMOS, that is responsible of the DC level shift. Figure 8 shows the buffered (and inverted) output of the second stage both before and after irradiation.

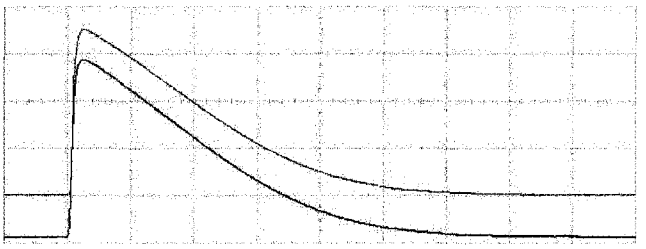

Figure 8. Front-end behavior before and after irradiation (lower trace). Vertical scale: 100mV/div, Horizontal scale: 500 ns/div. Input charge 10ke-.

The immediate consequence of the DC level shift is that in order to maintain the same charge threshold the programmable threshold voltage has to be adjusted by 100mV. Once that adjustment is done we have observed practically no change in the behavior of the chip. Figure 9 and 10 show the effect of radiation on the linearity and rise time of one channel. The fall-time remains practically unchanged. This is an indication that the NMOS has suffered no or very little degradation, since the fall-time is governed by the transconductance and threshold voltage of an N type transistor.

Figure 11 and 12 depict the threshold and noise distributions before and after exposure. The same behavior has been observed for all the four chips exposed. The threshold is practically unchanged while a decrease in noise is observed. The latter effect is due to an increase of the equivalent feedback "PMOS" resistance used in the second stage. This has been verified by changing the bias of the PMOS structure to restore its resistance to the pre-irradiation level.

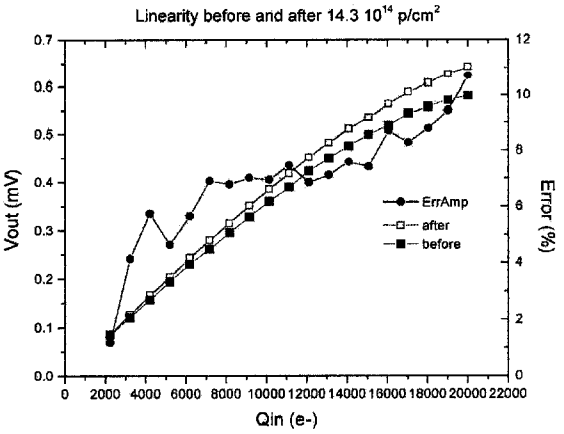

Figure 9. Vout vs. Qin before and after irradiation.

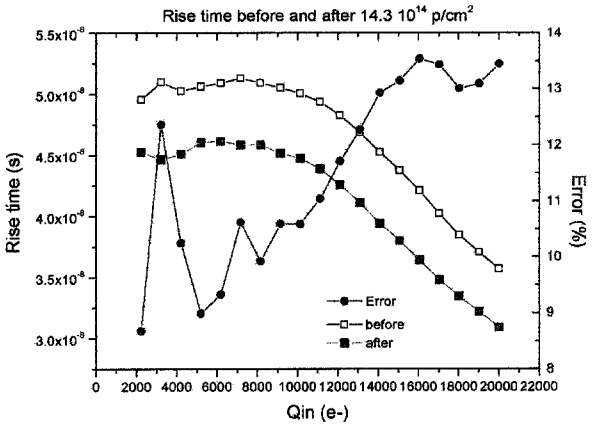

Figure 10. Effects of rise time.

V. Conclusions

We have presented several results related to the radiation hardness of two commercial 0.25µ processes. Characterization of simple devices as well as large complex circuits indicated a high level (up to 58Mrad) radiation tolerance. We also demonstrated that these technologies are also very likely to be immune to single event gate rupture.

We believe that these processes are very beneficial to people involved in the design of radiation hardened circuits.

VI. Acknowledgements

We would like to thank A. Dyer, G. Dychakowsky and K. Knickerbocker for their invaluable help.

VII. References

[1] W. Snoeys, "Radiation tolerance beyond 10 Mrad for a pixel readout chip in standard submicron CMOS", *CERN/LHCC/98-36*, September, 1998, [*Proc. Of the 4th Workshop on Electronics for LHC Experiments*, Rome, Italy, September, 1998, p. 114].

[2] A. Mekkaoui and J. Hoff, "30 MRad (SiO2) Radiation tolerant pixel front end for the BTeV experiment" *Proc. Of Pixel 2000*, Genova, Italy, June, 2000. To be published in NIM.

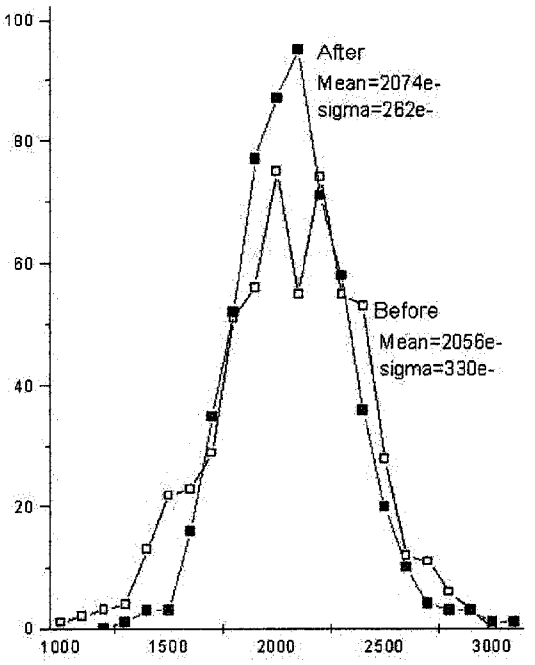

Figure 11. Threshold distribution before and after 4.4x10^{14} p/cm^2 (26Mrad).

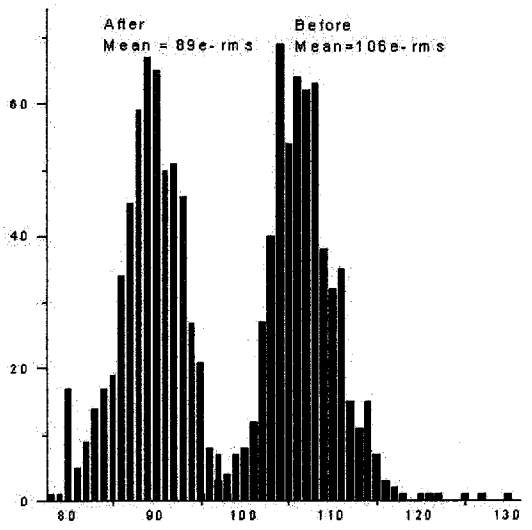

Figure 12. Noise distribution before and after proton irradiation.