



Development of High Data Readout Rate Pixel Module and Detector Hybridization at Fermilab

S.Zimmermann, S.Kwan, G.Cancelo, G.Cardoso, S.Cihangir,
D.Christian, R.Downing, J.Hoff, P.Kasper,
A.Mekkaoui, A.Vargas^{*+}, R. Yarema

Fermi National Accelerator Laboratory, Batavia, IL 60510 (USA)

**Universidad Autonoma de Puebla, Puebla, PUE 72570 (Mexico)*

Abstract

At Fermilab, both pixel detector multichip module and sensor hybridization are being developed for the BTeV experiment. The base line design of the module and preliminary results of characterization tests are presented.

1. Introduction

At Fermilab, the BTeV experiment has been proposed for the C-Zero interaction region of the Tevatron [1]. The innermost detector for this experiment will be a pixel detector composed of 31×2 pixel planes of approximately 100×100 mm each, assembled perpendicularly to the colliding beam and installed a few millimeters from the beam. Each plane is formed by sets of three different lengths of pixel hybridized modules, each composed of a single active-area sensor tile and of one row of pixel readout (RDO) integrate circuits (ICs).

The pixel detector will be employed for the lowest level trigger system, hence, the pixel readout ICs will read out all detected hits. This requirement imposes

a severe constraint on the RDO IC, hybridize module and data transmission rate to the data acquisition system. Several factors impact in the amount of data that each RDO IC needs to transfer: IC active area, distance from the beam, data format, etc. The final size of the RDO IC is still under consideration.

The BTeV pixel detector is based on a design relying on a hybrid approach. With this approach, the RDO IC and the sensor array are developed separately and the detector is constructed by flip-chip mating of the two together. This offers maximum flexibility in the development process, choice of fabrication technologies, and the choice of sensor material.

2. Proposed Pixel Module

Figure 1 shows a sketch of the proposed module (top and side views). The module is composed of three layers. The lowest layer is formed by the RDO ICs. The back of the ICs are

Work supported by the U.S. Department of Energy under contract No. DE-AC02-76CH03000.

⁺ Scholarship holder of CONACyT, Mexico.

in thermal contact with the supporting structure while the other side is bump-bonded to the pixel sensor. The clock, control and power pad interface of the RDO ICs extend beyond the edge of the sensor. The polyimide interconnect circuitry is glued on the top of this assembly and the RDO IC pad interface wired bounded to the circuit. The circuit then extends to one end of the module where the rad-hard module controller and high speed data serializers ICs and fiber optic connectors are assembled [2]. These components are located in this position so that they are outside the tracking volume. ATLAS and CMS explore similar solution [3, 4, 5].

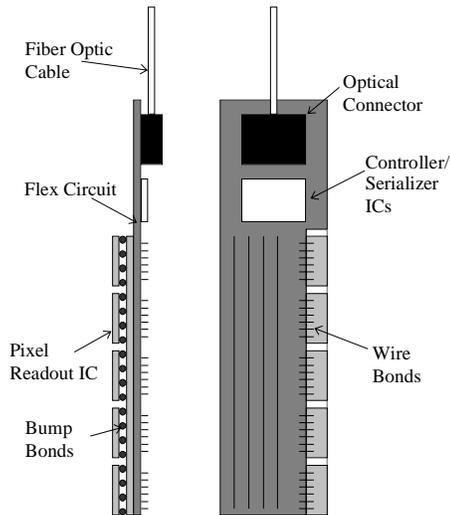


Figure 1. The Flex Polyimide Module

The pixel module readout strategy is paramount to employ the pixel detector in the lowest level trigger. Our present assumptions are based on simulations that describe the track behavior inside the pixel detector. The parameters used for the simulations are: luminosity of $2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ (corresponds to an average of two interactions per bunch crossing), pixel size of $400 \times 50 \text{ } \mu\text{m}$, threshold of 2000 e^- and magnetic field of 1.6 Tesla.

Figure 2 shows a sketch of the 40 ICs that may compose a pixel half plane. The beam passes on the place represented by the black dot. These numbers assume specific data format and IC size. The distance from the beam to the closest ICs is 6 mm.

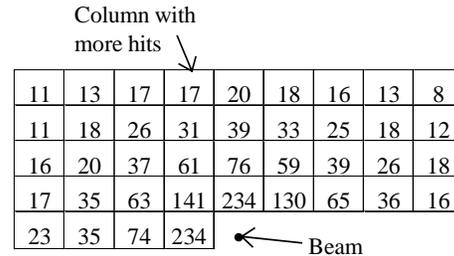


Figure 2. Average Bit Data Rate, in MBits/sec

The column with more hits requires the biggest data bandwidth. Figure 3 shows the proposed block diagram of the circuit interconnect with the data rate for this column. The serializer IC handles 16 bit words at 60 MWords/sec. There is one dedicated 12 bit data bus connecting the pixel RDO IC with the highest data rate directly to the serializer, another 12 bit data bus that is shared by two ICs and finally a six bit data bus that is shared by the two remaining ICs. The six bit data bus is split between the two serializers. With this interconnect scheme there is an additional bandwidth to handle peak data rates and unpredicted hits between 3.1 and 4.6 times the required average bandwidth.

Clearly, a high density circuitry is necessary to interconnect the pixel RDO ICs with the controller and serializer ICs. The width of the circuit trace area is approximately 5 mm and the estimated number of traces for clocks, controls and data is 45 traces

running in parallel in the densest portion of the flex circuit. Therefore, each trace, vias and clearance has to fit in less than 110 μm . Fujitsu Computer Packaging Technologies (FCPT, San Diego) is prototyping such high density interconnect. FCPT capabilities include flex circuits with line traces of 20 μm in a 40 μm pitch, copper line thickness smaller than 5 μm , vias spaced by 200 μm , via cover pads of 100 μm and average via hole diameter of 26 μm . FCPT can manufacture circuits with four copper layers or more using the Z via technique to interconnect flex circuit copper layer pairs [6].

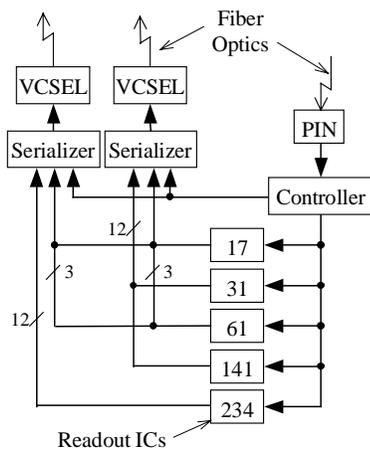


Figure 3. Pixel Module Block Diagram

Another approach to control and readout the RDO ICs is also under consideration. This option is a direct consequence of the BTeV detector layout [1]. The BTeV detector covers the forward direction, 10 to 300 mrad, with respect to both colliding beams. Hence, all volume outside this section is outside the active area and can be used to house readout and control electronics without interfering with the experiment. This other option takes advantage of this consideration. The proposal is to

move the serializer and controller logic 30 cm from the beam where the radiation dose will be less than 10 KRads. There, hopefully, components-off-the-shelf can be employed. The only IC on the pixel module would then be the RDO IC.

3. First Prototype of the Pixel Module

Figure 4 shows a picture of the first prototype of the pixel module. It is composed of a pixel sensor bump-bonded to five FPIX1 RDO ICs [7] and a four layer high density flex circuit manufactured by FCPT. In this prototype the flex interconnect is located on the side of the ICs instead of on the top of the sensor (as in the baseline design). The pixel sensor used can be bump-bonded to a total of 16 RDO ICs.

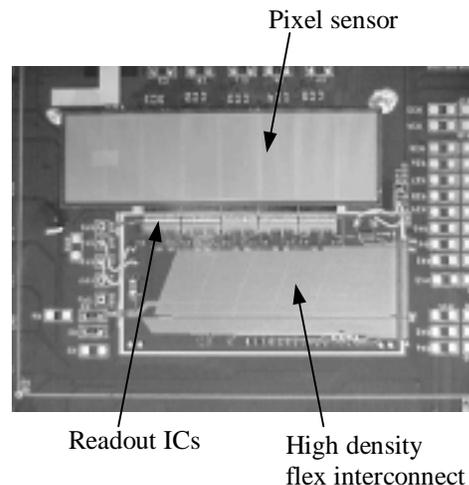


Figure 4. Prototype Pixel Module

This module has been characterized for noise and threshold dispersion. These characteristics were measured by injecting charge in the analog front end with a pulse generator and reading out the hit data through a logic state analyzer [8]. Data of just four RDO

ICs is available because one of the chips failed. The results for one specific threshold are summarized in Table 1. The comparison of these results with the results of a single FPIX1 IC shows no noticeable degradation in performance [9]. Furthermore, tests with dead timeless mode, where the charge inject in the front end is time swept in relation to the readout clock also does not reveal any degradation in performance, strongly suggesting no crosstalk problems between the digital and analog sections of the FPIX1 and flex circuit.

Table 1. Performance of the Five Chip Module (in e^-)

Chip	1	2	3	4
Threshold	1649	1406	1589	2865
Threshold σ	254	307	222	250
Noise	62	53	49	62
Noise σ	16	13	11	11

4. Results of the hybridization to pixel sensors

As already stated, the hybridization approach pursued offers maximum flexibility. However, it requires the availability of highly reliable, reasonably low cost fine-pitch flip-chip mating technology. Three bump bonding technologies were tested: indium, fluxed solder, and fluxless solder. Real sensors and RDO ICs were indium bumped at both the single chip or wafer level by BOEING, NA. Inc (Anaheim, CA) and Advance Interconnect Technology Ltd. (Hong Kong) with satisfactory yield and performance. Figure 5 shows the hit maps of one FPIX1 detector using a radioactive source. All the channels seem to be working.

Also, tests on dummy detectors to evaluate eutectic Pb/Sn solder were conducted. The vendor, MCNC (Research Triangle Park, NC), together with UNITIVE Electronics, produced the dummy parts, and then carried on with the bumping process. The detectors are composed of channels which are a number of daisy-chained bumps at 50 μm pitch connected to probe pads at an edge of the dummy detector. The bump yield was characterized by measuring the resistance of each channel, and (to check for shorts) the resistance between neighboring channels.

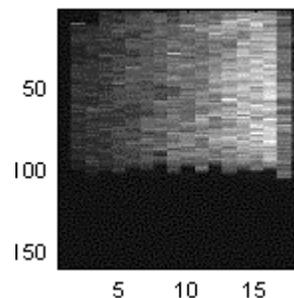


Figure 5: Hit map of one detector

Both fluxed and fluxless solder bumps have been studied. Much better results using the fluxless process were found. The yield from the fluxed process is poor and the delivered parts have a lot of residue left behind from the cleaning of the flux. For the fluxless assemblies, a process called Plasma Assisted Dry Soldering (PADS) [10] is used. The bumped chip wafer (top plates of the dummies) and unbumped substrate wafer (bottom plates of the dummies with only under-bump metallization put on) were diced and tacked together (flip-chip assembly) before being treated in the PADS process. The joints were then reflowed at 250°C. After being reflowed, the detectors were rinsed with methanol

and dried in air. The diameter of the bumps is ~40 microns, and the height is ~15 microns after mating. The estimated resistance of a single solder bump is less than 1 Ω .

Two of the 82 detectors tested were misaligned to cause one bump shift resulting in open channels and shorted adjacent channels. Five detectors had over 50% of their channels open or at high resistance. One was sent to MCNC to be examined. It was taken apart and found to have the bumps on the top plate (chip) not touching the pads on the bottom plate (substrate). This was probably due to contamination or debris on the substrate on that particular location. All this results in an assembly yield of 91.5% (75 good out of 82). For the good detectors, a channel yield of 99.32% or 6.8×10^{-3} failed-channel/channel (106 open or high-resistance channels altogether), and with 14 or 16 bumps per channel and with the assumption that only one bump is bad, a bump yield of 99.95% or 4.5×10^{-4} failure/bump.

5. Conclusions

This paper describes the baseline design and a variation of the pixel module to handle the data rate required for the BTeV experiment at Fermilab. The present prototype has shown good electrical performance characteristics.

Indium bump bonding is proven to be capable of successful fabrication at 50 micron pitch on real detectors. For solder bumps at 50 micron pitch, much better results have been obtained with the fluxless PADS processed detectors. The results are adequate for our needs and our tests have validated it as a

viable technology.

References

- [1] Kulyavtsev, A., *et.al.*, BTeV proposal, Fermilab, May 2000.
- [2] Cancelo, G.E., *et.al.*, "Fiber Optic based readout for BTeV's Pixel Detector," to be presented 6th Workshop on Elect. LHC Exp., Krakow, Sept. 2000.
- [3] Richardson, J., "The ATLAS pixel on-detector electronics," 5th Workshop on Elect. LHC Exp., Snowmass, pp.83-87, Sept. 1999.
- [4] Skubi, P., *et.al.*, "Flex circuits for the ATLAS pixel detector," Proc. Pixel98, pp.519-534, Batavia, IL, May 1998.
- [5] Baur, R., "Readout architecture of the CMS pixel detector," see these proceedings.
- [6] Chou, B., *et.al.* "Ultra-High-Density Interconnect Flex Substrates," HDI Magazine, Marietta, GA, Dec. 1998.
- [7] Christian, D.C., *et.al.*, "Development of a pixel readout chip for BTeV," NIM A 435, pp.144-152, 1999.
- [8] Vargas, A., "Development of software to characterize the Fermilab pixel readout chip, FPIX1, for the BTeV Experiment," to be submitted to NIM.
- [9] Mekkaoui, A., *et.al.*, "FPIX2: an advanced pixel readout chip," 5th Workshop on Elect. LHC Exp., Snowmass, pp. 98-102, Sept. 1999.
- [10] Koopman, N. *et.al.*, "Fluxless No-Clean Assembly of Solder Bumped Flip Chips," 46th ECTC, Orlando, Florida, May 28-31, 1996.

