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30Mrad(SiO_2) radiation tolerant pixel front end for the BTEV experiment☆

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Abstract

The FPIX project is an effort underway at Fermilab to develop a pixel detector ASIC appropriate for use in the BTEV experiment. The most ambitious aspect of this project is that all data from all hit pixels must be read out every beam crossing (132 ns) for use in the lowest level trigger system. Included in each 50 μm × 400 μm pixel is a three-bit analog to digital converter which provides pulse height information to improve resolution. Given the proximity to the beam, the chips must be radiation tolerant. Rather than focusing efforts on a rad-hard technology, the choice has been made to use the inherent radiation tolerance of deep submicron processes with radiation tolerant design techniques. This paper discusses both the design and the radiation tolerance of the FPIX pixel cell.

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Keywords: Pixel; Radiation tolerance; Deep submicron

1. FPIX history

Our first prototype chip, FPIX0, was designed in 1997 with the goal to establish a pixel front-end optimized for the Tevatron collider environment and which addresses some of the BTEV experiment requirements. It is an array of 12 columns × 64 rows with a column based sparse readout. The pixel cell includes a charge sensitive preamplifier AC coupled to a second stage for addition gain, a comparator, a peak detector and the readout logic. The peak detector provides a voltage proportional to the input charge that is read out with the pixel address and is digitized off chip. The chip was fabricated in the HP 0.8 μm CMOS process. A description of FPIX0 and its measurement results can be found in Refs. [1,2]. FPIX0 has been successfully tested in a beam at Fermilab in the 1999 summer. The beam test results can be found in Ref. [3].

In 1998 we undertook a more ambitious second step by designing the FPIX1 chip with a new readout architecture that addresses the BTEV experiment requirements (as understood at that time). A complete description of the architecture can be found in Refs. [5–7]. For the FPIX1 front end we used the same principles as in FPIX0 with few exceptions. The main difference is that we replaced the peak detector with a 2-bit flash ADC. We were encouraged to do so by Monte Carlo simulations of the BTEV interaction region which

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suggested that 2-bit analog information might be sufficient to obtain the required spatial resolution [4]. It was also the only solution known to us that is compatible with a readout as fast as that required for the experiment. FPIX1 was fabricated in the HP 0.5 μm process. Since the final chip has to be radiation hard, our thought at the time was to migrate our design to the then promised Honeywell 0.5 μm SOI rad-hard process. The latter has never been made available. Encouraged by the excellent results obtained by the CERN RD49 group [8,9] with regard of the radiation hardness of deep sub-micron processes, we decided to implement our design in a 0.25 μm technology. We had two 0.25 μm processes available to us: the one chosen by CERN for the LHC and the TSMC 0.25 μm process offered, through the MOSIS service, by the Taiwan Semiconductor Manufacturing Company. After some comparison of the two technologies, we decided to design our circuit such that it would meet the specifications independent of which of these two processes were used.

Our first radiation tolerant chip, named PreFPIX2, was designed in 1999 and fabricated in the TSMC 0.25 μm process. It contains several isolated transistors for radiation evaluation and eight cells containing the radiation tolerant analog front end (charge amplifier + 2nd stage + comparator + 1 FADC stage). Results from this chip will be presented subsequently.

After the successful test of preFPIX2, we proceeded with design of preFPIX2T which a 2 × 160 array of complete pixel cells. The pixel cell unit contains the re-designed analog front end (the same as in preFPIX2 with minor modifications), 3 bit FADC, and an enhanced (with respect to FPIX1) control logic. The pixel size was maintained to be 50 μm × 400 μm. PreFPIX2T has been tested both before and after exposure to 33 Mrad (SiO_2) of ionizing radiation. The results will be presented in the following sections.

2. Radiation tolerant front end

A radiation tolerant design uses enclosed structures for all NMOS transistors to prevent radiation-induced leakage through device edges, and guard rings to isolate devices [8,9]. To explain some of the challenges we faced when we wanted to move our design from a standard layout to one that is radiation tolerant, we will discuss the design of the feedback structure and leakage compensation in the charge preamplifier.

Fig. 1 depicts the block diagram of the FPIX1 pixel cell. The DC feedback is assured by the Mff–Mf transistor pair. The feedback transistor is biased with respect to the amplifier output by the diode connected transistor Mff which is forced to conduct a current Iff. Iff is a global parameter that controls the shaping of the output pulse. When Mf is in saturation, the feedback capacitor is discharged at a constant current Iff. This provides and enhanced controllability and stability. The principle also provides for automatic tracking with respect to the DC level of the preamp, which might drift because of bias level, temperature, radiation, etc. The same structure help in tolerating DC leakage currents. If an electron-collecting sensor is used, a DC leakage current would flow from the preamp input to the detector. This current would cause the DC level at the preamp output to raise. Consequently, the Vff bias voltage would follow, causing the equivalent feedback resistance to drop, which in turn minimize the DC level drop at the output. For adequate stability and noise the equivalent feedback resistance should take into account the highest leakage current expected. The net result is that the feedback current should be small (5–10 nA) and Mf should have a $(W/L) \ll 1$.

Because of the dependence of width of an enclosed transistor on its length, the minimum W/L is around 2.5 [10]. Furthermore, the transconductance of devices in the 0.25 μm processes are higher than in the 0.5 μm one, which complicates further the realization of an equivalent high resistance using an NMOS structure. It became clear to us that our scheme could not be implemented using the radiation tolerant style. A PMOS as a feedback device was rejected because of DC bias problems due to the fact that we chose to retain an NMOS as input device.

The solution was to decouple the DC feedback problem from the leakage compensation problem. We adopted the solution shown in Fig. 2. Assuming we compensate for the leakage current, the

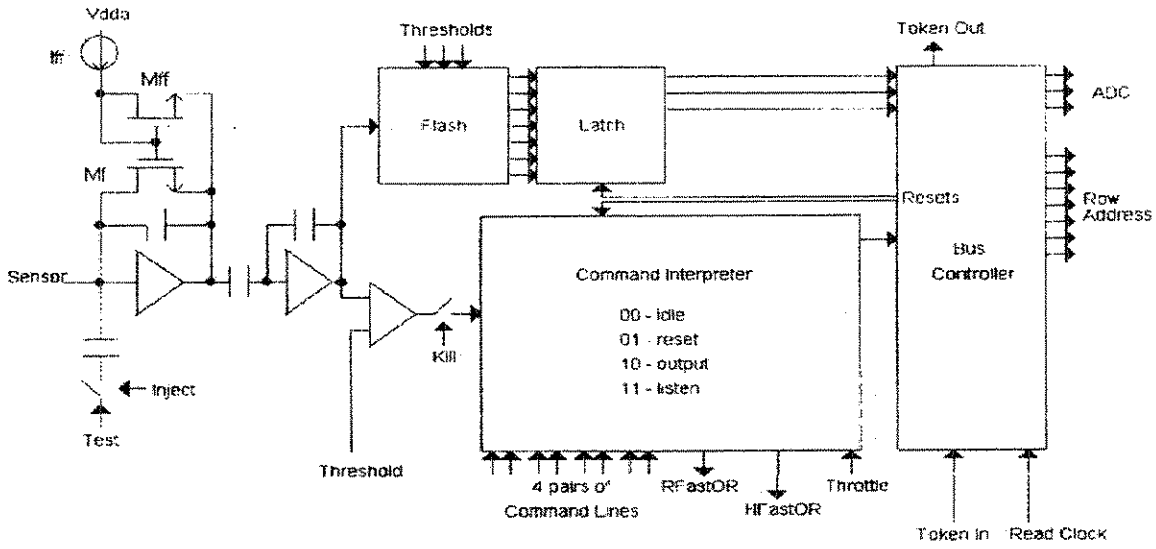

Fig. 1. A block diagram of the FPIX1 Cell.

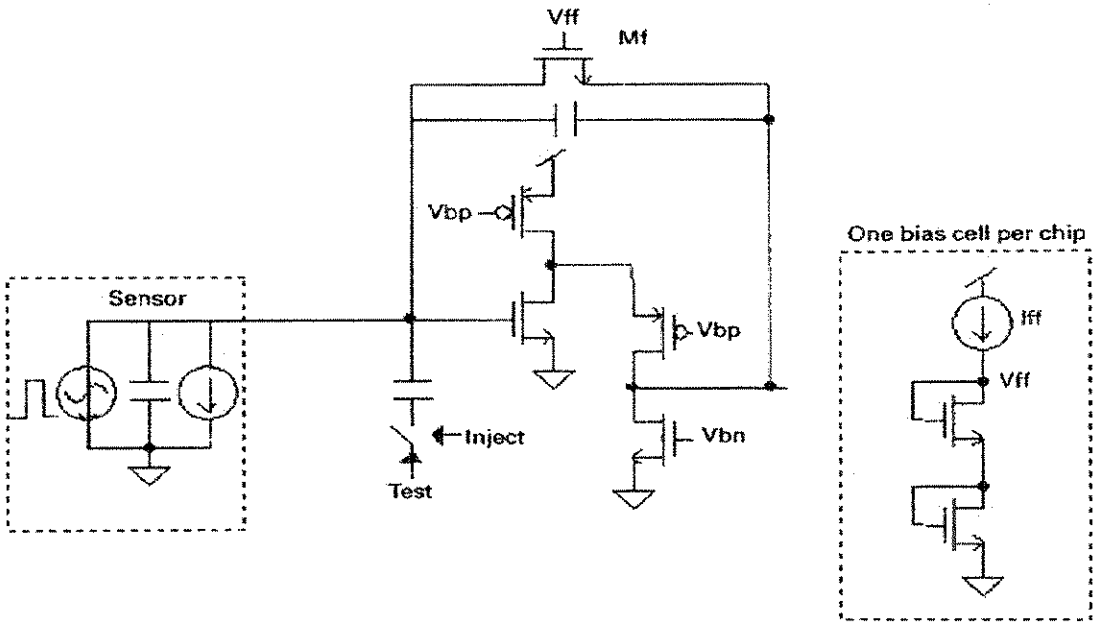

Fig. 2. The solution of the DC feedback problem.

feedback transistor does not have to be sized as a function of the maximum leakage current. The Vff voltage is provided globally by the bias cell shown in the figure. Transistor Mf is still biased with respect to a DC voltage that is determined by an NMOS transistor. This provides some tracking with respect to temperature and process variation. First order tracking of bias conditions will be

assured because both Iff and the current in the input device are function of a master bias current.

Leakage current compensation is carried out by the structure shown in Fig. 3. When no DC current is flowing through the feedback device both the input and output nodes of the preamplifier are at the same potential. When a DC current starts flowing through Mf (Rf in the figure) the output node voltage starts increasing, causing the output of the compensation amp to decrease. The current through the PMOS transistor increases in turn, decreasing the current through the feedback. When this double feedback action stabilizes, the current flowing through the equivalent feedback resistance is very small and the current conducted by the compensation PMOS is nearly equal to the leakage current.

It is very important that the compensation amp have a very low bandwidth not to interfere with high frequency signals and to preserve the stability of the front end. A high DC gain and a low offset are essential to minimize the residual current in the feedback. The largest leakage current that can be compensated depends, primarily, on the size of the compensation PMOS device, which also contributes noise directly at the input. Generally a compromise solution should be found. In our application the maximum expected leakage current is about 50 nA. Even if by taking a safety factor of 2, it was possible to size this device to reduce its contributed noise to an acceptable level (<4 percent increase in noise due to this device).

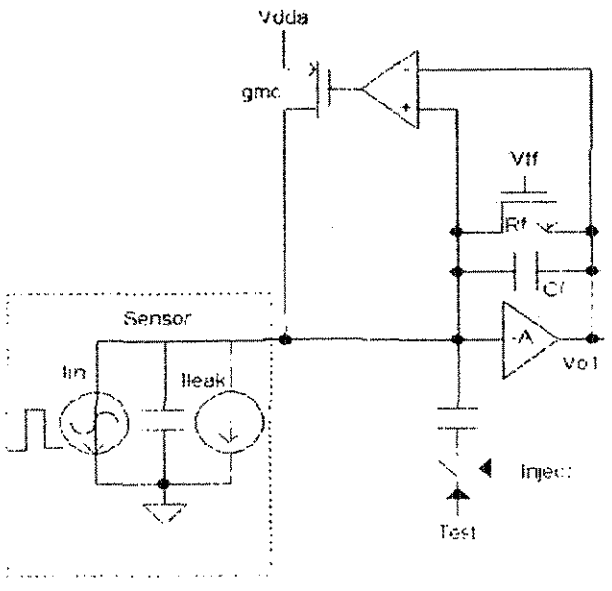

Fig. 3 Leakage compensation circuitry.

3. Results

Fig. 4 shows the front-end response to different input charges, at nominal bias settings. The measured gain (78 $\mu V/e^-$) is very close to the expected one (80 $\mu V/e^-$). As stated previously, the recovery time (return to base line) is controlled by the global feedback bias current Iff. Fig. 5 shows the response to the same input charge at different feedback bias currents. In the experiment, chips with high occupancy will be biased so as to speed recovery and reduce pixel dead time. Fig. 6 depicts both the 10–90 per cent recovery time and the Equivalent Noise Charge (ENC) versus the feedback bias current.

As mentioned earlier one of the main modifications we introduced in this design was the leakage compensation scheme. Fig. 7 shows the behavior of the amplifier when different leakage currents are injected at the input. The leakage current is forced from the outside into the input via an NMOS current mirror added to the layout of one of the eight channels. Leakage currents up to 300 nA could be injected without distorting the dynamic response. The noise contribution of the current mirror was, though, very high. It is clear from the figure that very small leakage current is needed to overcome the offset of the compensation amplifier. Once the offset is overcome, the amplifier is active and no change is observed in the output pulse shape with increasing leakage currents. The change in the fall time is due to the fact that the small offset leakage has caused the output potential of the charge amplifier to change, and hence changing the equivalent feedback resistance

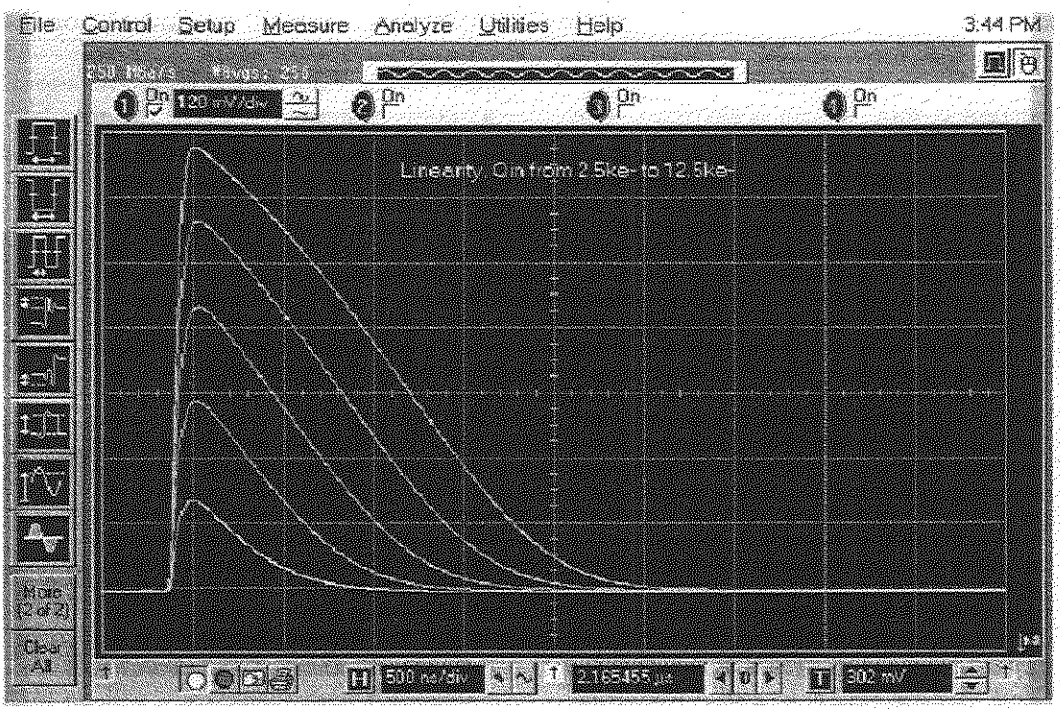

Fig. 4. Front-end response to different input charges.

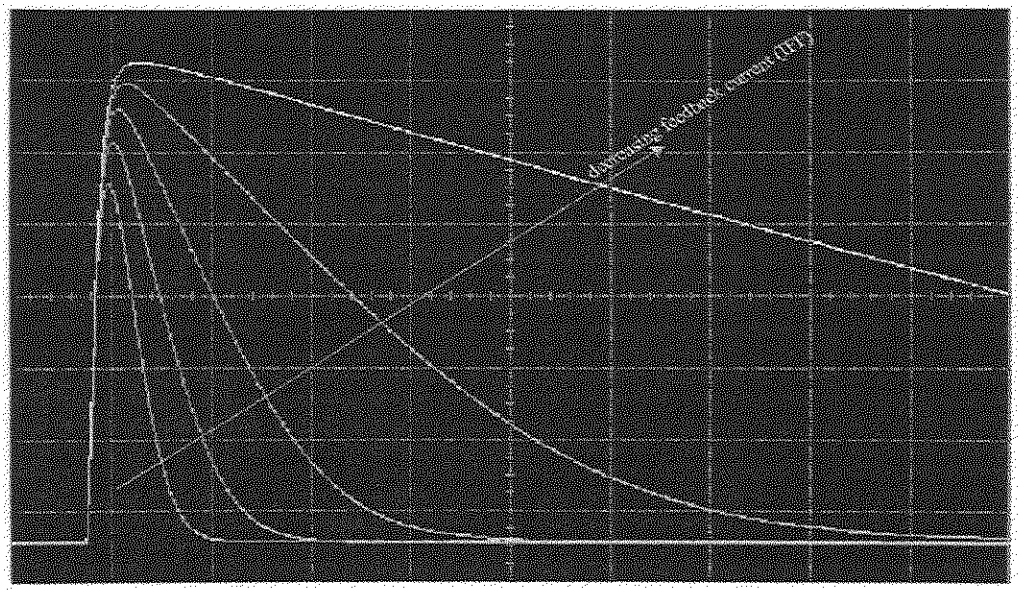

Fig. 5. Response to the same charge with different feedback biases.

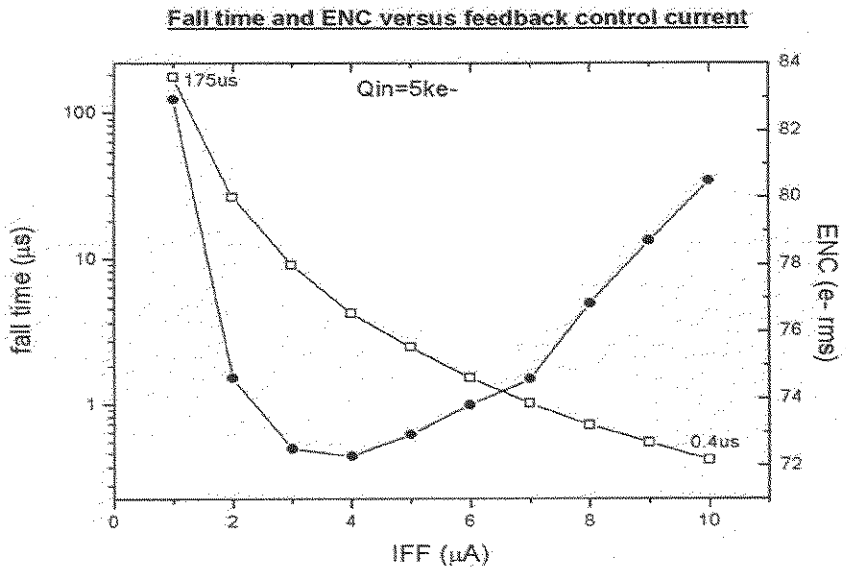

Fig. 6. Recovery time and equivalent noise charge.

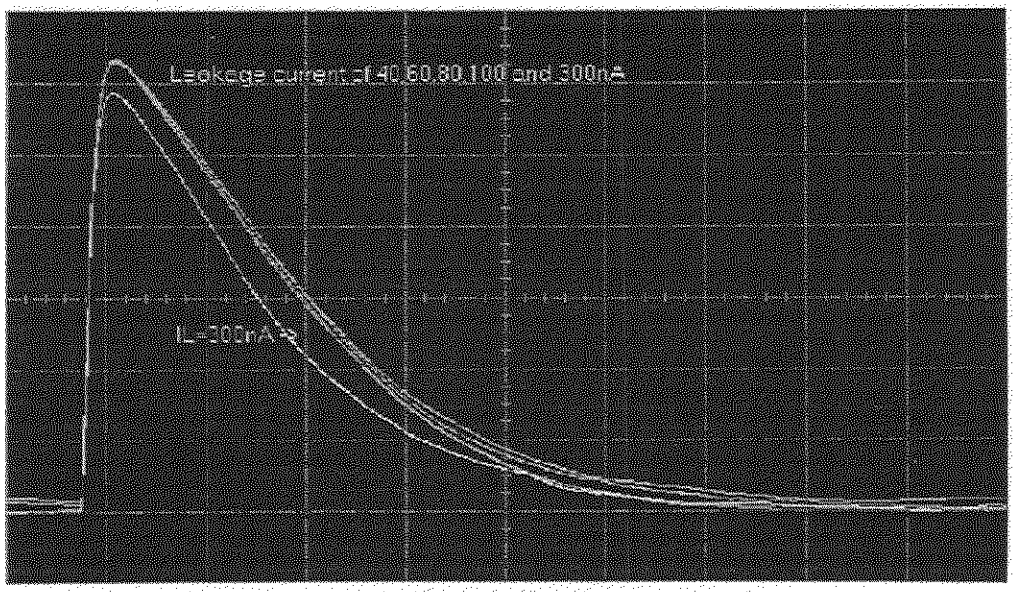

Fig. 7. Behavior under different leakage currents.

4. PreFPIX2T

preFPIX2T is a 2×160 array of readout pixel cells, each contains the re-designed analog front end (the same as in preFPIX2 with minor modifications), 3 bit FADC, and an enhanced (with respect to FPIX1) control logic. The block diagram of the cell is shown in Fig. 8. A complete

description of the readout architecture can be found in Ref. [11]. PreFPIX2T does not have the required end-of-column logic, it is implemented off chip. Our main objectives are to asses the threshold mismatch, noise distribution, systematic effects due to power distribution across the long columns and the radiation hardness of the design. The circuit has been tested both before and

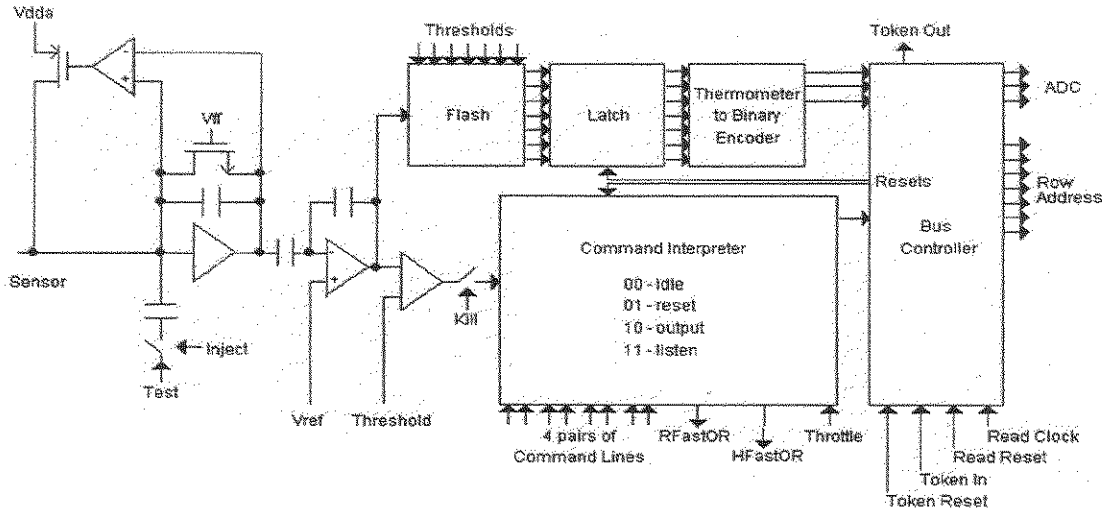

Fig. 8. preFPIX2 pixel cell block diagram.

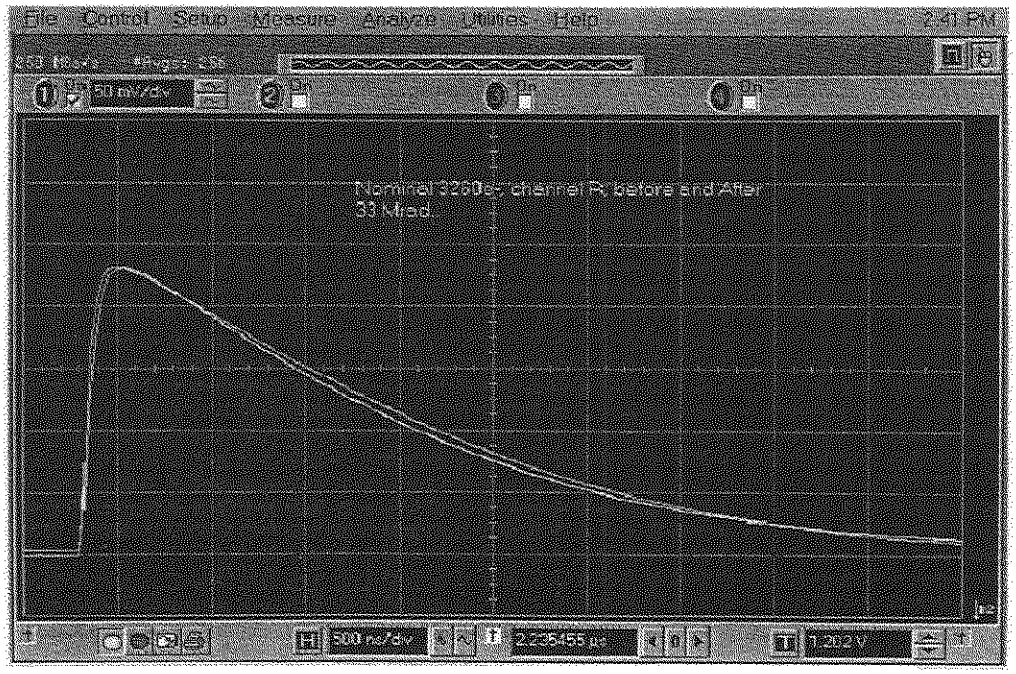

Fig. 9. Amplifier output before and after irradiation.

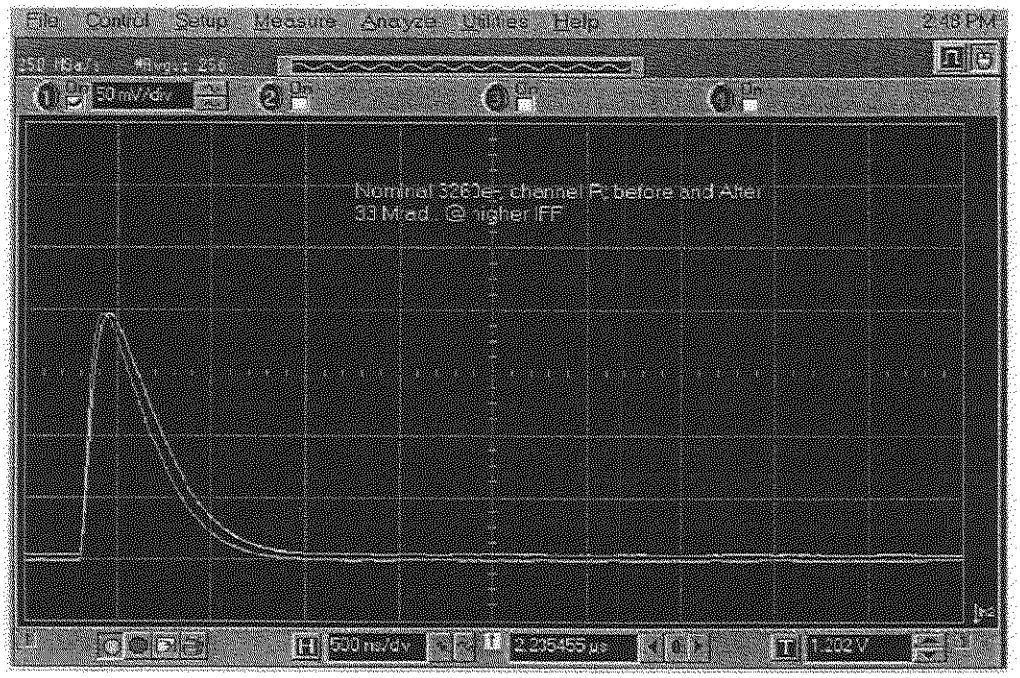

Fig. 10. Amplifier output before and after irradiation at higher feedback current.

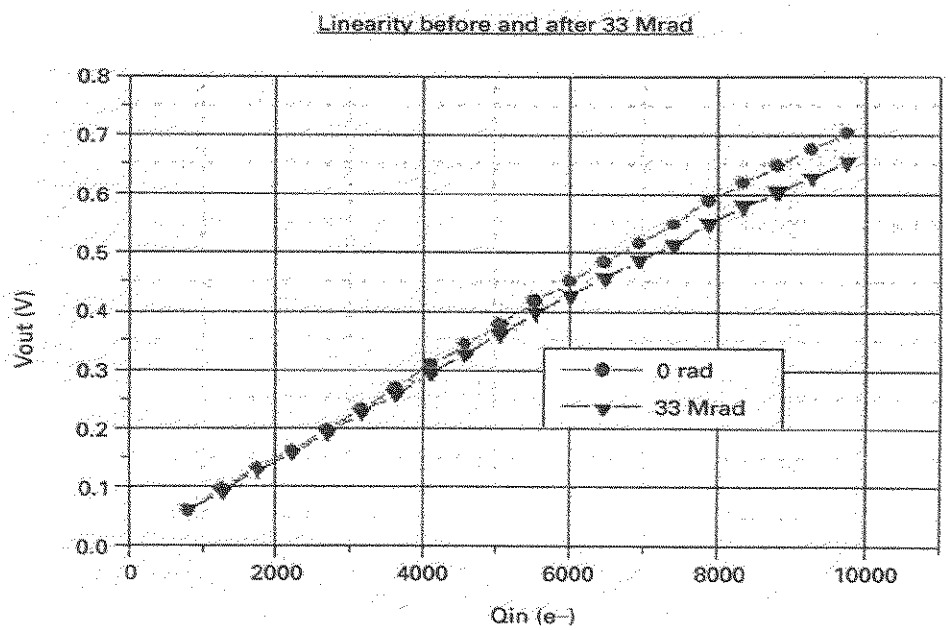

Fig. 11. Small signal linearity characteristics.

after exposure to 33 Mrad (SiO_2) of ionizing radiation.

The irradiation took place at the ^{60}Co source facility at Argonne National Lab. The dosimetry was performed using cobalt activated glass films and is known to be accurate to 20 percent. No filter for low energy particles was used, so any dose enhancement phenomenon was not taken into account. The estimated average rate was about 285 krad/h in SiO_2. All the results shown are after 1–7 days of annealing at room temperature. During irradiation, the chip was biased as in a normal operation. No bias adjustments were carried out for the post-irradiation measurements.

After 33 Mrad, the chip was fully functional with no degradation in speed (as inferred from the kill/inject shift register operation). We observed less than 10 percent change in "analog" power. Power was less after irradiation which is understandable from circuit point of view and is due to small VT change in the PMOS (<40 mV). The current consumption of the ADC comparators depends on the PMOS threshold voltage.

Fig. 9 shows the amplifier output pulse before and after 33 Mrad. The output pulse is measured at the output of a simple buffer amplifier placed at the output of the second stage. Fig. 10 shows the same measurement at a higher feedback current (faster return to base line). We observe less than 5 percent change in both the fall and rise times. A 3 mV DC shift is also observed. Small signal linearity characteristics are shown in Fig. 11. A maximum 7 percent gain degradation is incurred after irradiation. This is believed to be due to the simple output buffer (which is not part of the pixel cell). There are indications that even these small changes would disappear after proper annealing.

As stated earlier, the two important parameters that we wanted to monitor are the threshold and noise distribution across the chip. Figs. 12 and 13 show these distributions both before and after irradiation for the 320 cells. A decrease in the

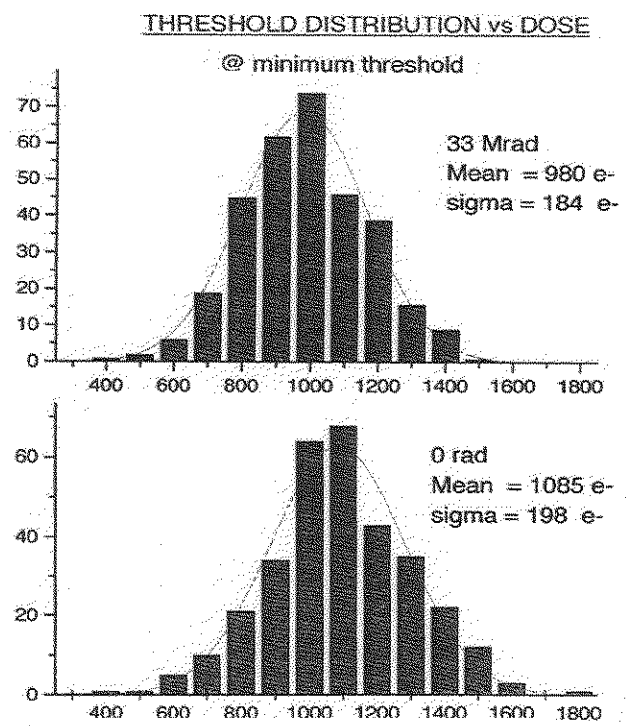

Fig. 12. Threshold variation before and after irradiation.

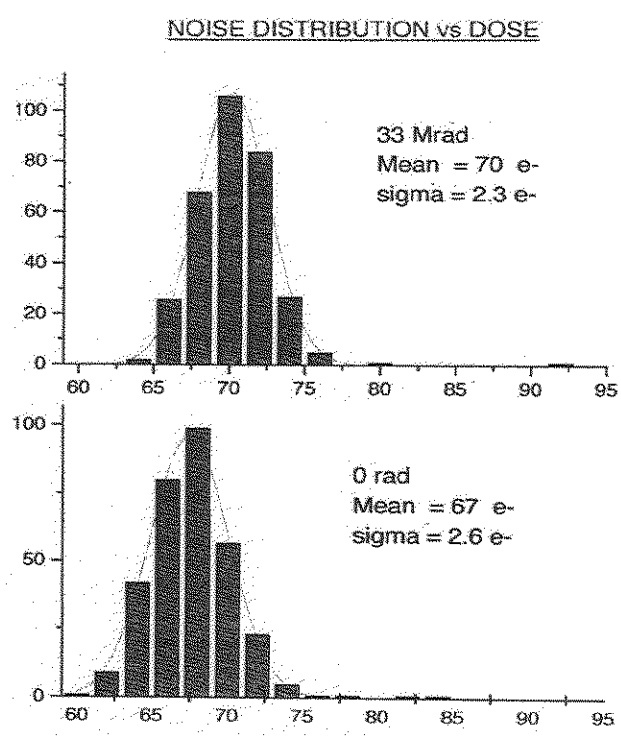

Fig. 13. Noise distribution before and after irradiation.

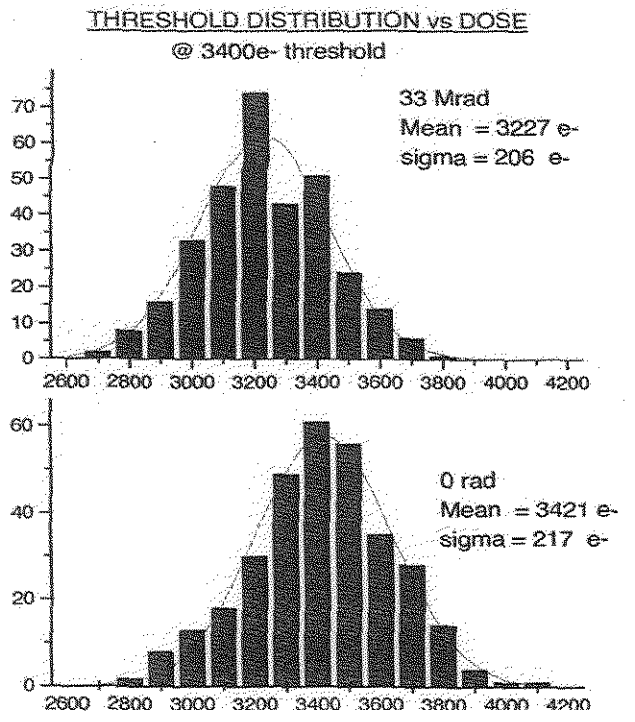

Fig. 14. *Threshold variation at higher threshold before and after irradiation.*

mean threshold of less than 200 e^- is seen while the sigma is practically unchanged. The mean ENC has increased by only 3 e, while the sigma did not change. Fig. 14 shows the threshold distribution at a higher threshold. Again, the mean threshold has been offset by only 200 e^-.

5. Conclusions

We successfully migrated our design from 0.5 μm process to 0.25 μm using radiation tolerant techniques. The circuit performed as expected before and after 33 Mrad. The radiation results presented in this paper, along with our unpublished results from discrete devices, are extremely encouraging. We believe that using commercial deep-submicron processes to address total dose radiation effects is a very viable solution.

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