



The Port Card for the Silicon Vertex Detector Upgrade of the Collider Detector at Fermilab

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Abstract

The Collider Detector at Fermilab is approaching the completion of the Silicon Vertex Detector upgrade for Run II. The Port Card is a Beryllia multichip module developed to control, read out, and regulate power for the silicon strip readout chips. It has two rad-hard Application Specific Integrated Circuits, parallel fiber optic transmitters, and voltage regulators. It resides 14 cm from the accelerator beam inside the tracking volume. The function and location of the Port Card impose severe constraints on its design. This paper presents the Port Card, and describes the adopted solutions to address the main design issues, as well as the result of many characterization tests.

grounding strategy. The PC is installed very close to the beam and it is exposed to high radiation doses. The design parameter used was 200 krad for the planned operation of the card. Furthermore, once the SVXII barrels are installed inside CDF the access for service is very difficult and require substantial down time. This constraint required special considerations regarding the PC's reliability. Finally, the total price of the PC also contributed to limit the set of possible implementations.

The PC will also control and read out CDF's Intermediate Silicon Layer [8] and Layer00 [9] detectors. These two detectors, together with the SVXII, form CDF's silicon tracker upgrade project. The application of the PC controlling and reading out the SVXII is sufficient to describe the PC and the strategies adopted to handle the constraints.

I. INTRODUCTION

The Collider Detector at Fermilab (CDF) is approaching the completion of the Silicon Vertex Detector upgrade (SVXII) for Run II [1,2]. The SVXII is formed by three barrels composed of 12 wedges in each side of the barrel. Figure 1 shows one of the SVXII barrels. A wedge is assembled with five layers of double sided silicon strip detectors (SSDs) [3]. The SSDs are read out through Application Specific Integrated Circuit (ASIC) readout chips, the SVX3 [4], assembled in hybrids [5] bonded to both sides of the SSDs. The pre-amplifier inputs of the SVX3 chips are wire bonded directly to the detector strips. The Port Card (PC) is a Beryllia based multichip module (MCM-C) [6] which sits on the top of the wedge, 14 cm from the beam and inside the CDF detector tracking volume. It communicates with the SVX3 chips through high density interconnect cables (HDIs). The main functions of the PC are control, configuration, and readout of the SVX3 chips, and to locally regulate the analog power supplies. The previous version of the SVX detector also used Port Cards [7].

The PC functions and location impose severe constraints to its design: low mass and size, high radiation dose, reliability, high heat transfer capability, remote control and data transmission, low noise regulated voltage, detector

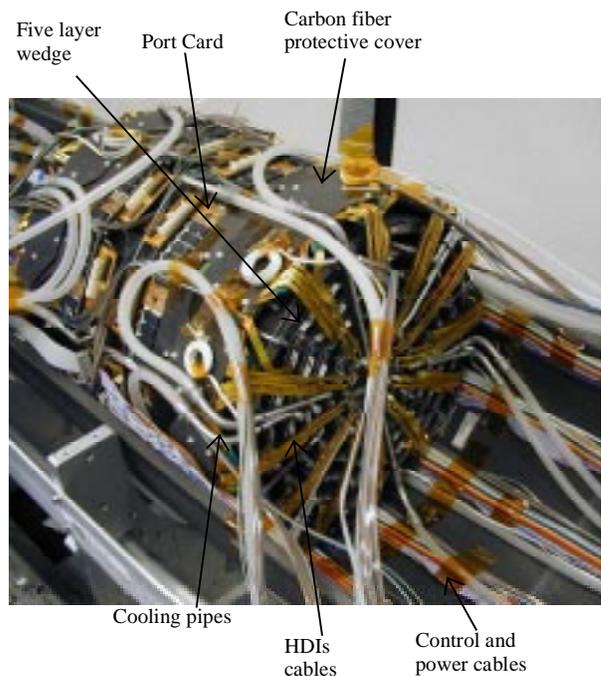


Figure 1. SVXII Barrel

II. FUNCTIONAL DESCRIPTION

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The PC has a digital section which handles all digital operations and an analog section formed by the voltage regulator and the high voltage bias interconnection. Figure 2 shows a picture of the whole assembled PC while Figure 3 shows a close up of the portion dedicated to a specific SVX3 hybrid.

A. Digital Operation

Figure 4 shows the block diagram of the digital section of the PC. The digital section is formed by one Transceiver (TX) chip [10] and five DAC/Decoder/Regulator (DDR) [11] chips. Each DDR is associated with one of the five SSD layers that form the wedge. The five digital power supplies (DVDD) are delivered to the SVX3 hybrids on the SSD layers after capacitive decoupling on the PC.

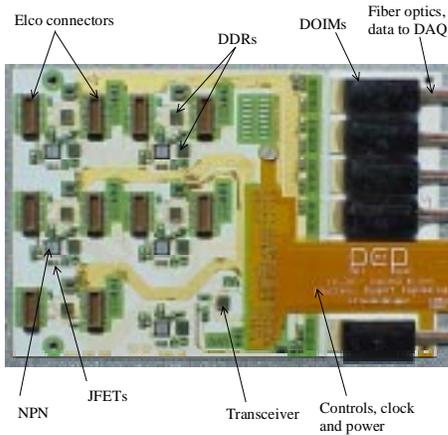


Figure 2. Assembled Port Card

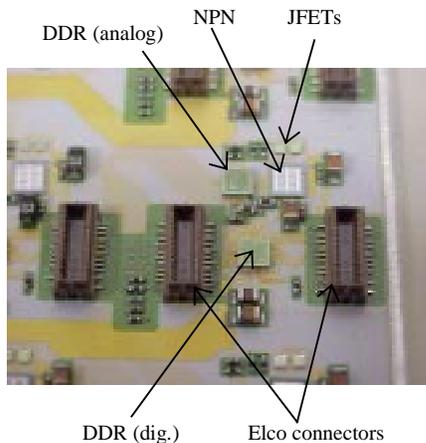


Figure 3. Close Up of the Assembled Port Card

The PC works under the tight control of the Fiber Interface Board (FIB) [12]. The FIB is part of the DAQ and is located approximately 100 feet from the PC and outside the CDF detector. The SVX3 chips are dead-timeless, and as shown in Figure 4, this feature requires different paths for controls and clocks and for data readout. To reduce the number of pads on the SVX3 chip and the complexity of the SSD hybrids, several control signals are single-ended CMOS.

These traces are not impedance terminated. To minimize reflections on these signals on the HDI cables, the PC is assembled close to the SSD layers.

The TX and the DDR are ASICs designed and manufactured using the Honeywell 0.8 μm rad-hard process. The DDR has four major sections: a decoder that decodes the control signals from the data acquisition system (DAQ), and generates the required control and configuration pattern for the SVX3 chip operation, a DAC to generate the analog voltage reference for the charge inject feature of the SVX3 chips, an operational amplifier and voltage reference (V_{REF}) to regulate the analog power for the SVX3 front-end electronics, and buffers for the SVX3 chip clocks. As previously mentioned, each SSD layer has two associated DDR chips: one DDR dedicated exclusively to digital operations and the other just for voltage regulation. This approach was taken to reduce voltage regulator noise as it avoids internal coupling of the digital section of the DDR into the operational amplifier and V_{REF} .

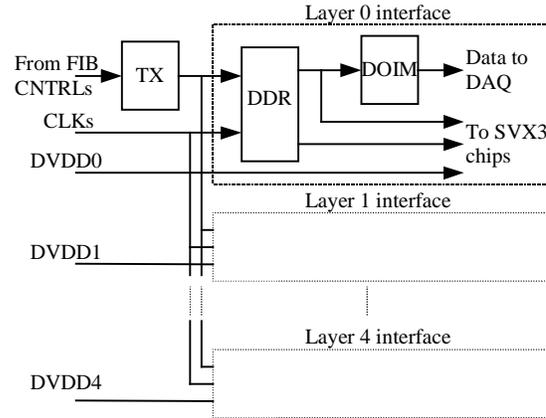


Figure 4. Digital Section

The TX is composed of 10 differential drivers and receivers conforming with an electrical protocol based on adjustable (from 5 to 15 mA) differential current. This protocol has been named low current differential signals (LCDS). On the PC the TX is configured as a receiver. The TX chip receives from the FIB LCDS controls, configuration and clocks, and transforms them to single-ended CMOS. The PC routes these signals to the five DDR chips dedicated to digital operation. The DDRs decode the controls and buffer the clocks. Two ELCO connectors [13] located on both sides of the DDRs (see Figure 3) and the HDIs deliver the decoded and buffered signals to the SVX3 chips.

The SVX3 chips read out the SSD information and transmit it to the PC through the same HDI cable. The electrical protocol of the SVX3 data also is LCDS. The PC routes the data to the Transmitter Dense Optical Interface Modules (DOIMs) [14]. The Transmitter DOIMs are a set of nine LCDS receivers internally connected to nine fiber optic transmitters. They transmit the SVX3 data to the FIB through fiber optics.

An important constraint on the design of the PC is reliability. Access to the SVXII detector and associated electronics is very difficult and not achievable during a run. A standard solution to this constraint is redundancy. However, as it was already described, other constraints like low mass and size precludes the implementation of such an option. A detailed analysis of the SVXII detector shows that, though not desirable, the loss of a single scatter layer does not impose severe performance degradation to the SVXII detector, in contrast to the loss of a full wedge. Therefore, the PC was engineered in such a way that failure of a single DDR set or voltage regulator will affect just the silicon layer associated with those components. The only component on the PC that is common to all layers is the TX chip. This design strategy decreases the probability of losing a full wedge.

B. Voltage Regulators

Figure 5 shows the block diagram of the analog section of the PC. It is formed by a voltage regulator and high voltage bias for the SSDs. The voltage regulators are assembled on the PC itself to keep them close to the SVX3 hybrids. The bias is delivered directly to the hybrids where they are low pass filtered and connected to the SSD.

The voltage regulator uses a standard configuration as depicted in Figure 5. The PC is designed to operate in a high radiation environment. To simplify the selection of components for the voltage regulator, the following strategy was adopted: design the operational amplifier and the voltage reference using Honeywell rad-hard process and select a JFET and power NPN transistor for the high current portion of the regulator.

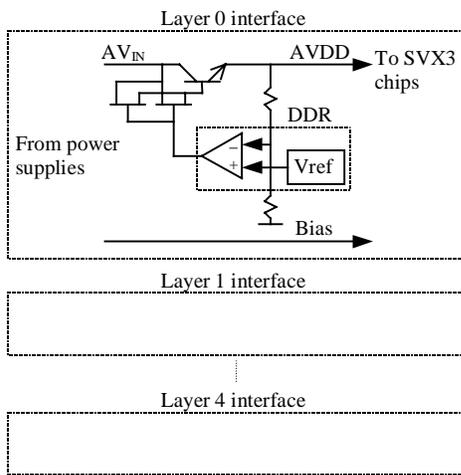


Figure 5. Analog Section

The JFET used is the U291 die from Siliconix. The output of the operational amplifier is capable of operating from power to ground rails when driving very high impedance loads as is the case of the JFET gate. Two JFETs are connected in parallel to allow for larger gain drop of the NPN transistor. Furthermore, the JFETs are quite rad-hard

since electrical fields are used to control the drain current. The JFET dies were wafer probed and selected with more stringent specifications to guarantee full control of the voltage regulator's output current. Samples of the production lot were irradiated up to 1.8×10^{13} protons/cm² (approximately 500 krad) using the 8 GeV Fermilab booster. No gain change was observed, and the gate reserve current increased to 20 nA. When measuring the gain, the temperature of the JFETs were not controlled. Figure 6 shows a typical I-V curve of one of the JFETs after 500 krad.

The NPN carries the high current (about 1.2A for the fourth SVX3 hybrid) portion of the voltage regulator. The NPN transistor used is the chip 185 from Solitron [15]. The two JFETs provide enough current to guarantee proper operation of the regulator even with the NPN gain as small as 10. These NPNs were also fully wafer tested to guarantee more stringent specifications, such as current gain. Samples of the production lot were also irradiated up to 3.6×10^{12} protons/cm² (approximately 500 krad) using a 63 MeV proton beam at UC Davis (CA). The gain of the transistors decreased from 200 to 40, which is still comfortably above the minimum gain supported by the regulator. When measuring the gains, the temperature of the NPNs were not controlled.

Figure 7 shows a typical I-V curve of one of the NPNs after 500 krad. Other radiation exposure tests with another transistor lot resulted in a gain drop to 25. Low radiation dose rate tests have not been done.

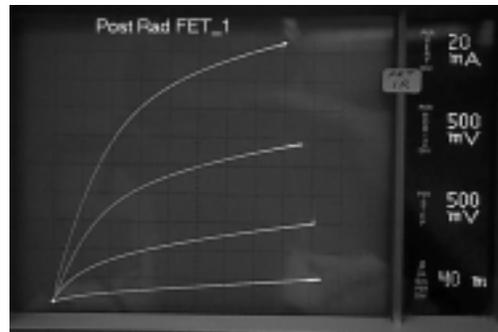


Figure 6. JFET I-V Curves after 500 krad

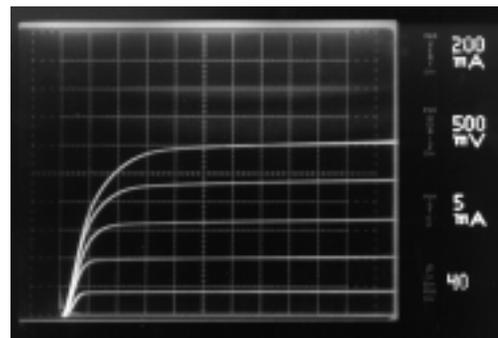


Figure 7. NPN I-V Curves after 500 krad

This design strategy of using of a rad-hard ASIC coupled with the NPN and the JFET allowed for easier design. Only the NPN had to be carefully selected for radiation tolerance. However, a disadvantage of the implemented solution is that the voltage drop over the JFET transistor (V_{ds}) has to be big enough to guarantee that it operates in the saturation region, which considerably increases the power dissipation.

III. MECHANICAL AND THERMAL CONSIDERATIONS

The PC board uses thick film MCM-C technology. The board was manufactured by APTA (San Diego). The PC have printed on the Beryllia substrate three silver layers for power and ground planes, one silver-gold transition layer and four gold trace layers with eight dielectric layer in between. The digital power distribution is laid out on the top trace layer. The wide traces are visible in Figure 2 and Figure 3.

Since the PC is inside the tracking volume, it has a small mass to minimize interference with particle trajectories and a small size to fit in the tight space available. The PC substrate, Beryllia, has very good heat conduction properties coupled with a small radiation length. The PC is about 103 mm long and 70 mm wide with a thickness of 0.5 mm and is very fragile. In order to improve card flatness, some circuitry is included on the bottom side of the PC; moving some of the circuit layers from the top to the bottom of the card reduces bowing resulting from coefficient of thermal expansion differences during cool down from its elevated processing temperature. Vias connect the two sides of the circuitry through holes in the substrate.

Each PC is mounted to a support plate using a small nylon screw in each of the five mounting holes. These support plates are constructed from an open-cell foam core laminated between two skins of carbon fiber yielding a lightweight, low-radiation-length structure with an overall thickness of about 3 mm. Cutouts in this plate accommodate two sections of the cooling channel rings which also provide structural support for a set of 12 cards. Each cooling channel has a rectangular cross-section of about 7 mm wide, providing a large area for heat removal. A layer of thermal grease in the channel areas is used to ensure good thermal contact between the card and the cooling rings. Additional cutouts in the support plates contain small nylon nuts glued in place for the PC mounting screws. Carbon fiber bar clamps located to the right side of the card as it is shown in Figure 2, provide cable strain relief to reduce the risk of damage to the fragile Beryllia substrate.

The DOIMs and the power transistors generate substantial heat, and maintaining a cold environment is an important factor for the temperature-sensitive SSDs located nearby. The Beryllia and the metal thermal vias carry the heat to the cooling channels. The support plate is designed such that one cooling channel passes directly underneath the row of DOIMs, which can generate a total of about 9 W, while the other passes underneath a field of thermal vias centered 21 mm from the left edge of the PC. The thermal vias, which occupy 1% of the bottom-side dielectric in this area, reduce the thermal resistance between the Beryllia substrate and the

cooling channel. The thermal vias provide about a 2°C reduction in the PC temperatures in this region. No dielectric is present on the bottom of the PC in the DOIM region allowing a more direct thermal path between the Beryllia and the cooling channel. The total power dissipation including the voltage regulators and DOIMs is smaller than 15W.

IV. GROUNDING AND POWER DISTRIBUTION

The PC is an integral part of the SVXII detector power distribution and grounding system. Each SSD layer requires one digital voltage (DVDD), one regulated analog voltage (AVDD), and two high voltage bias supplies. These four voltages form a power supply set. The PC connects five power supply sets to each one of the SVX3 hybrid layers that form a wedge. The PC is designed in such a way that any power supply set can be turned off without affecting the operation of the other remaining hybrids. This feature is designed to handle possible failures that may require turning off one specific hybrid. As it was stated before, the loss of a single scatter layer does not impose severe performance degradation to the SVXII detector.

Power and detector bias arrive at the PC through a flat ribbon cable and a flex pigtail. A portion of the pigtail is shown in Figure 2. All power supplies, including the bias, implement floating grounds. To minimize the complexity of the ground scheme, all digital grounds (associated with DVDDs) are connected together on the PC in just one digital ground plane (DGND). Figure 8 shows a simplified sketch of the grounding configuration with just two analog ground planes (AGND). The PC implements five different analog ground planes (associated with AV_{IN}) which are not connected with the digital ground until they reach the SVX3 hybrids. The same approach was adopted for the bias voltages which are not depicted in Figure 8. On the SVX3 chip hybrids, all grounds (including bias, analog and digital grounds of the five SVX3 hybrids) are connected together through the detector bulkhead. The small digital ground loops formed by the different HDI cables, the bulkhead and the PC common digital ground have not shown performance degradation of the detector. The whole detector is connected to safety ground in just one place.

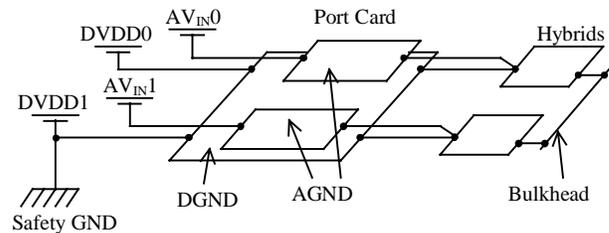


Figure 8. Grounding

The capacitance between traces, power, and ground planes can be substantial in the MCM-C technology. This is due to the small thickness and associated big dielectric constant (typically between 5 and 9) of the dielectric materials. In order to minimize the capacitance between the digital and analog ground planes, and therefore, minimize the ground loop for high frequency AC noise, the analog power

and ground are laid out on the bottom side of the PC, increasing the distance between these two types of planes. Furthermore, each one of the five analog power and ground planes are laid out just under the DDR and power transistors which decreases the area that the digital and analog planes overlap. This intended feature decreased the capacitance between these two type of planes (as much as six times).

V. PERFORMANCE AND IRRADIATION TESTS

The SSD noise performance when operating with the PC is very good. The SSD noise when a test DAQ reads out the SVX3 chips and when the PC reads them out has been measured. Both measurements are comparable. Furthermore, when the PC controls a full wedge, the noise of the SSD layers is similar to the noise of each one of the layers operating independently.

The total radiation dose expected for the PC is 162 krad. To include a safety margin, the PC was designed to support 200 krad. The type of radiation will be mostly pions (about 60%) and kaons (20-30%). The remainder will be protons, anti-protons and anti-neutrons. The energy on average will be close to 500-800 MeV. Two fully operational PCs were irradiated at UC Davis, one with 200 krad and the other with 400 krad. They were characterized after irradiation:

- a) Both PCs continued to be fully functional.
- b) The DOIM power consumption remained unchanged, but the DOIM laser light output decreased by 13% and 20% after 200 and 400 krad exposure respectively. This can be compensated for by externally increasing the voltage drop across the laser diode. The optical power incremented by 55 mW per 0.1V before exposure, 51 mW after 200 krad and 44 mW after 400 krad.
- c) The DDR DAC calibration voltage slope did not change after 200 krad. The voltage of each DAC configuration changed by 1 to 3 mV after 400 krad.
- d) The analog voltage regulation continued working, even after 400 krad.
- e) Any shift on the SVX3 pedestals was not measured. Also, the noise performance continued to be the same.

This irradiated PC is currently being used for long term reliability testing with resistive loads. After two months of operation, no failure was detected. Furthermore, several PCs are being extensively used to test and characterize production quantities of SSD layers. The PCs have been very reliable.

VI. CONCLUSIONS

Presently all PCs for the CDF silicon detector upgrade have been produced and are being installed on the barrels. The design strategies adopted to handle the constraints associated with this project have been extensively tested and very good performance has been measured. The SVXII operation is scheduled to start in March 2001.

VII. ACKNOWLEDGMENTS

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