

# Flex Circuits for the ATLAS Pixel Detector

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## Abstract

Recent progress on designs of low-mass, flexible circuits for the ATLAS pixel detector will be discussed. Thin flexible circuits can be used to provide power and signal connections between front-end readout chips and data acquisition chips on the 2 cm by 6 cm ATLAS pixel detector module. Layouts and SPICE simulations will be presented for such circuits based on non-standard printed circuit board design rules. Test results from circuits fabricated for other applications using similar design rules will also be presented.

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## 1 Introduction

An array of hybrid pixel detectors is being developed for use at the Large Hadron Collider (LHC) by the ATLAS collaboration. The detector layout consists of three barrel layers, and five disk layers at each end. Each pixel module has sixteen front-end (FE) chips bump-bonded to a single sensor. One module design option utilizes a thin flexible circuit (Flex Hybrid) which is mounted on the back of the sensor to provide interconnections for power and digital signals between the FE chips, a Module Clock and Control chip (MCC), and an optical link which are mounted on it. Wire bond pads on the edge of the hybrid will be used to connect power and signal lines to corresponding wire bond pads located on the FE chips, which extend beyond the edge of the sensor. The module is 2.14 cm wide and 6.24 cm long. This conceptual module design is illustrated in Figure 1. Several possible designs for the Flex Hybrid are presented here along with results of simulations of expected performance.

## 2 Flex Hybrid Designs

Minimizing mass in the active tracking volume is of crucial importance in obtaining the optimum physics performance of the ATLAS detector. We are therefore required to use thin (flexible) substrate and metal layers in design of the Flex Hybrid. Flexible printed circuit technology typically uses film substrates such as Kapton with a minimum thickness of 25  $\mu\text{m}$  containing patterned surface metal layers with or without cover insulating layers (passivation). Plated through via's can be used to connect traces in different layers. Many vendors use "standard" design rules allowing minimum trace widths

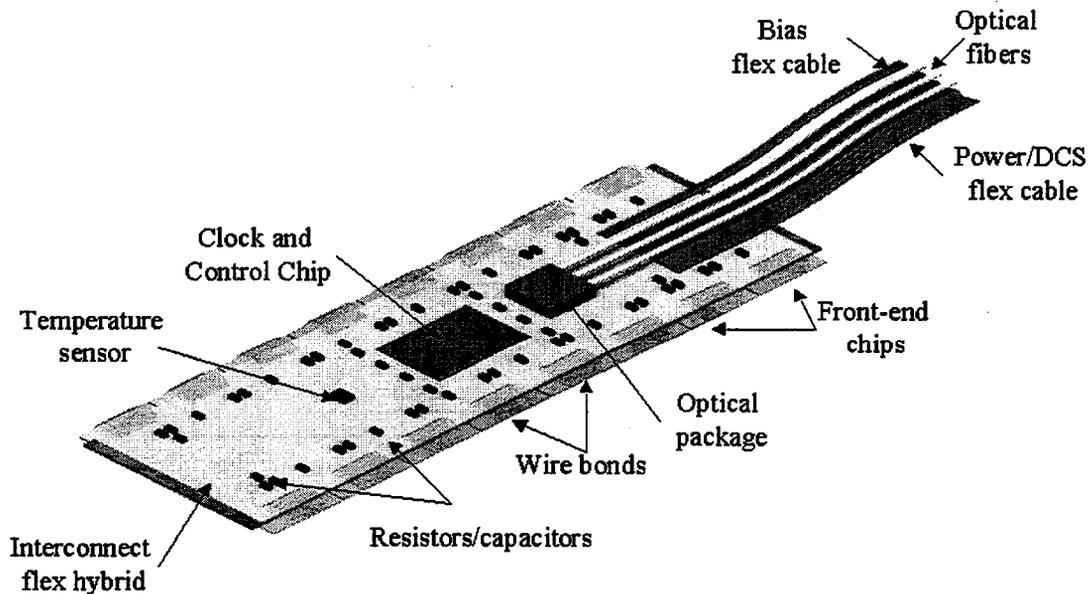
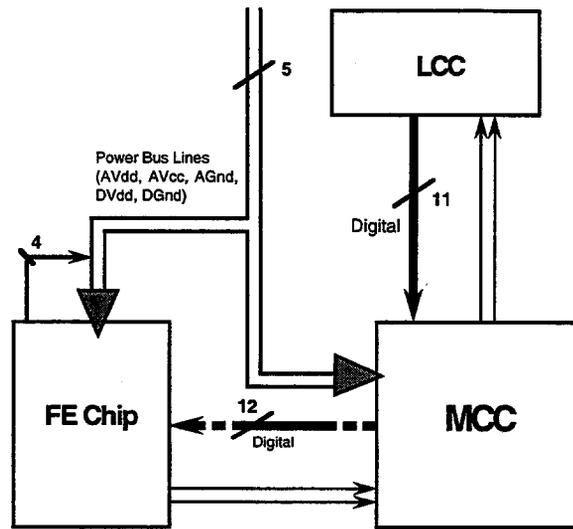


Fig. 1. Conceptual design for an ATLAS pixel module. The module is 2.14 cm wide and 6.24 cm long.

and spaces of  $100\ \mu\text{m}$ ,  $400\ \mu\text{m}$  via cover pads, and  $200\ \mu\text{m}$  via through holes. Several vendors have developed High Density Interconnect (HDI) processes which can attain smaller feature sizes. For example the General Electric Corporate Research and Development (GECRD) HDI process can achieve  $30\ \mu\text{m}$  trace widths and spaces,  $75\ \mu\text{m}$  via cover pads, and  $25\ \mu\text{m}$  via through holes.

In the designs to be described here, the optical link has been replaced by an off-module Ladder Control Chip (LCC). The required signal and power connections between the FE chips, the MCC chip, and the LCC which are provided by the Flex Hybrid are illustrated in Figure 2. Low Voltage Differential (LVD) lines are used for the digital signals. "Broadside coupled" lines

## Block Diagram of Signal Connections



MCC : Module controller chip  
LCC : Ladder controller chip.

Fig. 2. Block diagram showing the signal and power connections required to be made by the Flex Hybrid.

with paired differential signals on opposite sides of a substrate layer were used whenever possible, particularly in designs using the standard design rules. In designs using HDI rules, it was often necessary to use co-planar paired differential lines in order to minimize the number of metal layers. The maximum current specifications for the FE chips were 25 mA for 3 V analog power, 50 mA for 1.5 V analog power, and 30 mA for 3 V digital power. The maximum current specification for the MCC chip was 100 mA for 3 V digital power. A maximum voltage drop of 100 mV was allowed in the power (and ground) lines over the length of the module.

The LHC beam crossing frequency is 40 MHz which is also the clock frequency for the pixel readout chips. Typical 40 MHz square waves have large-amplitude frequency components near 40, 80, and 120 MHz with smaller components at higher harmonic frequencies, so crosstalk and attenuation must

be minimized for frequencies up to several hundred MHz.

A complete layout was done assuming prototype (demonstrator) designs for the FE and MCC chips using standard design rules. (It is also based on an older module design which had 12 FE chips per disk module.) It was found that six metal layers were required to make the necessary connections. This hybrid was over 300  $\mu m$  thick and did not meet the material budget constraints for the pixel module. We were then motivated to use a two-piece approach in which routing near the MCC is done on a separate flex circuit called the MCC Mount (MCCM) using the HDI rules. The MCCM is then mounted on a Flex Hybrid which is designed using standard rules. This approach has the advantage that each flex circuit required only two metal layers and the overlap area is minimized. Wire bond connections must be made to connect the two flex circuits. The layout of the Flex Hybrid is shown in Figure 3 and the layout of the MCCM is shown in Figure 4.

### 3 Performance Simulations

To estimate the performance of the flex hybrid designs, a transmission line analysis including calculation of attenuation and crosstalk was performed using the commercial software package Maxwell Spicelink [1]. This package does a finite-element calculation of electric and magnetic fields using the multipole method in order to extract the resistance, capacitance, and inductance of conductive circuit elements. The RCL values obtained can then be loaded into SPICE so that the circuit performance can be simulated.

In order to verify this method, a simulation was first done on an existing flex circuit of relatively simple geometry which was developed for the CLEO III

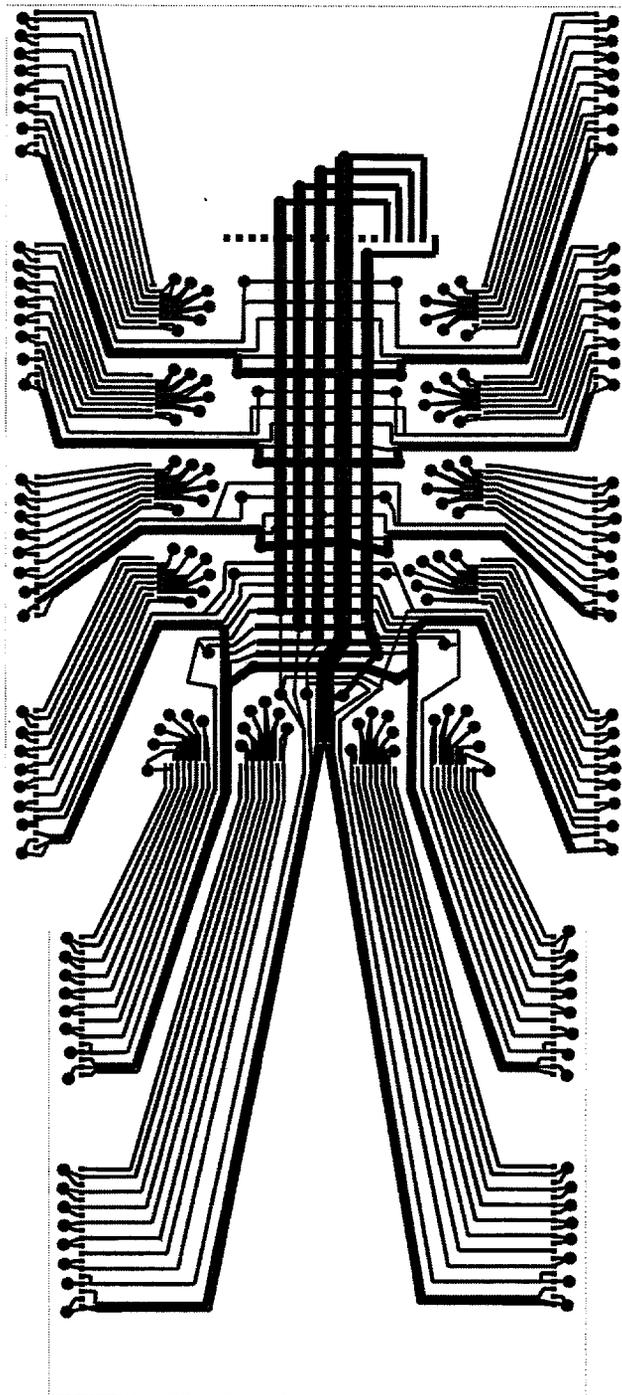


Fig. 3. Layout of the two metal layer Flex Hybrid using standard design rules.

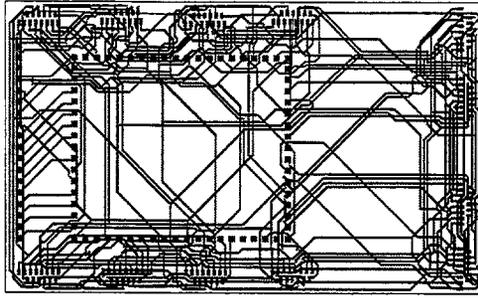


Fig. 4. Layout of the two metal layer MCCM using HDI (GECRD) design rules.

silicon microstrip detector [2]. We have established a collaboration between the University of Oklahoma and GECRD to develop the CLEO III flex circuits based on their existing high density interconnect process [3]. The flex design uses two metal layers patterned with traces on either side of a  $25\ \mu\text{m}$  Kapton substrate. Each side is coated with a layer of acrylic passivation  $12.5\ \mu\text{m}$  thick except for the area on top where wire bond pads are located. Traces are  $30\ \mu\text{m}$  wide and are made of  $6\ \mu\text{m}$  of Cu,  $0.7\ \mu\text{m}$  of Ni, and have  $1.0\ \mu\text{m}$  Au plating. A thin layer of Ti is sputtered on the Kapton before the Cu is applied to improve the adhesion of the Cu layer. The top layer (defined by the presence of bond pads) has 255 traces and the bottom layer has 256 traces. Via's with  $25\ \mu\text{m}$  square plated-through holes and  $75\ \mu\text{m}$  square cover pads are used to connect the bottom traces to bond pads on the top side. Bond pads are typically  $170\ \mu\text{m} \times 60\ \mu\text{m}$ .

The process, which is proprietary, uses a direct-write laser rather than conventional lithography to expose resist and thereby form the patterns. The laser is also used to construct the via holes through layers of Kapton. The total trace capacitance has been measured to be  $< 1\ \text{pF}/\text{cm}$  and the trace resistance has been measured to be  $< 1.2\ \Omega/\text{cm}$ . The rate for defects such as non-continuous traces and shorts has been determined to be  $< 0.1\%$  of all traces with about 50% of the circuits containing no defects [4]. Wire bonding

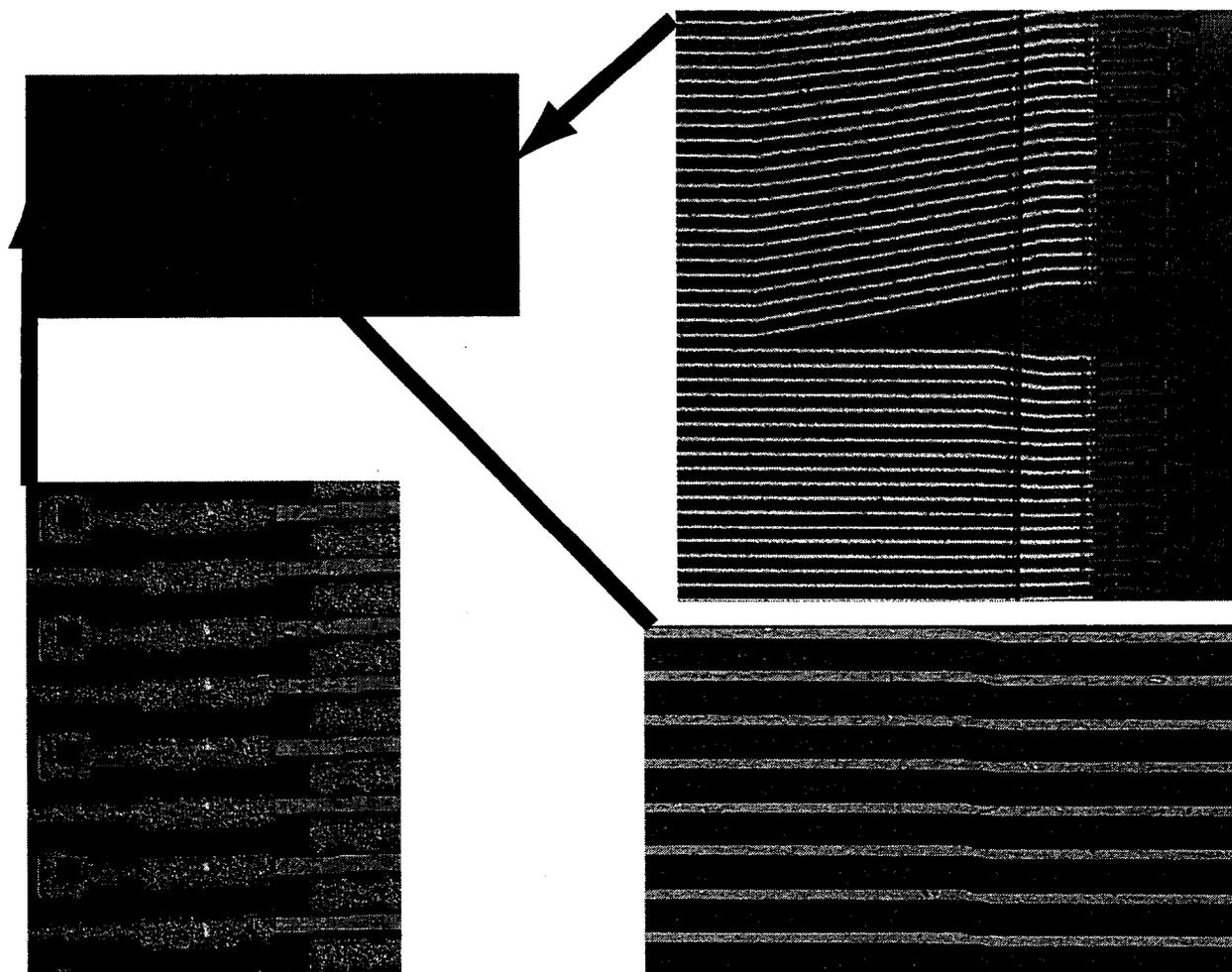


Fig. 5. Photographs of several key regions of a CLEO III production flex circuit.

to the flex circuits can be done easily with reasonable pull-strengths. The flex circuits are fabricated in a “frame” consisting of a single layer of Kapton stretched over a 17.5 cm inner diameter metal ring. A typical production flex circuit is shown in Figure 5. This process meets all the requirements for fabrication of the ATLAS MCCM design.

Simulation of the transmission line properties of a portion (up to seven traces) of the CLEO III flex circuit was done using the Maxwell Spicelink package and the results were compared to measurements. The method and results

are described in detail in Ref. [5]. The Maxwell Extractor uses finite element analysis and the multipole method to extract RCL matrices for 3-dimensional structures and discontinuities. The extracted quantities can be exported directly in matrix format, or can be used to automatically generate SPICE models. In the simulation, a square wave clock signal with 2 ns rise and fall times was used as input to one ("active") trace. The attenuation (output voltage/input voltage) on opposite ends of the active trace and crosstalk (output voltage on neighboring trace/input voltage on active trace) were determined from the SPICE simulations as a function of clock pulse frequency. All traces were terminated by 50  $\Omega$  resistors although the expected characteristic impedance of the CLEO III geometry is expected to be  $> 150 \Omega$ . This mismatch in impedance made the crosstalk and attenuation larger and easier to measure.

The attenuation and crosstalk were measured using a microprobe station and an HP 4194A impedance phase/gain analyzer. The measurements were dominated by noise for frequencies below 100 Hz and above 10 MHz. Figure 6 shows the minimum portion on the CLEO III flex circuit used in the simulations. Figure 7 shows the attenuation (in decibels) obtained from the simulations and Figure 8 shows the crosstalk on the nearest neighbor on the opposite side of the flex circuit. The X's in Figures 7 and 8 show the results of the measurements. Reasonable agreement is obtained between the simulations and measurements for frequencies between 100 Hz and 1 MHz where the measurements are most reliable.

Sections of the Flex Hybrid and MCCM designs were also simulated using the same methods as for the CLEO III flex circuit. A typical section of the Flex Hybrid is shown in Figure 9. In this case, LVD signal high is applied to

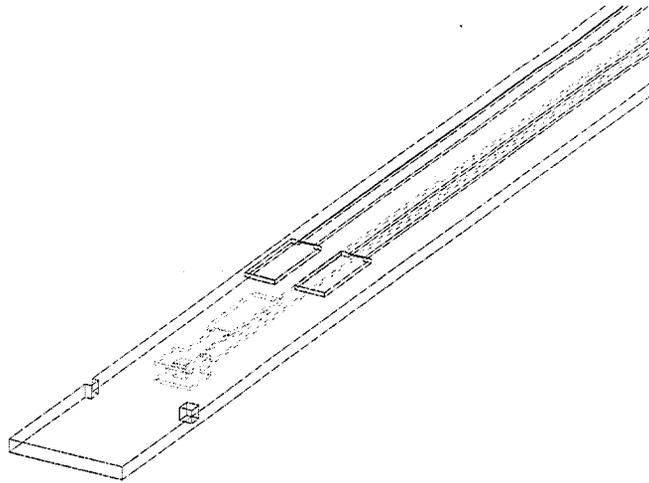


Fig. 6. The minimum portion on the CLEO III flex circuit used in the simulations.

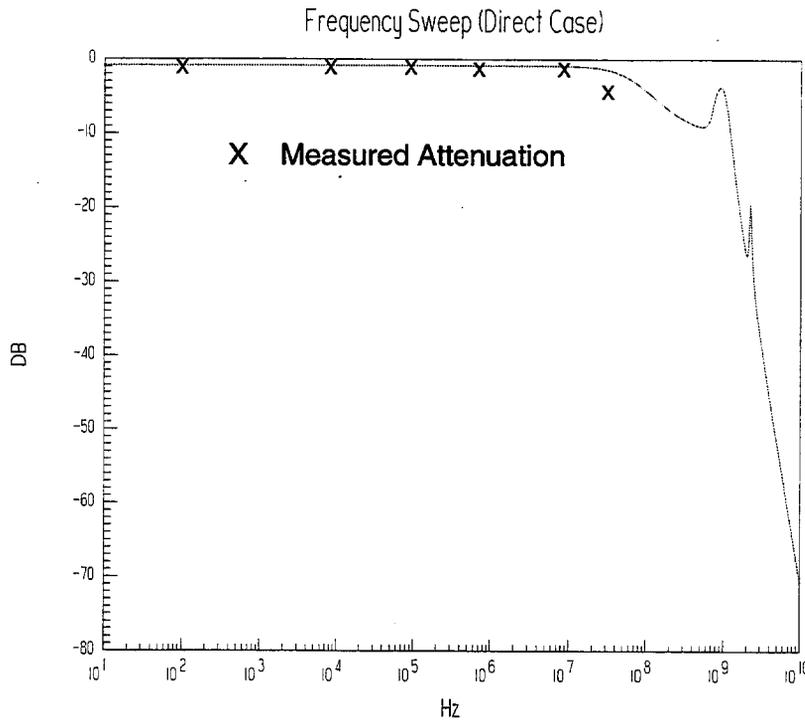


Fig. 7. The attenuation obtained from the simulations. The X's show the results of measurements.

the active trace and LVD signal low is applied to the trace on the opposite side of the two layer Flex hybrid. All traces are assumed to be terminated with  $100 \Omega$  resistors at both ends. Typical simulation results for the input and output (on opposite ends) for a 40 MHz clock pulse for signal high are

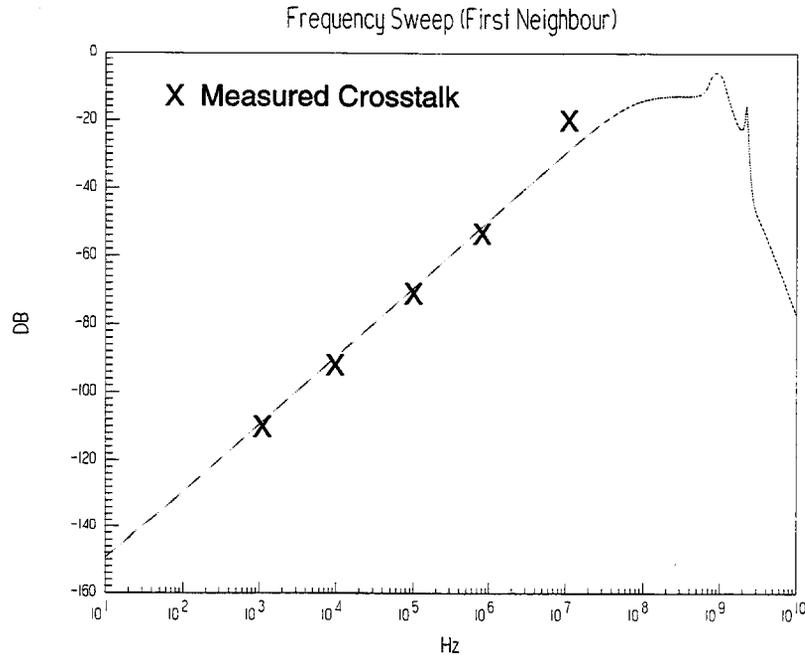


Fig. 8. The crosstalk on the nearest neighbor trace on the opposite side obtained from the simulations. The X's show the results of measurements.

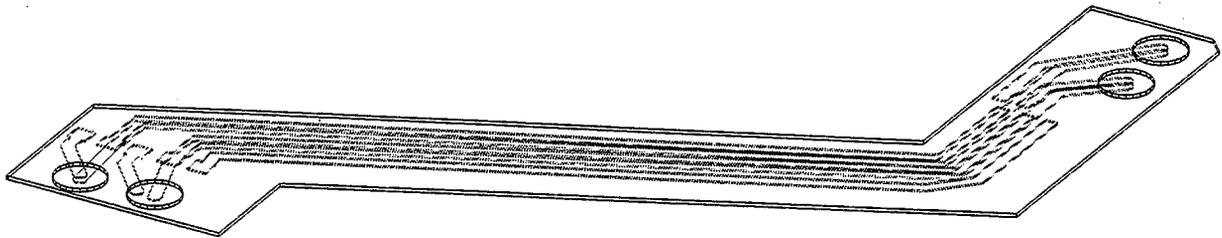


Fig. 9. A typical section of the two metal layer Flex Hybrid used in the simulations.

shown in Figure 10. The frequency dependence of the crosstalk on the nearest neighbor (same side) trace is shown in Figure 11.

A typical section of the MCCM is shown in Figure 12. Square wave clock signals were applied to the LVD high and low signal pairs as in the case of the Flex Hybrid. The MCCM has mostly co-planar LVD lines. Simulation results for the attenuation and nearest neighbor crosstalk as functions of frequency are shown in Figure 13. Figure 14 shows the phase change relative to the

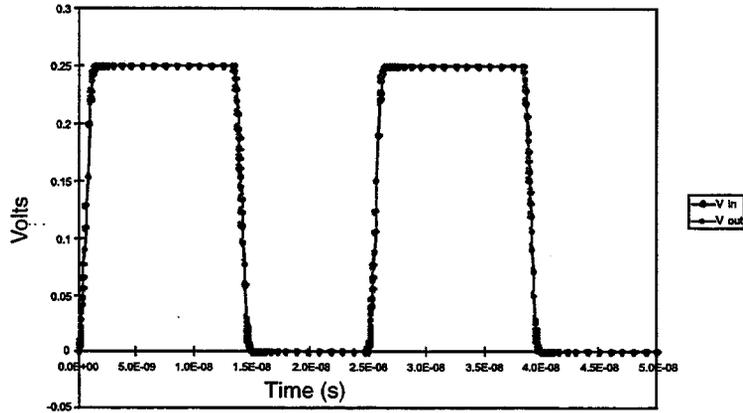


Fig. 10. Simulation results for the input and output (on opposite ends) for a 40 MHz clock pulse for LVD signal high on a Flex Hybrid trace.

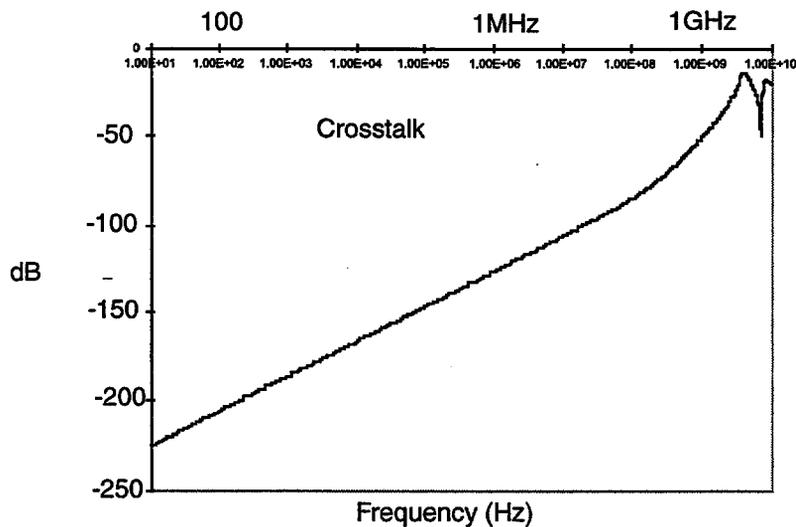


Fig. 11. Simulation result for the frequency dependence of the crosstalk on the nearest neighbor Flex Hybrid trace for LVD signal high.

generated clock phase for the active and crosstalk signals versus frequency. A large variation of phase change is observed above 5 GHz when the wavelength of the input pulse approaches twice the length of the trace as expected. Qualitatively similar results are obtained when portions of the Flex Hybrid and

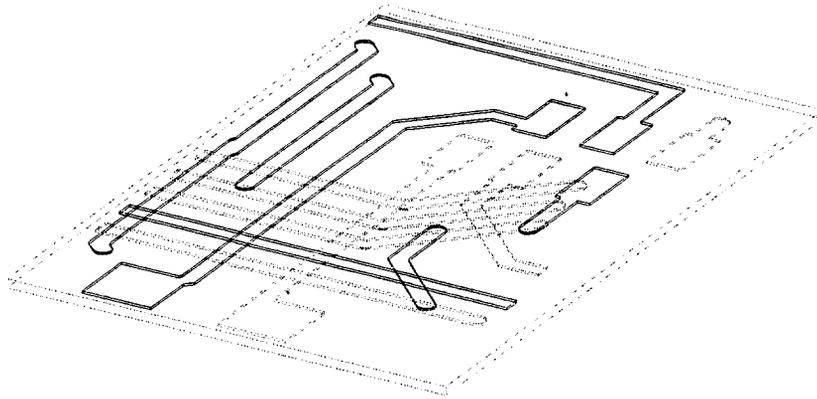


Fig. 12. A typical section of the two metal layer MCCM used in the simulations.

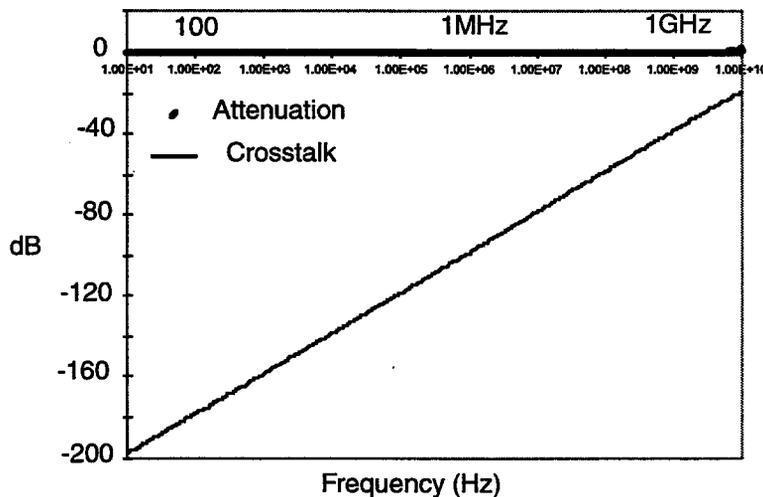


Fig. 13. Simulation results for the frequency dependence of the attenuation of the MCCM active trace and crosstalk on the nearest neighbor trace for LVD signal high.

MCCM are simulated simultaneously.

The simulation results for the two layer Flex Hybrid and MCCM show that the crosstalk on the nearest neighbor is less than -40 dB at 1 GHz and less than -60 dB at 40 MHz. Signal attenuation is negligible up to 500 MHz. Encouraged by these results, we have designed a prototype Flex Hybrid for fabrication as described in the next section. Evolution of the disk mechanical

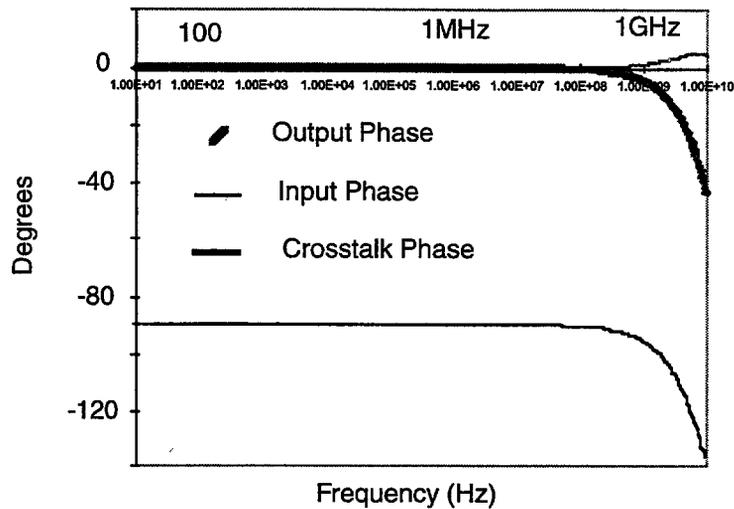


Fig. 14. Simulation results for the frequency dependence of the phase change of the MCCM active trace and the nearest neighbor trace for LVD signal high.

design has led to a solution which allows the same pixel module to be used in both the barrel and disk regions. The two metal layer monolithic Flex Hybrid described below can be used on this pixel module which was shown in Figure 1.

#### 4 ATLAS Prototype Flex Hybrid

A prototype hybrid has been designed which will allow performance tests to be made in the CERN test beam. The prototype hybrid consists of a Kapton substrate with a thickness between 25 and 50  $\mu m$  and with metal traces on both sides. Signal and power lines connect the wire bond pads at the edge of the module to wire bond pads near the MCC. The bottom traces are connected to the traces and bond pads on top with via's which have 70  $\mu m$  diameter holes and 130  $\mu m$  diameter cover pads. Both sides of the hybrid can be covered with a passivation layer except for the areas where bond pads are located. Power and ground lines as well as differential signal lines are placed

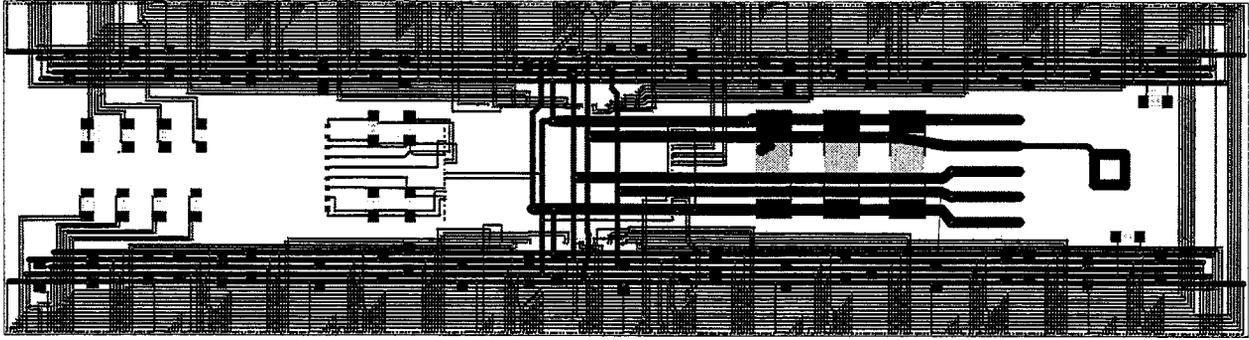


Fig. 15. Layout of both sides of the complete prototype Flex Hybrid.

parallel to each other on the same metal layer. Typical signal traces are  $75\ \mu\text{m}$  wide with  $75\ \mu\text{m}$  spaces between them. The Flex Hybrid also has passive components mounted directly on it including 12 termination resistors and 51 decoupling capacitors, although the number of decoupling capacitors may be reduced based on empirical testing. The present design calls for 0402 form factor SMD's (Surface Mount Device) for the discrete components, except for 3 tantalum capacitors, which are EIA size A. Figure 15 shows the layout of both sides of the complete prototype hybrid. The wire bond pads at the edge which allow connection to the FE chips have a pitch of  $150\ \mu\text{m}$ .

We are actively exploring options with several vendors including the one used for the flex connectors for the CLEO III project (GECRD), Dynamics Research Corporation (Wilmington, MA), and CERN. The first prototype will have Cu traces approximately 6 microns thick, with a barrier metal (e.g., Cr or Ni) and Au plating for the bond pads which is the same as that used for CLEO III. However, CERN has the capability to manufacture flex circuits with Al traces and that option will also be pursued.

## 5 Conclusion

Flex circuit designs have been made which provide required pixel module interconnections between front-end and module control chips and allow mounting of passive components such as decoupling capacitors and termination resistors. Material constraints favor high density, non-standard design rules which allow the routing to be done in two metal layers. Simulations indicate that the designs meet signal integrity requirements. Fabrication of a prototype Flex Hybrid during the next several months will allow full characterization of a complete pixel module during high energy beam tests.

## 6 Acknowledgments

I would like to thank my ATLAS colleagues for help in preparing this presentation. I also thank the organizers of Pixel '98 for a very enjoyable and productive workshop. This work is supported by the U. S. Department of Energy.

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# CMS Forward Pixel Port Card: A Smart Interface between Pixel Readout and DAQ

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## **Abstract**

To coordinate the data acquisition of many pixel readout chips for the CMS Forward Pixel Detector, there will be a local, high-speed interface located relatively close to the readout chips. This interface, known as the Port Card, handles environmental monitoring, houses optical couplers for data transmission, and issues slow control commands to the pixel readout chips. One special function of the Port Card is to prevent data corruption due to sudden trigger overload conditions.

# Overview of CMS Forward Pixel Tracker and Port Card

The CMS Forward Pixel Tracker consists of 2 modular disks of pixel detectors mounted on each side of the interaction region. Each disk is divided into sectors with 24 "blades". Each blade has sensors with attached readout chips mounted on both sides of the blade. There are approximately  $12 \times 10^6$  pixels bump-bonded to 4,320 readout chips. A 15 cm long high density interface cable (HDI) handles the data, low voltage, slow control signals and readout sequencing lines from the readout chips (ROCs) to a Port Card.

The local control of the CMS Forward Pixel Tracker will be provided by the Port Card. This is a low-mass PC board that will be situated at the outer radii of each blade. It will interface the front-end Readout Chips (ROC's) with the Front End Digitizer (FED) and the Front End Controller (FEC) modules of the CMS DAQ System. There will be two Port Cards per blade; one card controlling the entire side of a blade. The Port Card and its associated electronics provide the following functions:

- send phase adjusted Clock and Level 1 Trigger signals to the Readout Chips
- send slow control signals (set pixel thresholds, enable/disable readout, calibration, etc.) to the Readout Chips
- monitor the temperature, bias current and low voltage levels of each blade
- provide a location for the optical link transmitters which will send the analog pixel data (pulse height, address and event number) via optical fiber to the Front End Digitizer
- distribute the sensor bias voltages
- issue hardware resets to the Readout Chips
- manage the readout by initiating and terminating a readout token pass
- temporarily suspend readout if there is a local trigger pile-up
- write Start of Frame and End of Frame records to the FED for each token pass

## Port Card Design Details

The Port Card consists of the following major components: a Communications Control Unit (CCU), a Phased Locked Loop (PLL), a Detector Control Unit (DCU), four Token Bit Managers (TBM's) and a set of four optical-link drivers and laser transmitters. These are shown in a layout diagram of the Port Card in Figure 1. The CCU, DCU and PLL are custom ASIC's that are currently under design and development by the CERN/ECP division for the CMS Tracker.[1, 2] The TBM, on the other hand, is a custom chip that must be developed specifically for the CMS pixel system for use by both the disks and the barrel. The optical links are under development by the CERN/ECP division and will also be used by the CMS trackers and calorimeters for transmitting data.[3, 4, 5] All components must be radiation hard.

At the Port Card, there will be one Token Bit Manager and one optical driver for each HDI cable. Upon receipt of a Level 1 trigger, the TBM will send a token bit down the HDI

which will be passed along among a group of front end chips. Upon receipt of the token bit, each chip will send its data directly to an optical-link driver via a data line on the HDI. Once a Readout Chip receives the token bit, the readout is automatic with no further intervention required.

Below, we describe each of the four custom ASIC's needed for the Port Card.

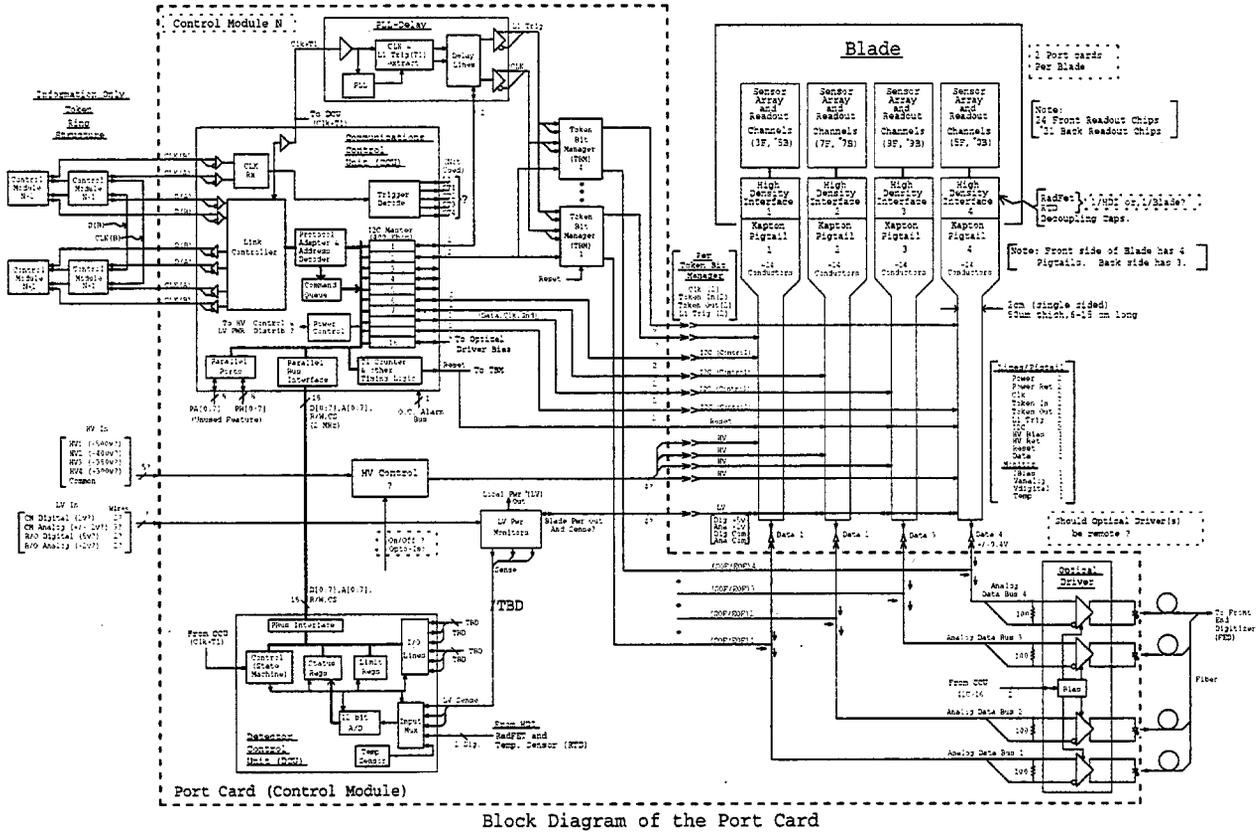


Figure 1: Block diagram of the port card

## Communication Control Unit (CCU)

The CCU ASIC is the master control unit. It performs the following functions:

- receives control commands from the Front End Controller (FEC)
- receives the Clock and Level 1 signals from the FEC
- issues slow control commands to the Readout Chips
- issues control commands to the TBM
- interfaces to the PLL and DCU
- sets the threshold bias of the optical-link drivers.

The CCU communicates with the DAQ via a token ring structure shown in figure 2. It communicates the slow control signals to both the TBM and to the Readout Chips via I<sup>2</sup>C

## CMS Token Ring Structure

(with Secondary Redundant Path to Improve Reliability)

<http://www.physics.rutgers.edu/hex/cms>

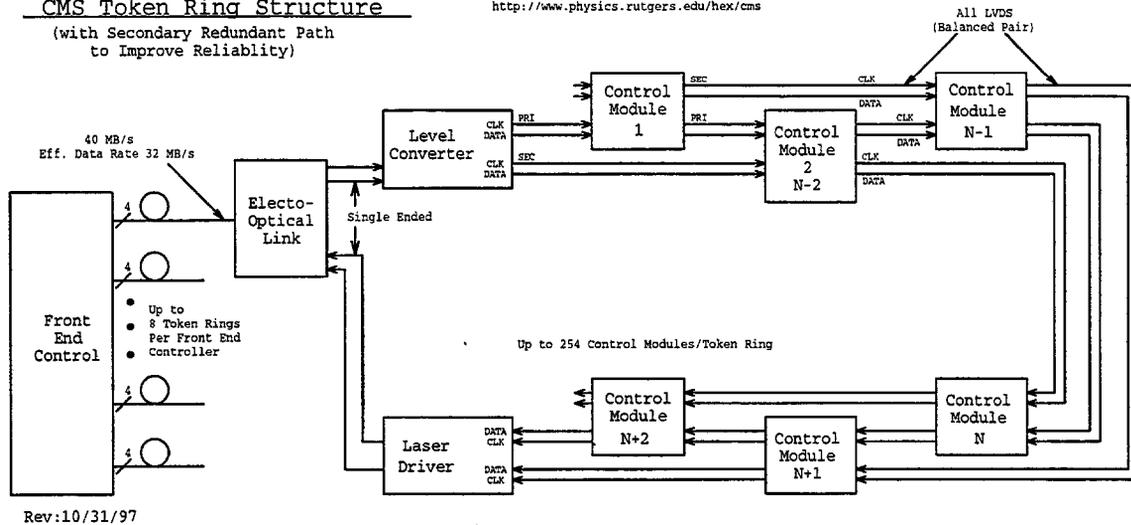


Figure 2: CMS Token Ring Structure

ports which is an industrial bus standard used for slow control. As currently designed, the CCU contains 16 I<sup>2</sup>C master ports which are more than the number needed for the Port Card functions as indicated in figure 1.

## Detector Control Unit (DCU)

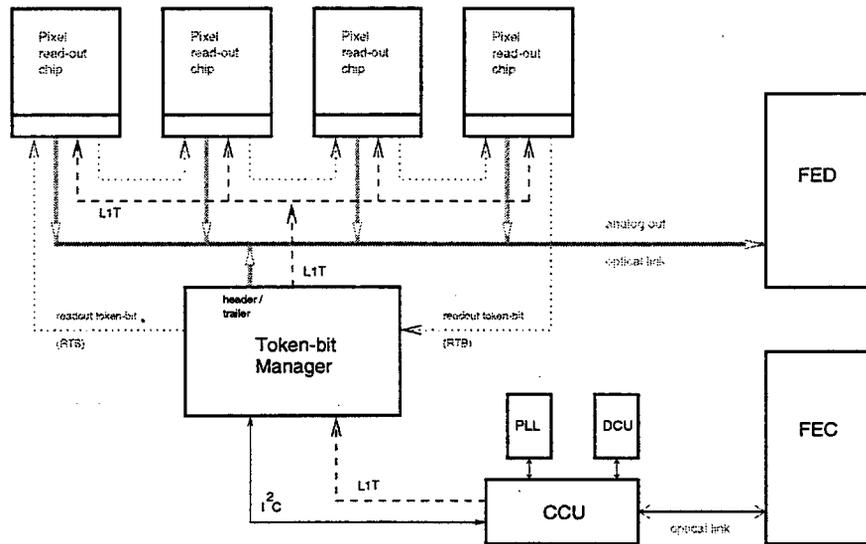
The DCU ASIC will have the function of receiving input monitoring signals and issuing alarms if these inputs exceed certain specified ranges. For the forward pixel disks, the DCU will monitor the temperature, low voltage levels and bias current of each plaquette. The chip will be designed and developed for use by the entire CMS tracking system. Although the design of this chip is not finalized, it is envisioned that it will contain a 12-bit ADC which can address several sources via an input multiplexer. There will be an internal state machine that will perform repetitive measurements on selected inputs signals and compare them with a set of limit registers. When one of the monitored inputs exceeds the set limits, an alarm will be sent to the external FEC via the CCU. The DCU will communicate with the CCU via a parallel bus interface.

## Phase Locked Loop (PLL)

The PLL ASIC will supply phase-adjusted Clock and Level 1 trigger signals to the readout chips. It receives a signal from the FEC via the CCU consisting of a coded Clock plus Level 1 signal. It decodes this signal and separates the Clock and Level 1 signals onto two separate lines and sends them to each of the four Token Bit Managers for distribution to the ROCs. The timing phase of the Clock and Level 1 are set by a programmable delay. The Clock output can be shifted in steps of 1 ns and the Level 1 signal can be shifted in multiples of the clock period.

## Token Bit Manager (TBM)

The TBM is a custom ASIC that needs to be specially made for the pixel systems (both barrel and forward pixel detectors). Its primary function is to manage the local readout by initiating a token bit pass among a group of Readout Chips when a Level 1 trigger is received and by monitoring the return of the token bit. It is needed to deal with the situation in which the readout of a local area of the detector is momentarily not able to keep up with the trigger rate due either to a locally large concentration of hits due to jet events or local noise hits. A separate function of the TBM will be to write the Start of Frame and End of Frame data records for each data stream associated with a token bit pass. It will also keep track of the event number and pass this information to the DAQ in the Start and End of Frames.



Pixel Read-Out Using Token-Bit Manager

Figure 3: Pixel read-out using the Token-Bit manager.

A schematic of the TBM is shown in figure 3 and a functional block diagram is shown in figure 4. Upon receipt of a Level 1 trigger from the PLL the TBM will:

- increment a 6-bit event counter
- increment a trigger stack.

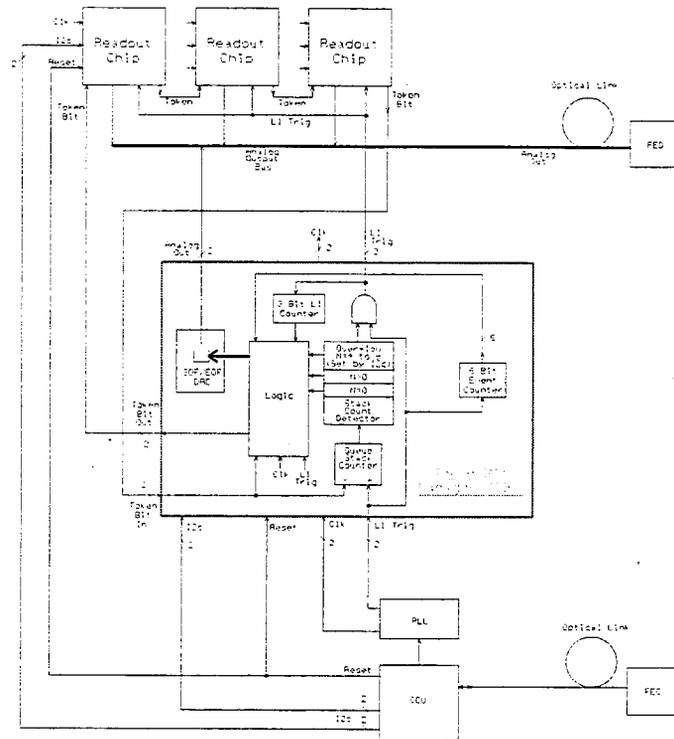
If the trigger stack is not full (less than 8), it will then:

- issue the Level 1 trigger to the group of readout chips
- increment a 3-bit trigger counter
- wait until all previous queued readout is finished

- write a Start of Frame header on the data line
- issue a readout token bit to the Readout Chips.

When a readout token bit returns, it will:

- write an End of Frame record on the data line.



Rev 1 4/30/98

Token Bit Manager Detail  
Forward Pixel Block Diagram

<http://www.physics.nyu.edu/~fews>

Figure 4: A diagram of the readout subsystem detailing the Token Bit Manager.

The format of the Start of Frame and End of Frame records is not yet specified. However, these records will contain both the current 6-bit event counter and the 3-bit trigger counter. Each of the Readout Chips will also contain 3-bit trigger counters which are incremented whenever they receive a Level 1 trigger from the TBM. The contents of the Readout Chip trigger counters will then be identical to the contents of the trigger counter in the TBM. When a readout chip writes its data, it associates the data with a particular trigger by writing the trigger counter as a 3-bit coded analog signal. By reading the Start of Frame header, the FED can then unambiguously associate the 3-bit trigger number received from

the Readout Chip with the global 6-bit event number. Note that 3-bits are sufficient for the trigger number since the TBM will not allow more than 8 unserved Level 1 triggers to be outstanding. The End of Frame will contain the current 3-bit trigger counter. Comparison of this trigger number with the trigger number in the Start of Frame will inform the FED of how many event triggers are contained in the readout pass. Note that when a Readout Chip receives a token bit it will write out the data for the trigger associated with the token along with any data from a later trigger that may exist.

We have had discussions with Honeywell on production of the TBM chip. Since it will be located at the end of the blades at about 15 cm from the beam line it must be implemented in a radiation hardened process such as the Honeywell SOI process. The digital portion of the chip can be implemented on an existing Honeywell gate array, HX2040. This array has 27,000 usable gates which are far more than the approximately 1000 gates needed for the TBM. Since the TBM will need to write analog data, namely, the Start and End of Frame records, it will need a radiation-hard high-speed DAC.

We are investigating several options for implementing this analog function. One would be to produce a separate analog chip containing a DAC developed by another group. The Readout Chip itself will need a high-speed DAC for sending the trigger counter number. Since both the Readout Chips and the TBM will talk to the same data line, these DAC's and associated drivers should be identical. A second option, if the design for this DAC were to exist in a Honeywell process, would be to incorporate it as an embedded or "dropped-in" cell as part of the digital TBM chip. This can be done at a reasonable cost by Honeywell.

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# Bump Bonding for ATLAS

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on behalf of the ATLAS Collaboration

May 1998

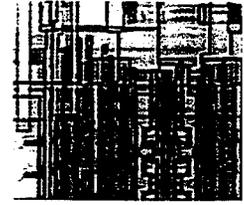
M. Gilchriese LBNL May 9, 1998

## Outline

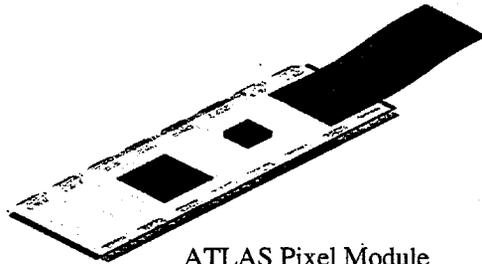
- ATLAS bump bonding requirements
- Prototype program plan
- Prototype results
- Vendor summary
- Outstanding issues
- Conclusions

# ATLAS Bump Bonding Requirements

- Number of bumps/placements
  - 2228 modules
  - 16 front-end chips per module
  - 35648 front-end chips => placements(+ yield losses)
  - 24x160 pixels per chip
  - $1.4 \times 10^8$  channels => bumps (+ yield losses)
- Bump spacing and size
  - Spacing currently  $50\mu$  in both x and y(center-to-center)
  - Sized for good yield and no shorts(roughly  $20\mu$  diam.)
- Wafers
  - 4"(for silicon detectors, which have "backside" processing), 250-300 microns thick (desire some small percentage to be 200 microns thick for innermost layer).
  - 6" for front-end integrated circuits(standard thickness, will thin later)

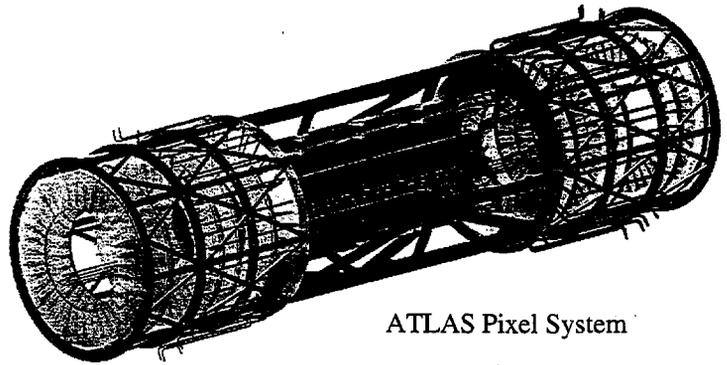


Bump bond pads on ATLAS prototype front-end B IC



ATLAS Pixel Module

3



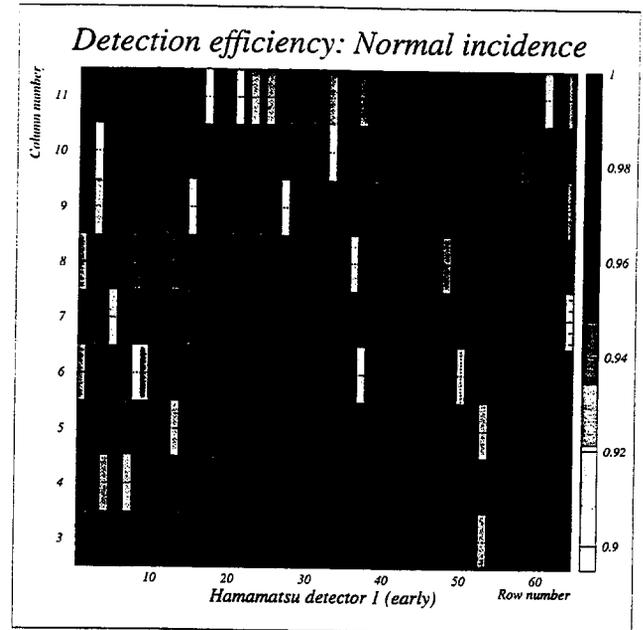
ATLAS Pixel System

## ATLAS Prototype Program

- Bump bonding of active silicon detectors and front-end ICs
  - Supports detector and electronics testing
  - Also see if bump deposition process affects detector properties(including after irradiation)
- Bump bonding of dummy parts
  - Bump deposition on dummy wafers(4" only so far)
  - Replicate bump pattern expected on detectors and ICs but connected to allow simple continuity tests to be made after flip-chip assembly to assess yield
  - Much cheaper than active parts, can do many more
- Thinning and dicing of bumped wafers
  - Require IC wafers to be thinned to 150 microns
- Verification of mechanical properties of bumps(tensile and shear strengths)
  - Dummy parts first
- Understand impact of stresses induced by mounting to mechanical structure
  - Coefficient of thermal expansion mismatch (although small) => thermally induced stress and creep
- Indirectly support bonding to alternatives to silicon eg. diamond(not discussed here).

# Bump Bonding of Active Components

- Have successfully bump bonded silicon detectors to ICs with good yield at Boeing(indium, USA), IZM(solder, Germany), LETI/Tronics(solder, France).
- Some dozens of single-chip assemblies have been completed, and a few 16 chip modules have been done or are just about to be done.
- Number of devices is too small to characterize yield, but it's easily good enough to allow testing of ICs and detectors.
- Devices have been tested over the last year or so for ATLAS in test beams.



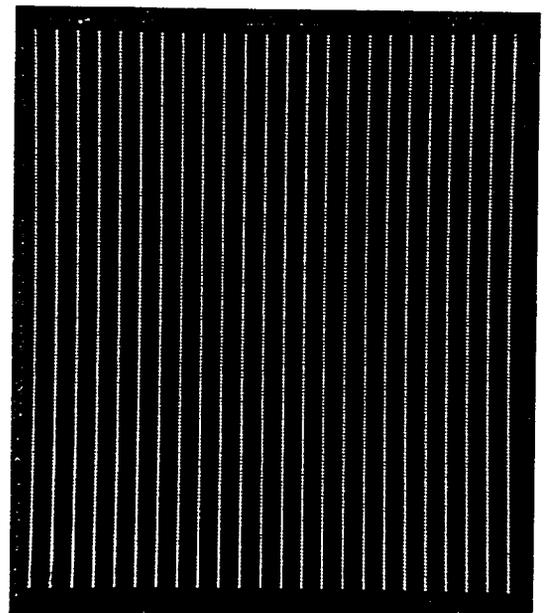
Efficiency of single-chip assembly

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# Bump Deposition on Dummy Components

- Four inch dummy wafers (of slightly different types) have been made by LBNL, CIS(Germany) and Seiko(Japan).
- Bumps have been deposited on these wafers (different vendors used different wafers) by
  - Alenia(indium, Italy)
  - Boeing(indium, USA)
  - Diamond Tech One(indium and solder, USA)
  - IZM(solder, Germany)
  - Seiko(solder, Japan)
  - Tronics(solder, France)
- Visual inspection of the bumped wafers has shown that the defect rate (largely missing bumps apparently from photoresist defects - my guess) is better than  $10^{-4}$  (typically a few  $\times 10^{-5}$ ) except for Diamond Tech One (which was unacceptable).



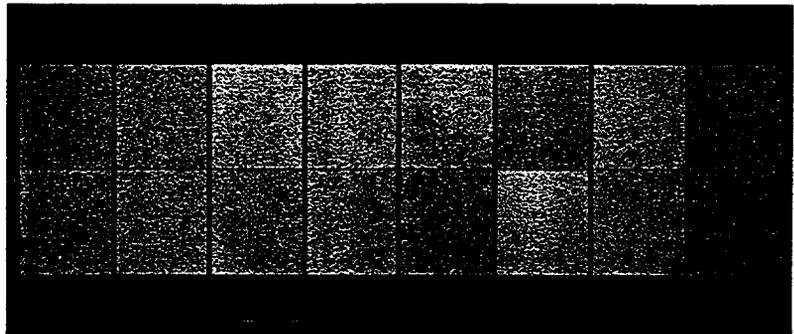
Dummy IC chip from Boeing

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# Flip-chip Assembly of Dummy Components

- The bumped dummy wafers have been used to make dummy, 16-chip modules.
- Boeing, Diamond Tech One, IZM, Seiko and Tronics have all assembled 16-chip modules. Alenia is in the process of doing so. A 16-chip module using parts from Boeing was assembled by UC Davis also.
- Continuity tests have been done on modules made by Boeing, IZM and Seiko.
- The number of modules measured is small, too small to allow one to separate the yield of flip-chip assembly from the bump deposition yield. However, the measured defect rate on these 16-chip modules (from loss of continuity) is less than  $10^{-4}$ , which is acceptable.

Dummy 16-chip module  
assembled by Boeing



M. Gilchriese LBNL May 9, 1998

## Mechanical Tests

- Only very preliminary mechanical tests have been done.
- Very rough measurements have been made of the strength in tension and shear. For about 3800 bumps, each 20-25 microns in diameter
  - Minimum strength in tension and shear for indium bumps is about 2.5 lbs
  - Solder is stronger, and the minimum strength in tension (shear) is about 14 lbs (10 lbs).
  - These are very rough numbers. Strength depends on strain rate, other factors and can easily be different by factors of two or more. More tests are needed, or more vendor data.
- We have also done preliminary tests of the effect of cooling dummy modules from room temperature to  $-20^{\circ}\text{C}$  while they are attached to simulated mechanical supports.
  - Temperature cycling tests (up to 15 cycles) have been done for both solder and indium dummy modules with different attachment schemes, including rigid attachment. No changes have been observed so far.
  - We have also started creep tests by keeping modules at the lower temperature (in a vertical position). No changes seen so far for indium after four weeks, tests are continuing
- Bottom line. Strength looks adequate so far. Thermally induced stresses appear to be tolerable.
- Just in case, one 16-chip module was assembled with underfill. We would like to avoid this because of possible interaction with the detectors (not known to be a problem, but why use it if not necessary). However, if strength problems do appear, this is a possible option.

# Vendor Summary and Status

- Bump Deposition and Flip-Chip Assembly - Prototypes Made
  - Alenia - work in progress. Flip-chip currently outside company but will have inside capability soon. Can do both 4" and 6" wafers.
  - Boeing - corporate decision to no longer do bump deposition for outside customers. Still open to flip-chip assembly.
  - IZM - work in progress. All work done inside. Can do both 4" and 6" wafers.
  - Seiko - decision to abandon 4" wafer bumping line(only 6" supported). Am told other Japanese companies same.
  - Tronics - work in progress. All work done inside. Only 4" wafers at present. Need to get 6" capability.
- Bump Deposition and Flip-Chip Assembly - Contacts Underway
  - AIT - both solder and indium. All work done inside. Can do both 4" and 6" wafers.
  - Rockwell Science Center - indium. All work done inside.
  - In house at LBNL - transfer of Boeing bumping process to LBNL(no flip chip capability)
- Bump Deposition and Flip-Chip Assembly - Failed
  - Diamond Tech One
  - MCNC
- Bump Deposition and Flip-Chip Assembly - Not Capable/Not Interested but Contacted
  - Amkor
  - Aptos
  - Flipchip Technology
  - IBM(USA)
- Flip-chip Assembly - Not Capable/Not Interested but Contacted
  - Flextronics
  - Multichip Assembly
- Preliminary pricing information obtained from some vendors.

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## Outstanding Issues and Future Work

- Outstanding issues
  - Impact of bumping process on irradiated detectors. Bump detectors irradiated at LBNL, preliminary measurements made at New Mexico. Looks OK but need more statistics. In progress.
  - Possibility for rework. Is this possible at all? Everyone knows that the chip yield must be very, very high to have 16-chip modules with high yield, and burn-in is not possible. Alenia says they will study rework. No results. Very tough.
  - Improved inspection
    - Inspection after bump deposition so far done by eye. This works pretty well, but a number of different automated systems (3D profilers) exist and are in use in the bumping industry. We have contacted a few vendors and have had one do a dummy bump map. It's beautiful but expensive. Looking for cheaper alternative. Not clear it's needed but would be nice to have if cheap.
    - Inspection after assembly. Just started investigation of X-ray and ultrasonic scanning.
  - What is real yield?
- Future work
  - More active components are in the pipeline, including first 6" IC wafers
  - Need to assess results later this year and decide how to proceed on both real wafer and dummy wafer work.

# Conclusions

- Proof-of-principle that bump bonding meeting ATLAS specifications with good yield has been obtained with multiple vendors.
- Sixteen-chip modules have been assembled by multiple vendors.
- Mechanical properties of assembled modules appear so far to be adequate to allow handling, etc and thermally-induced stresses that will result from mounting on mechanical/cooling structures appear tolerable.
- Both indium and eutectic solder appear to be viable candidates for ATLAS.
- We have a lot of work to do to go from our current prototype stage to production with good yield!

# Flip Chip Bump Bonding at UC Davis

Gary Grim, Chris Hill, Richard Lander

Why is an academic Inst. doing this industrial work?

It goes back to D. Pellett's involvement in D. Nygren's SSC pixel group.

Key pieces of the pixel problem:

Readout electronics - LBL doing that.

Hybridization - No one doing much.

Sensors - We didn't worry about it at the time.

So we started with hybridization.

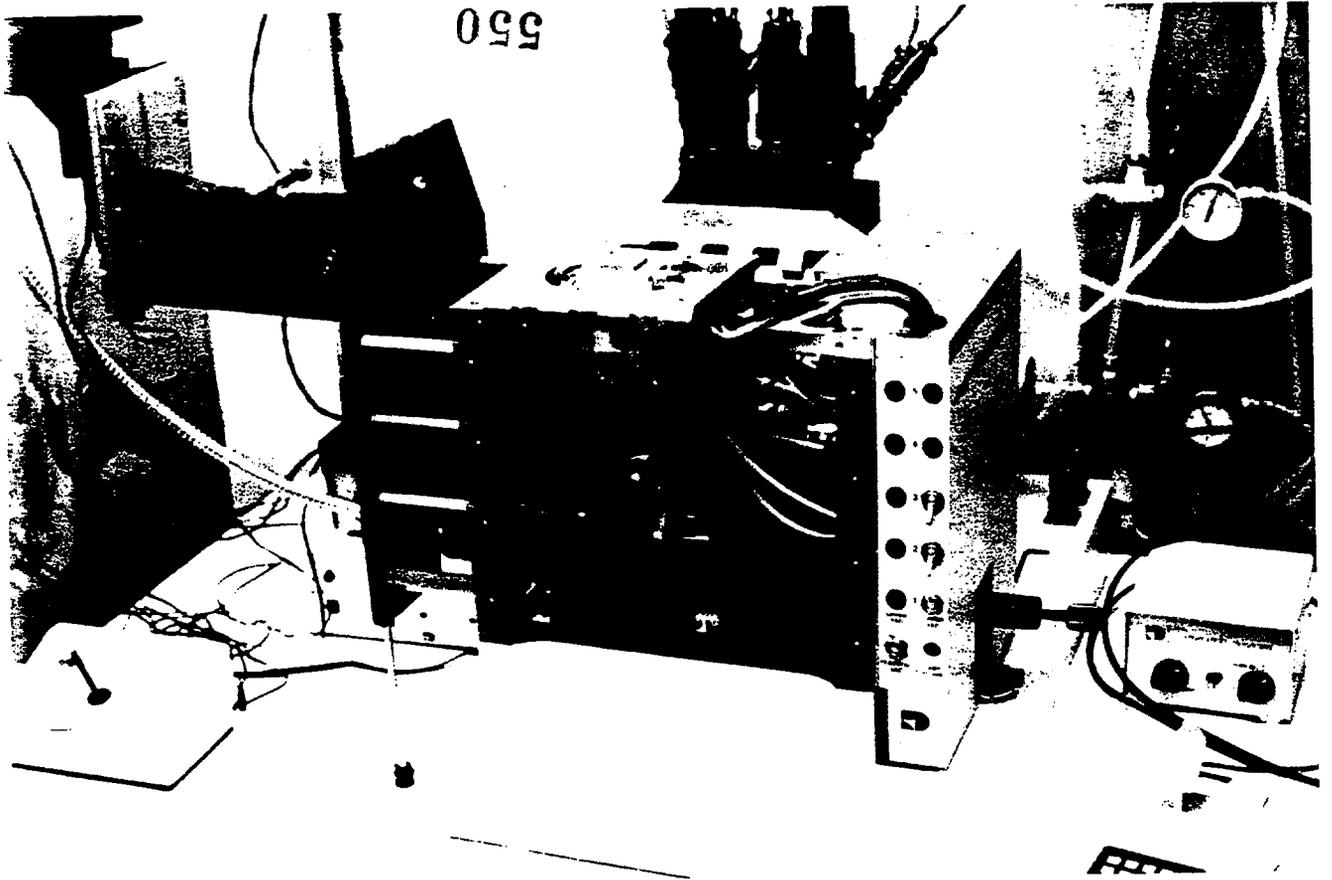
DOE grant from University Research Instrumentation Program

Bonder, Clean Room, Test Equipment

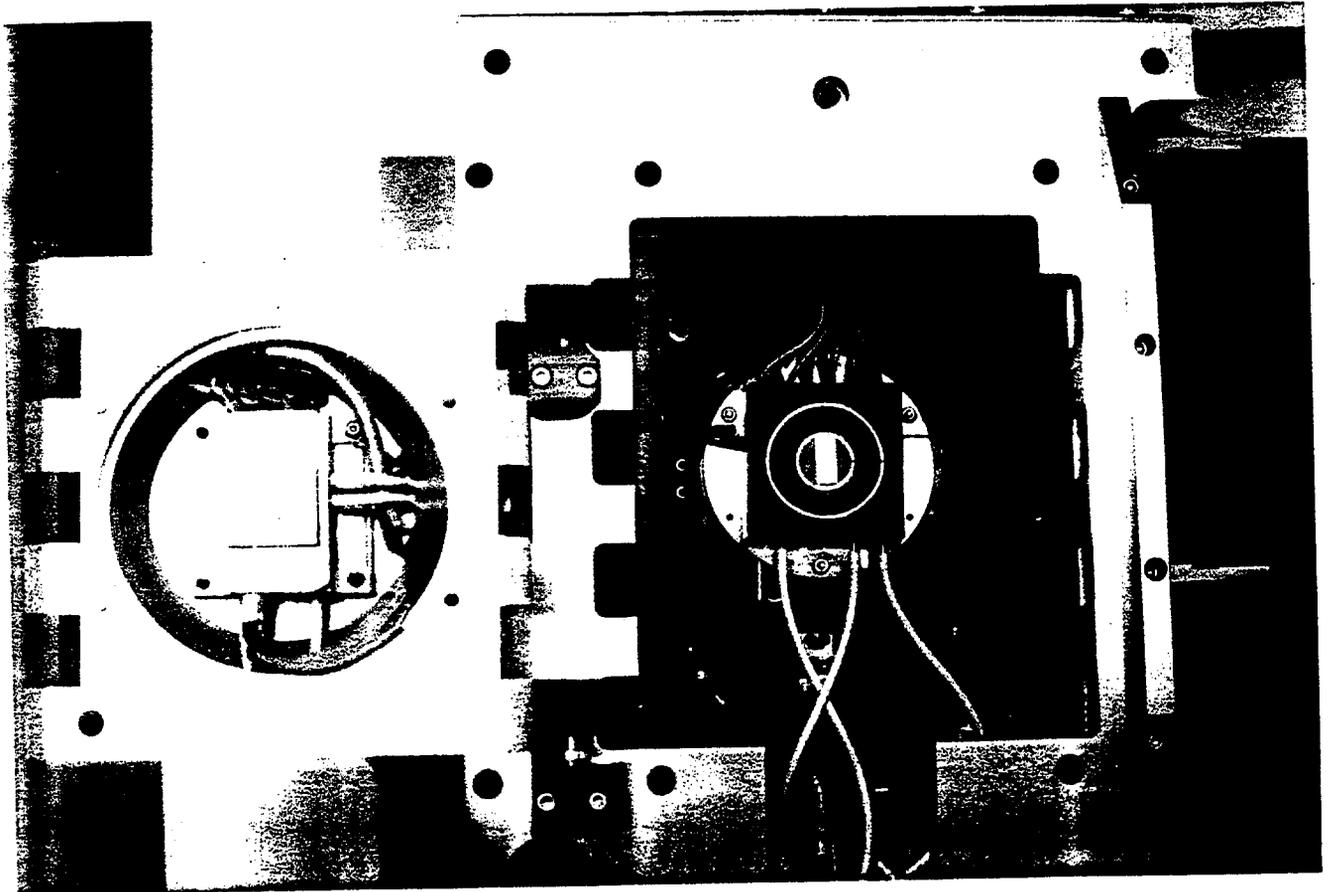


BONDING LAB - UC DAVIS

550



TOP CHUCK FLIPPED OPEN



Then....

SSC died \$\$\$  
\$ \$ \$  
↓  
Slow Progress

But...

CMS → Pixels  
→ USCMS takes on forward pixels  
→ UCD responsible for - forward pixel readout  
(with PSI)  
- hybridization

UCLA meeting - Nygren 3/95  
PSI meeting - Pellett 6/95

51  
51  
1

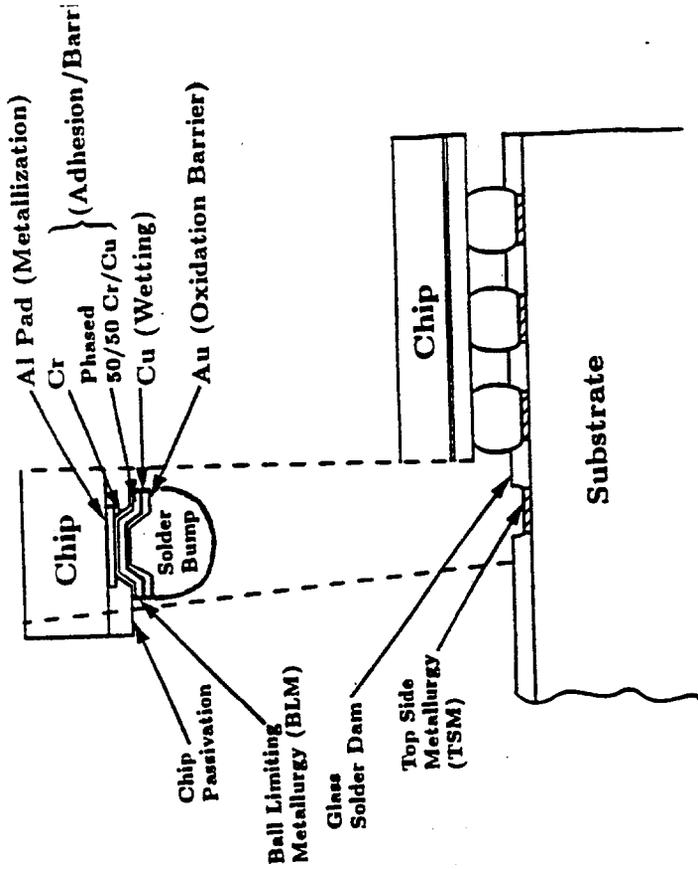
But....readout will need a sensor to fully test

6/96 ---> BNL for sensor fabrication

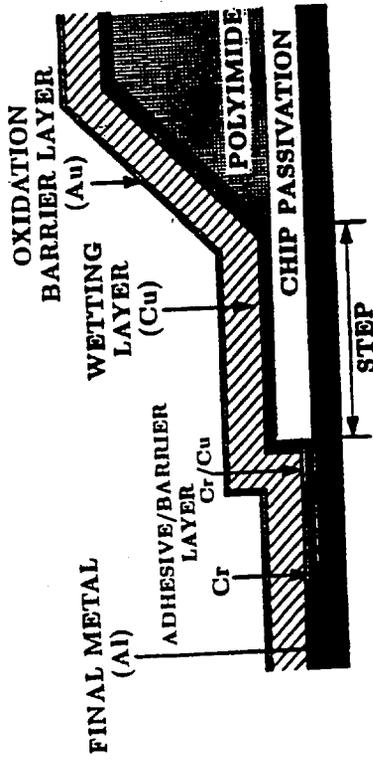
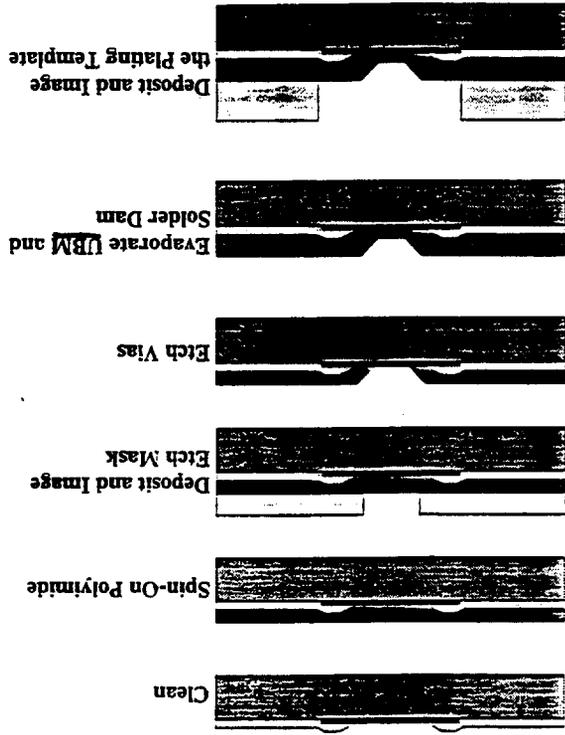
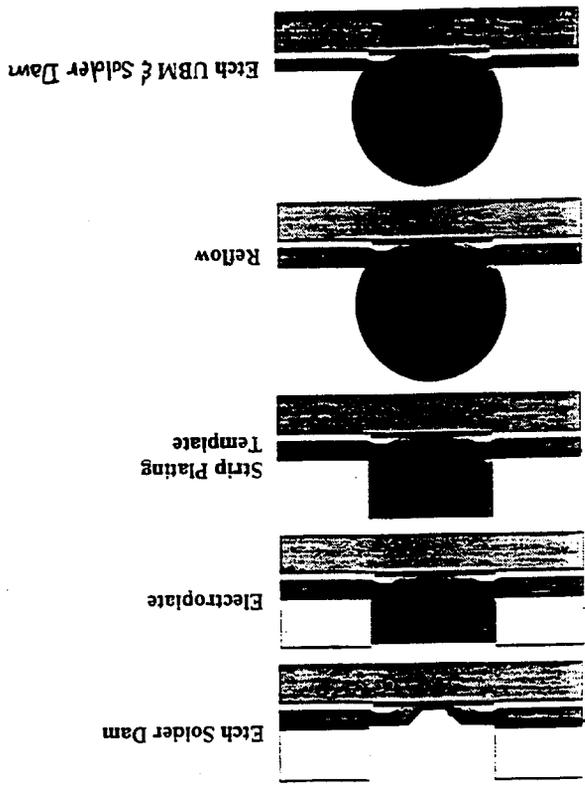
- So we wound up involved in all three pieces

You heard about Column Architecture.....G. Grim  
and Sensors.....G. Bolla

- Now a few words about flip chip bump bonding

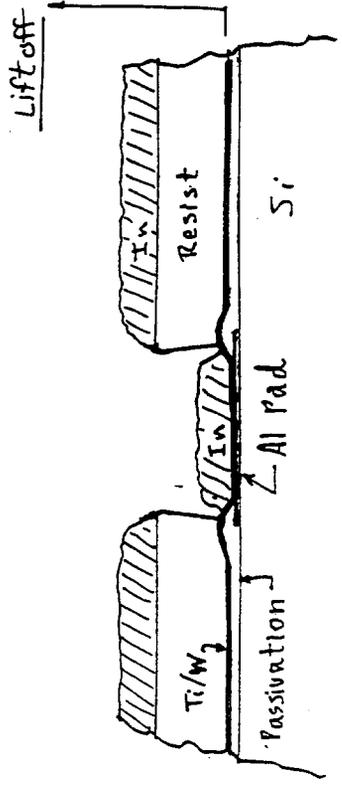


IBM C4 PROCESS  
Pb/Sn Solder

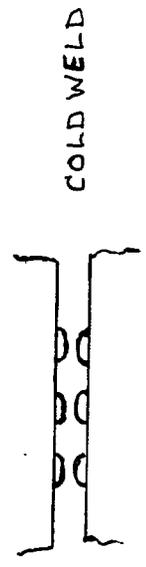


(b) IBM's C4 (controlled collapse chip connection) technology; (b) IBM's ball-limiting metallurgy structure.

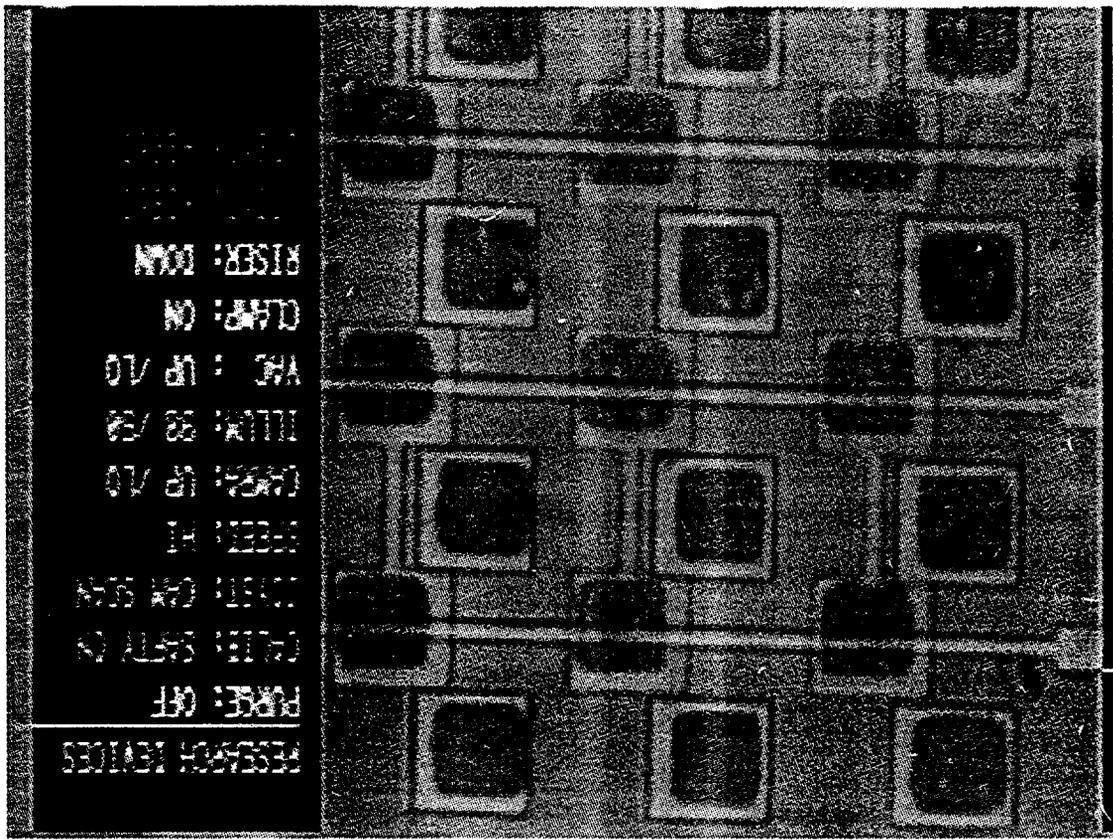
Bumps on both chips



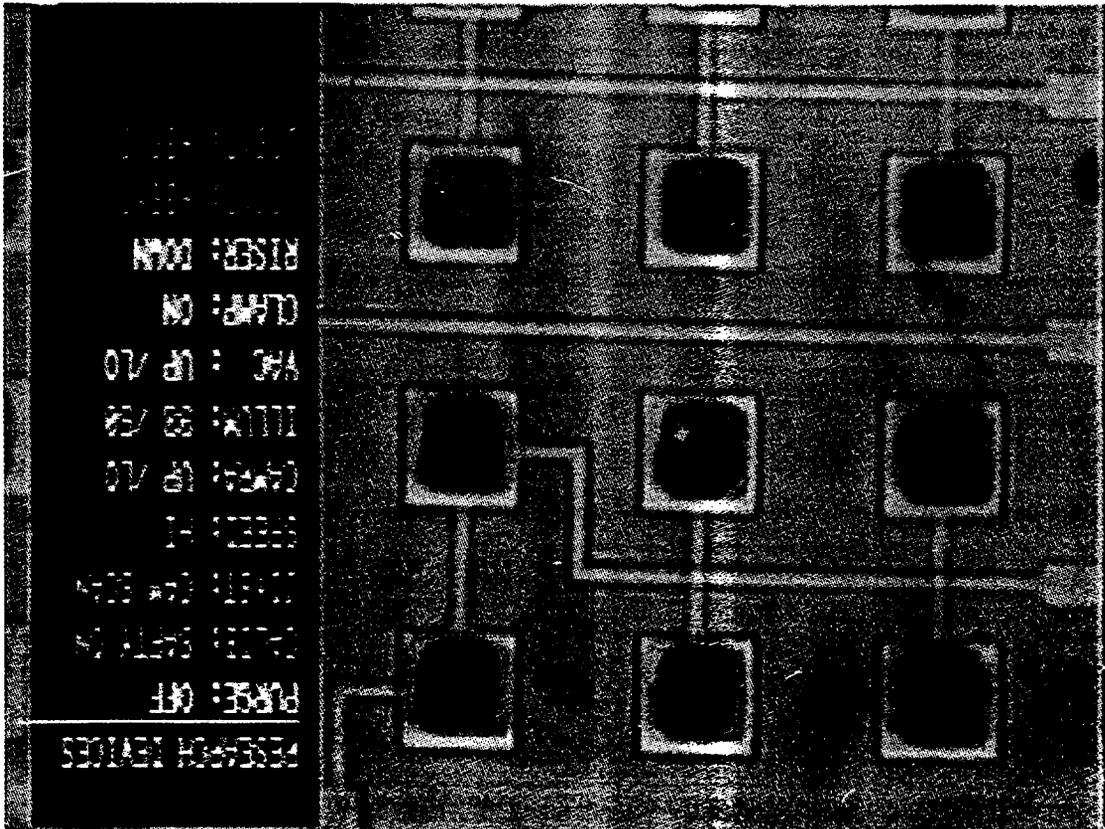
- Clean
- Deposit UBM (Ti/W)
- Deposit resist and pattern it (etch)
- Deposit indium
- Lift off resist and excess indium
- Selectively etch excess Ti/W



BUMPS BEFORE ALIGNMENT



RESEARCH MATERIALS  
 PART: 017  
 DATE: 08/10  
 TIME: 09:59  
 USER: H  
 GROUP: 10/10  
 ITEM: 00/00  
 VHS: 10/10  
 CLASS: 00  
 RISER: 0000



TECHNICAL CONSIDERATIONS

- CAPACITANCE ..... LOW  
SMALL BUMPS
- THERMAL CONDUCTANCE .... HIGH ✓
- RESISTANCE ..... LOW ✓
- TEMPERATURE STRESS ..... -100 C
- MECH. STRENGTH ..... REASONABLE
- YIELD PER BUMP ..... VERY HIGH

CONNECTIVITY TEST

13

AN INDIUM ALLOY

40X40  $\mu\text{m}^2$  BUMPS

100  $\mu\text{m}$  pitch [AIT]

> 100 FLIP CHIP ATTACHMENTS,

PRESSURE 2  $\text{mg}/\mu\text{m}^2$   
TEMP. 25 - 40  $^{\circ}\text{C}$   
TIME 60 SEC.

>10,000 INTERCONNECTS MEASURED

RESISTANCE < 1 OHM

CONNECT YIELD (99.78% +- 0.06)%

==> 99.7%, 95% CL

[RD19, Lisbon]

51  
51  
51

IN/SN/AG ALLOY (w/ LBL)

10 FLIP CHIP ATTACHMENTS  
> 5400 INTERCONNECTS MEASURED  
20x20  $\mu\text{m}^2$

PRESSURE 15 -20  $\text{mg}/\mu\text{m}^2$   
TEMP. 25 - 40  $^{\circ}\text{C}$   
TIME 60 SEC.

CONNECT YIELD >99.9% (0/5400)

-20  $^{\circ}\text{C}$  & 100 G's AT 2 KHZ,

RESISTIVE TECHNOLOGY INC.

- AU STUDS ON MULTILAYER ALUMINA SUBSTRATE
- AU PLATED BUMPS ON CHIPS  
HEAT, HIGH PRESSURE
- AU STUDS ON MULTILAYER ALUMINA SUBSTRATE
- IN/PB BUMPS ON CHIPS  
ROOM TEMP, HIGH PRESSURE

PLANAR TECHNOLOGY OF AMERICA

- ANISOTROPIC CONDUCTIVE FILM  
ROOM TEMP, HIGH PRESSURE

51  
52  
53

HEWLETT/PACKARD

- QUARTZ - POLY - METALLIZED Si  
ROOM TEMP, LOW PRESSURE
- TRANSFER Si STRUCTURES  
ROOM TEMP, MOD. PRESS

BUMP GROWING FACILITY

- - EVAPORATOR SYSTEM SETUP

PRIMEX X-RAY IMAGER

ORBIT TI/W UBM 4-INCH WAFERS

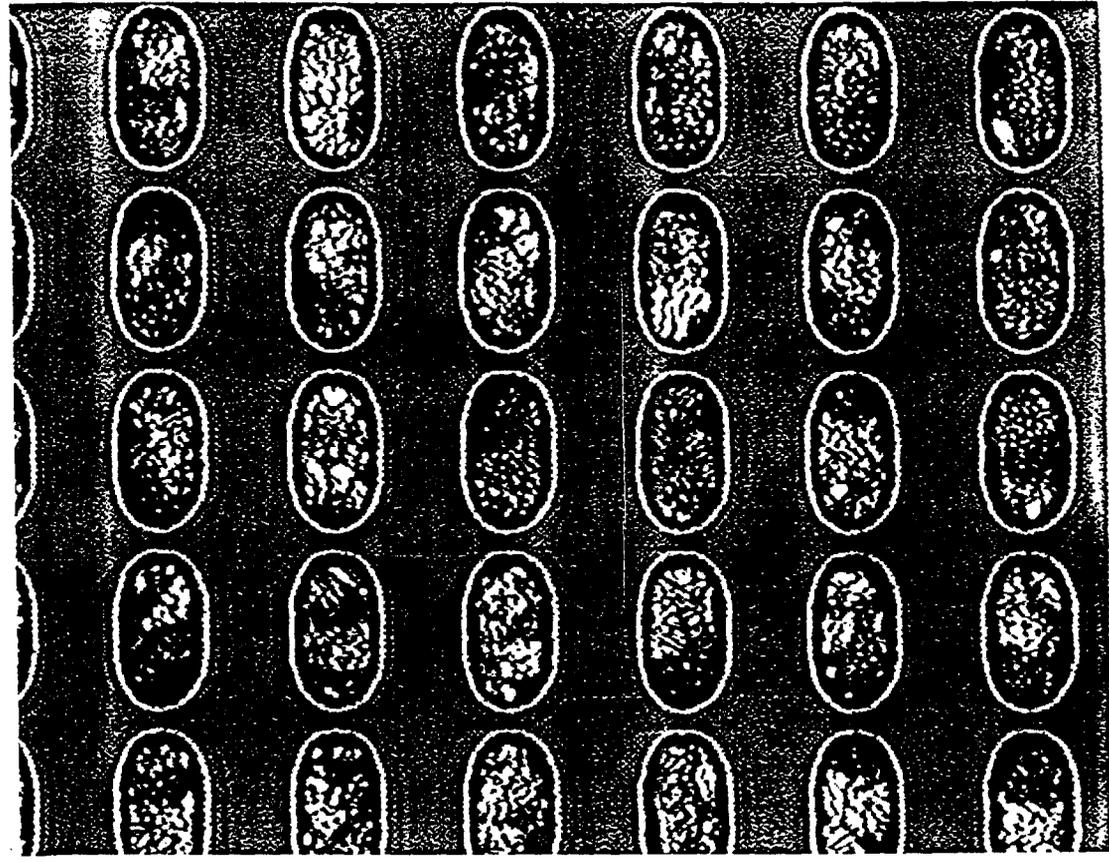
- DEPOSITED BUMPS  
18X30  $\mu\text{m}^2$   
60,000/CHIP  
1X3  $\text{CM}^2$  CHIP PAIRS
- BONDED 1X3  $\text{CM}^2$  CHIPS
- GOOD IMAGES

DUMMY CHIPS

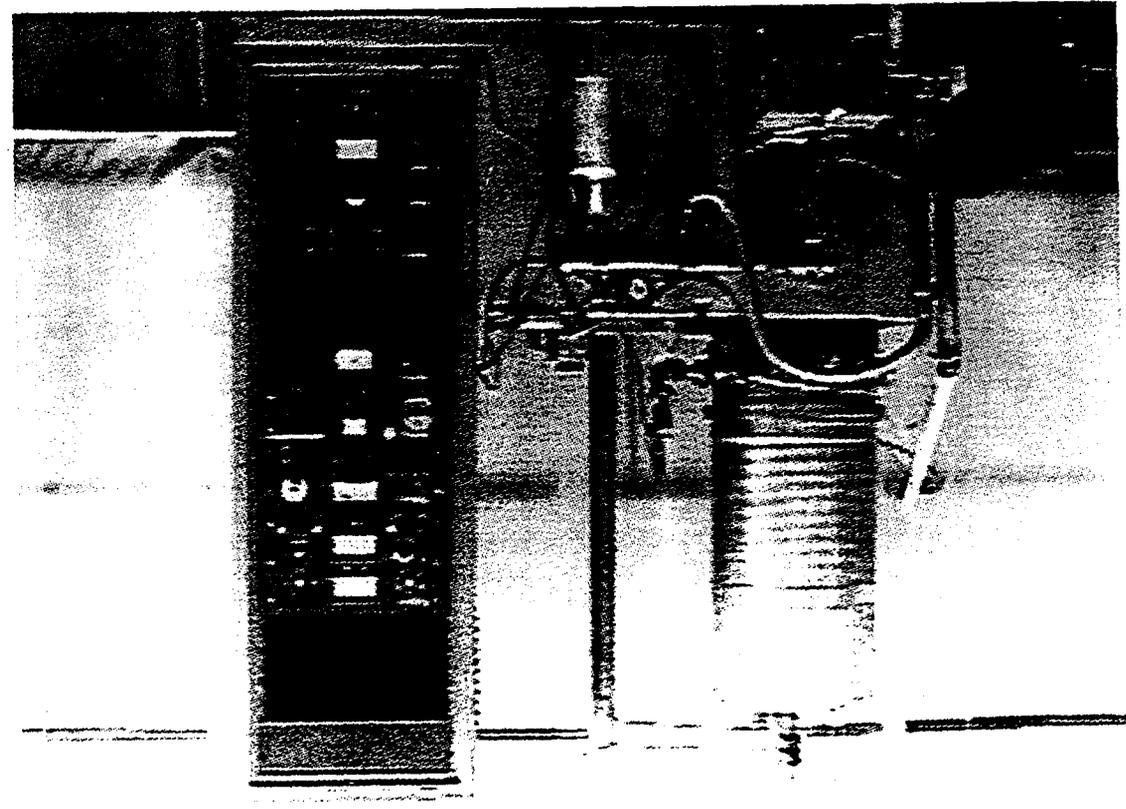
- 80X80 ARRAY
- 25X25  $\mu\text{m}^2$ , 50  $\mu\text{m}$  PITCH
- - TENSILE STRENGTH
- - SHEAR STRENGTH
- - LIQUID NITROGEN

X-RAY IMAGED CHIP

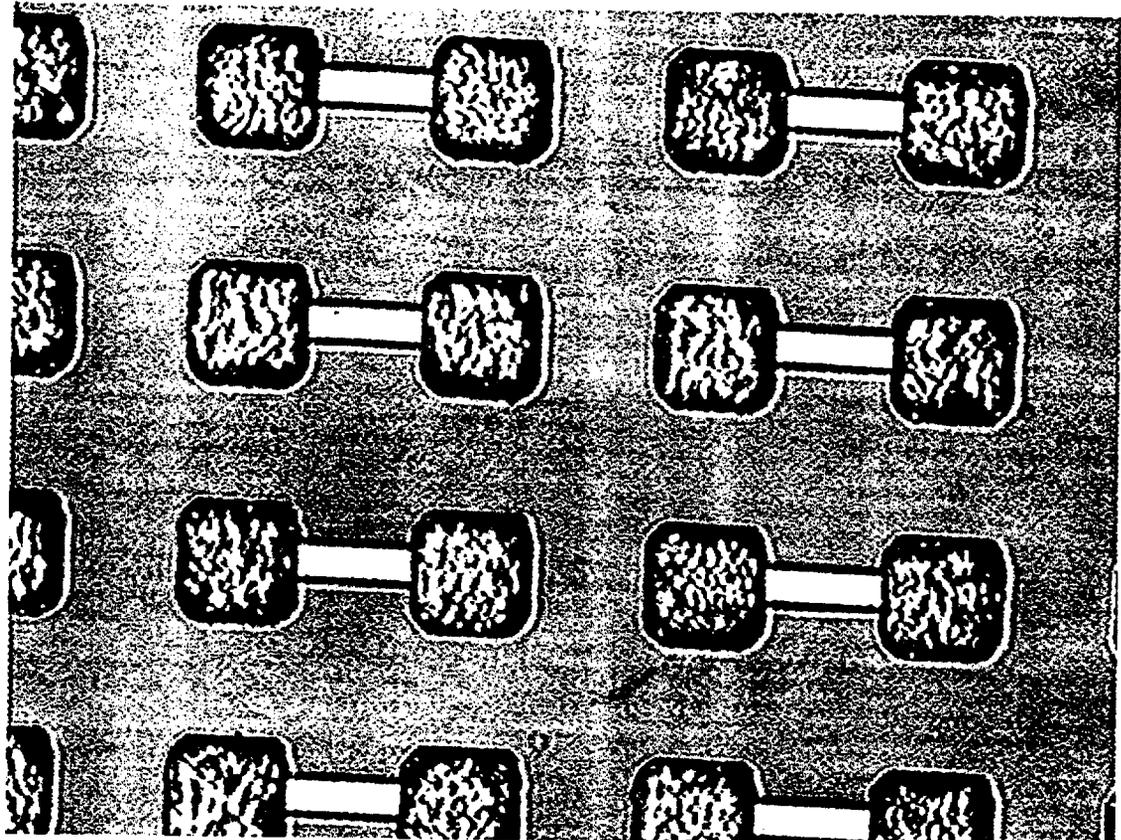
~ 18 x 30  $\mu\text{m}^2$  Indium-UCD



INDIUM EVAPORATOR

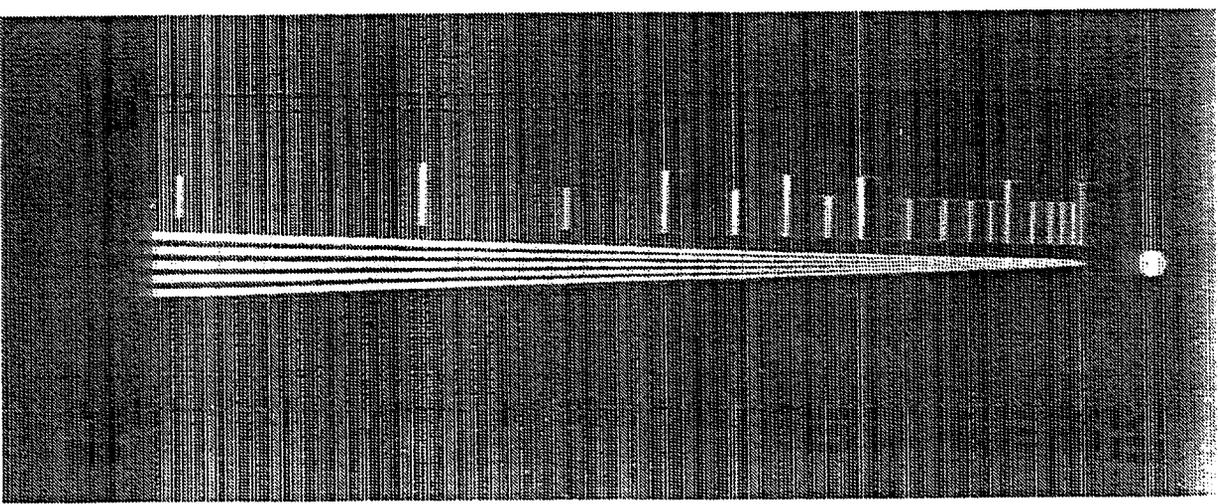


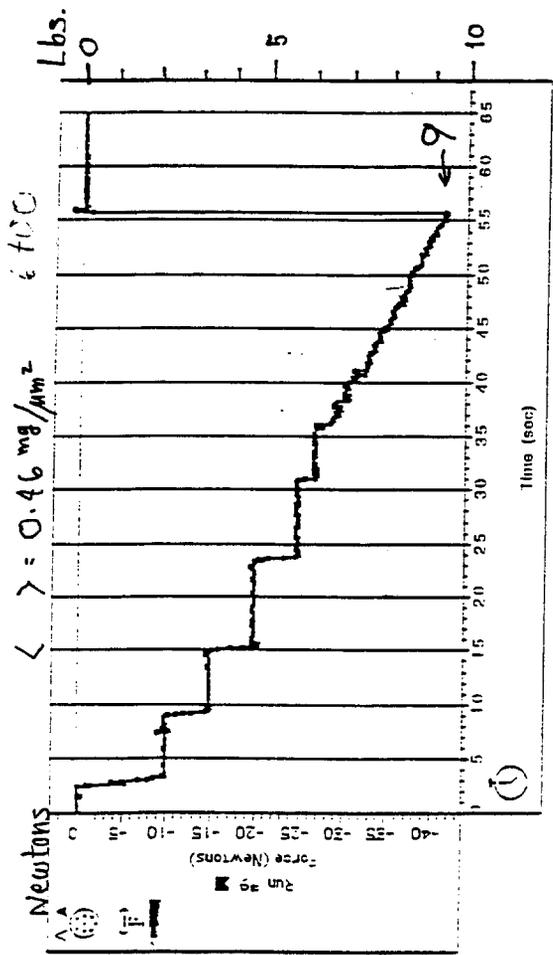
INDIUM - UCD  
25 μm SQUARE, 50 μm PITCH



19

X-RAY  
IMAGE





PSI readout 52x53 = 2756 bumps

0.46 mg/μm<sup>2</sup> yield stress

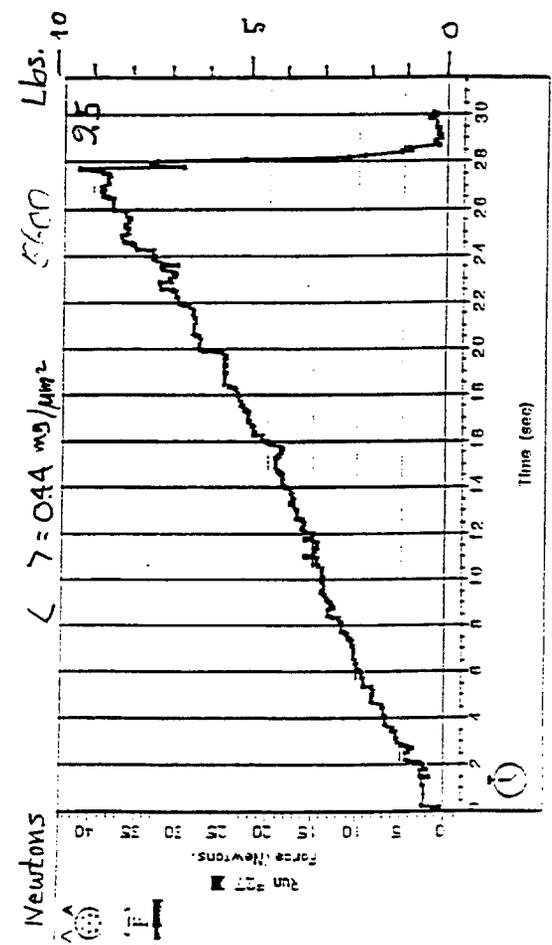
22 μm diameter bump --> 1.1 lbs

25 μm " --> 1.4 "

30 μm " " --> 2.0 "

● Conclude:

Even small In bumps are strong enough to tolerate handling during assembly.



TIME STUDY

4 CHIPS PER SUBSTRATE  
 150 μm GAP BETWEEN CHIP EDGES

4 HOUR RUN BY TECH  
 - 4 MIN. PER PLACEMENT

SETUP, BREAKS, ETC.

➔ 8 MIN. PER PLACEMENT TOTAL

€C/day = 6000/20 weeks ≈ FWD PIXEL

● 150 μm GAP NOT A FACTOR

FUTURE

NOW SETTING UP UBM

- Ti/W

- ZINCATE

51  
56  
0

NEED HIGH PLACEMENT YIELD PER DIE

PLAQUETTE  $Y_n = (\epsilon)n$

$n \backslash \epsilon$	.99	.98	.95	.90
10	.90	.82	.60	.35
8	.92	.85	.66	.43
6	.94	.88	.74	.53

WANT HI  $\epsilon$  AND KNOWN SMALL  $\sigma$  ( $\epsilon$ )

SOME BINOMIAL STATISTICS

$\epsilon \backslash n$	.99	.98	.95
100	.010	.014	.022
200	.0070	.010	.015
300	.0057	.0081	.011
500	.0045	.006	.010

TO KEEP ERROR BELOW 0.01, NEED AT LEAST A  
 FEW 100 PLACEMENTS TO QUALIFY VENDORS

## SUMMARY

- We have substantial experience with flip chip bump bonding, the hybridization method of choice for CMS.
- We have in-house facilities for indium bump deposition and flip chip bonding, and will have facilities for cleaning & UBM (Ti/ W) deposition.
- We can bond US CMS prototypes with indium.
- If necessary, we could carry out the entire production bonding for US CMS.



# Flip-Chip and Bump Interconnect Technologies for Sensor Applications

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## Flip-Chip & Bump Interconnect Technologies for Sensor Applications

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### Outline:

- Bump interconnect and flip-chip bonding requirements for sensor/detector applications
- Bump interconnection technologies:
  - Indium bumps: X-ray detectors, IR sensors, and RF applications
  - Lead-tin bumps: Flip-chip-on-board (FCOB) applications
- Comparison between indium and eutectic solder bumps:
  - Fabrication process
  - Minimum achievable bump dimensions and pitch
  - Electrical and mechanical characteristics
  - Bumping and flip-chip bonding yields
  - Manufacturability and cost
- Summary and Conclusions

# Indium Bumps

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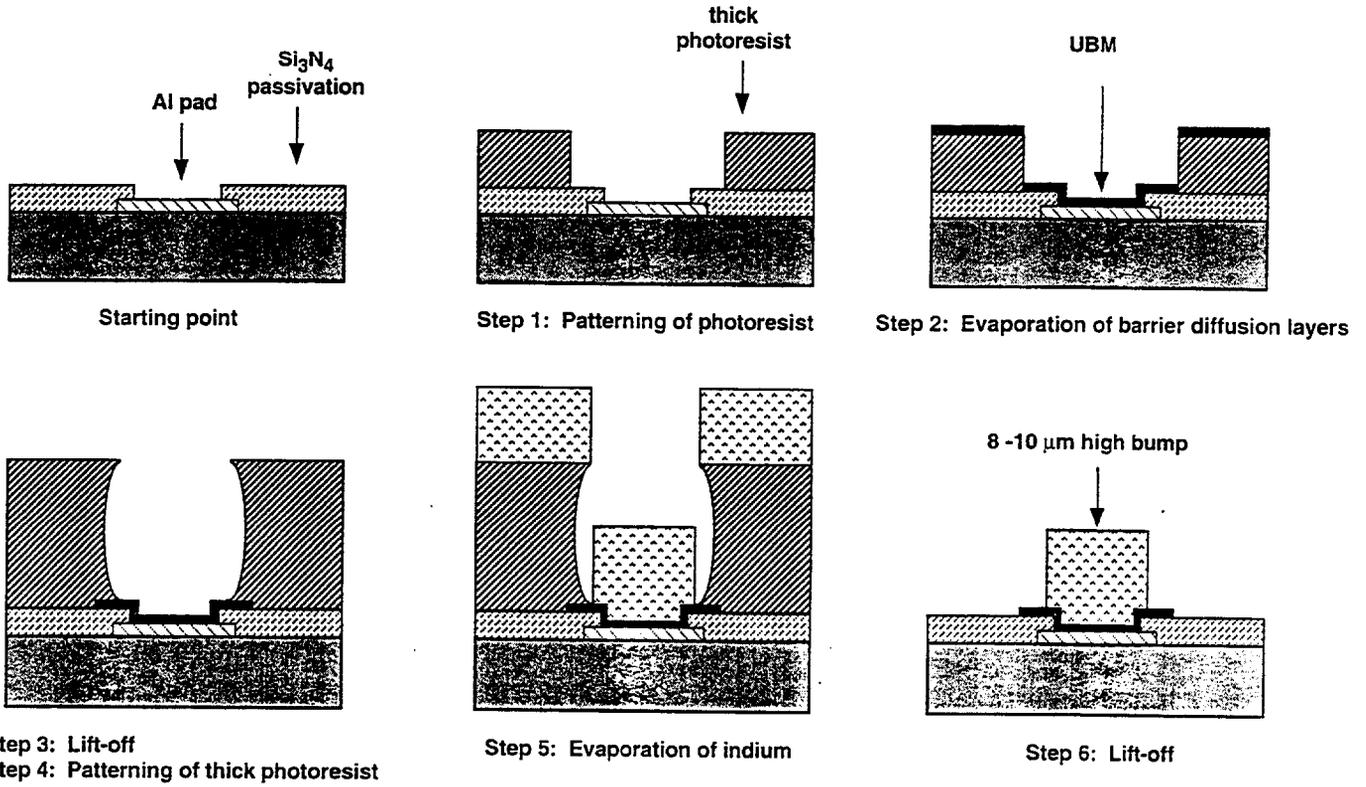
- Used primarily in the hybridization of semiconductor materials for sensors/detectors:
  - IR sensors (HgCdTe, InSb, GaAs to Si) and X-ray detectors (CdZnTe, Si to Si)
- Fabricated by thermal evaporation (using a lift-off process)
  - smaller bumps, finer pitch, better uniformity and control, single die bumping
- Sputter deposited 2-metal layer barrier diffusion UBM
- Soft compliant bump with a melting point of 156°C
- Forms a non-conducting oxide layer
- Enhancement of surface area of bump a factor in mechanical strength
- Both sides have to be bumped
- Typical bump sizes of 25-50  $\mu\text{m}$  with a height of 8-10  $\mu\text{m}$
- Large arrays with 100K+ bumps possible - 12  $\mu\text{m}$  diameter bumps on a 25  $\mu\text{m}$  pitch
- Flip-chip bonding using compression only (room temperature process) requiring ~2-3 grams/bump (for 50 x 50  $\mu\text{m}$  bump area with a height of 8-10  $\mu\text{m}$ )
- Bump resistance of ~1-2 Ohms for a 25  $\mu\text{m}$  square bump with a height of 10  $\mu\text{m}$
- Requires a flip-chip bonder with 1-2 micron alignment accuracy and planarization
- Expensive to fabricate

## Flip-Chip & Bump Interconnect Technologies for Sensor Applications

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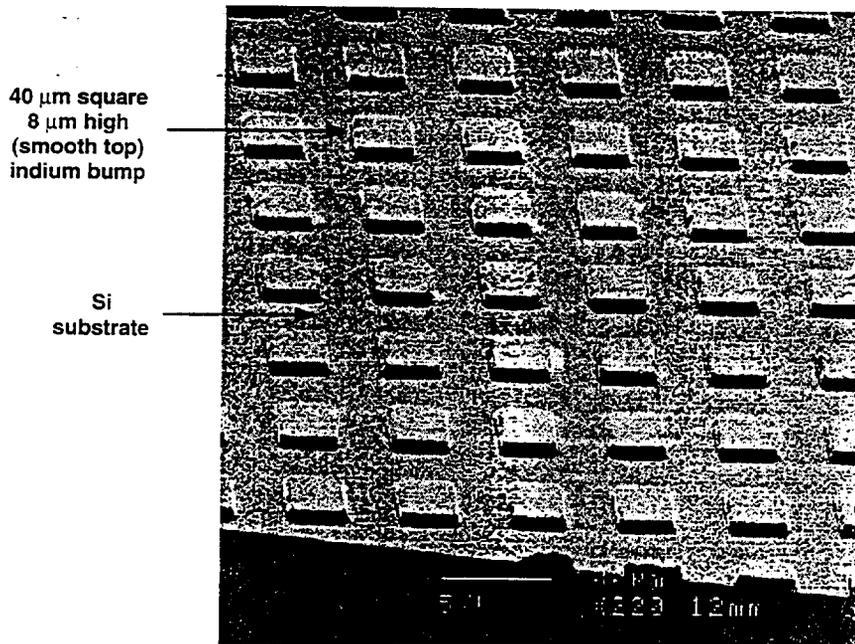
- Issues to be addressed in the choice of bump interconnect technology:
  - hybridization of sensor/detector to Si
  - required minimum bump dimensions and pitch
  - size of die and number and distribution of interconnections
  - availability of sensor material in wafer form
  - operating temperature (liquid nitrogen or room temperature)
  - electrical and mechanical characteristics
  - bumping and bonding yields
  - manufacturability
  - cost

# Fabrication of Indium Bumps by Evaporation



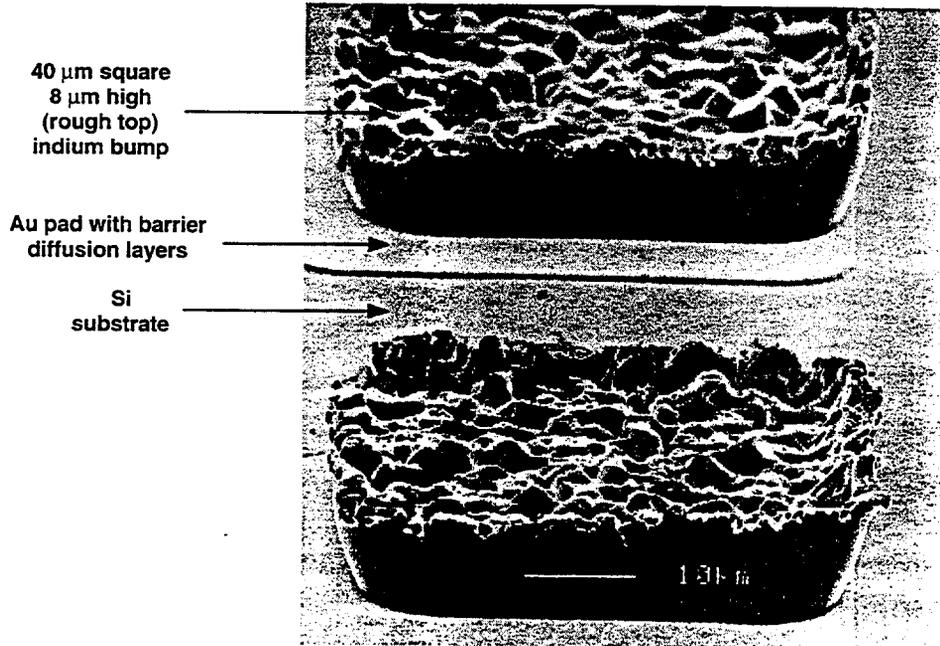
## Evaporated Array of Indium Bumps

(scanning electron micrograph)



# Evaporated Indium Bumps

(scanning electron micrograph)

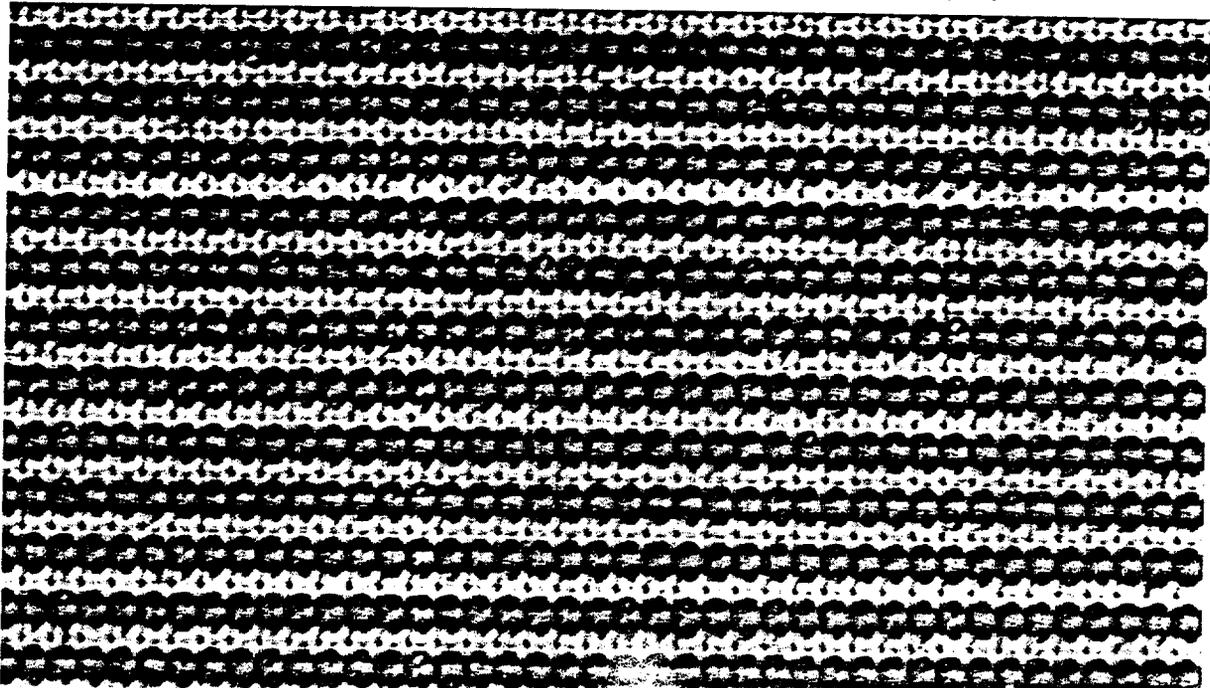


Advanced Interconnect Technology

# Array of Evaporated Indium Bumps

(optical micrograph)

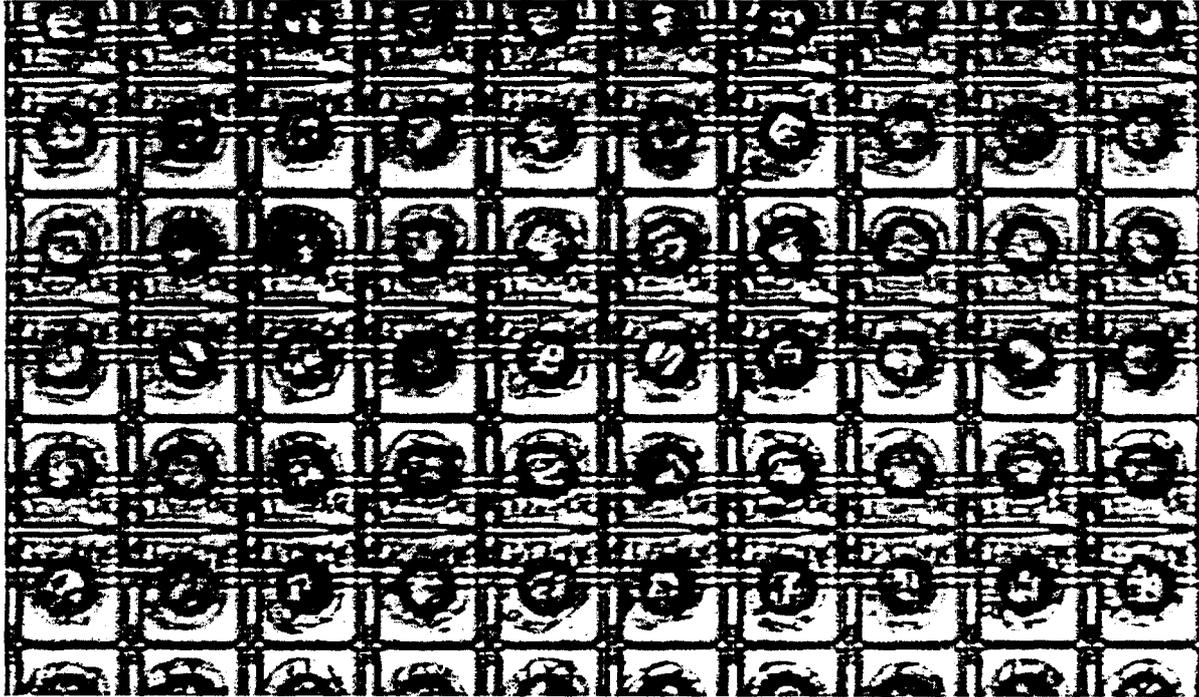
Partial array of 140,000 bumps: 12  $\mu\text{m}$  diameter, 8  $\mu\text{m}$  height, 25  $\mu\text{m}$  pitch



# Array of Evaporated Indium Bumps

(optical micrograph)

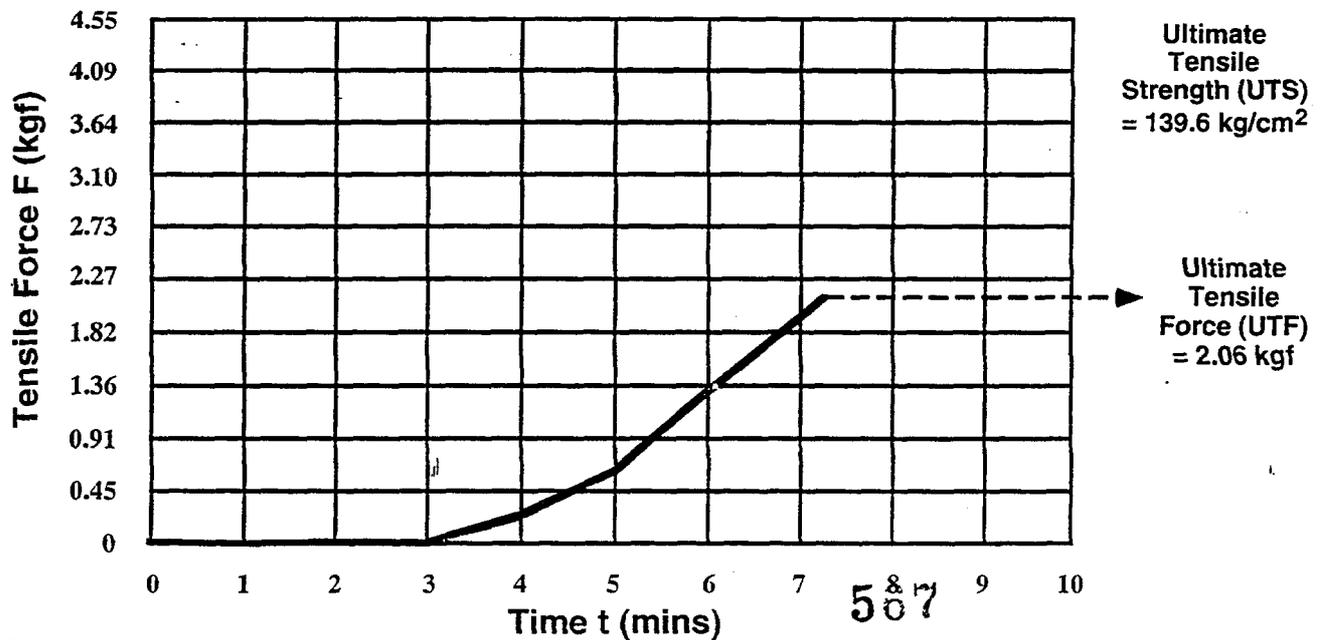
Partial array of 140,000 bumps: 12  $\mu\text{m}$  diameter, 8  $\mu\text{m}$  height, 25  $\mu\text{m}$  pitch



Advanced Interconnect Technology

## Mechanical Strength of Bonded Indium Bumps

304 indium bumps, 70 x 70  $\mu\text{m}$  area, 12  $\mu\text{m}$  height

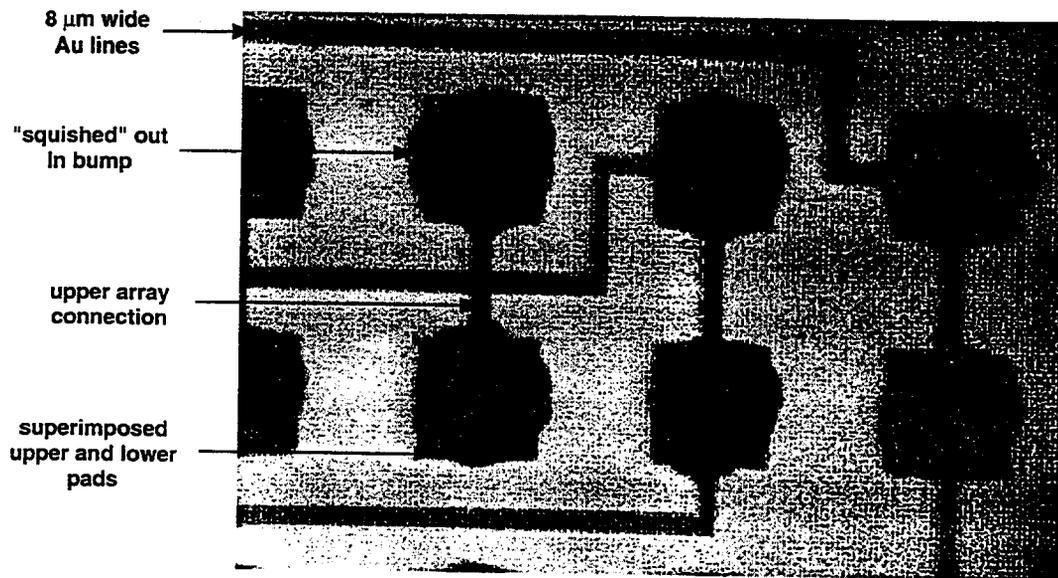


**Notes:**

Pull tester with a calibrated load cell of 9.09 kg with a pull speed of 0.21 inch/min  
All failures were within the bulk of the indium

# IR Illuminated Flip-Chip Bonded Array of Indium Bumps

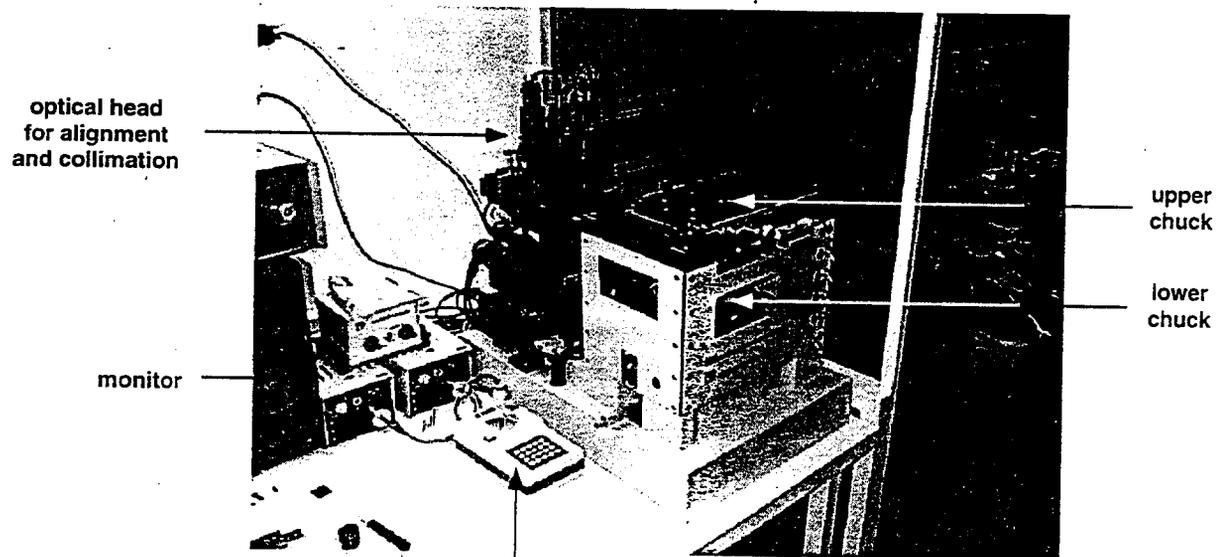
(back-side illuminated Si substrate)



Advanced Interconnect Technology

## Flip-Chip Aligner/Bonder

Research Devices Aligner/Bonder Model M8-A



controller  
iovstfck

568

# Indium Bumping and Bonding Yields

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- **Bumping yields of >95%**  
Example: 6" wafer with 22 detector chips (each with 140K pixels)  
21 detectors had no missing bumps (visual inspection)  
1 detector (at the edge of the wafer) had a line of shorted bumps
- **Manual flip-chip bonding yields of >85%**  
Example: 20 modules fabricated, each detector with 140K bumps  
Lost one module in defective wire bonding  
Out of the remaining 19 modules, 16 were perfect with no defective bonds  
Remainder of 3 modules had 10-20 missing pixels (primarily at the corners/edges)

# Electroplated Lead-Tin Solder Bumps

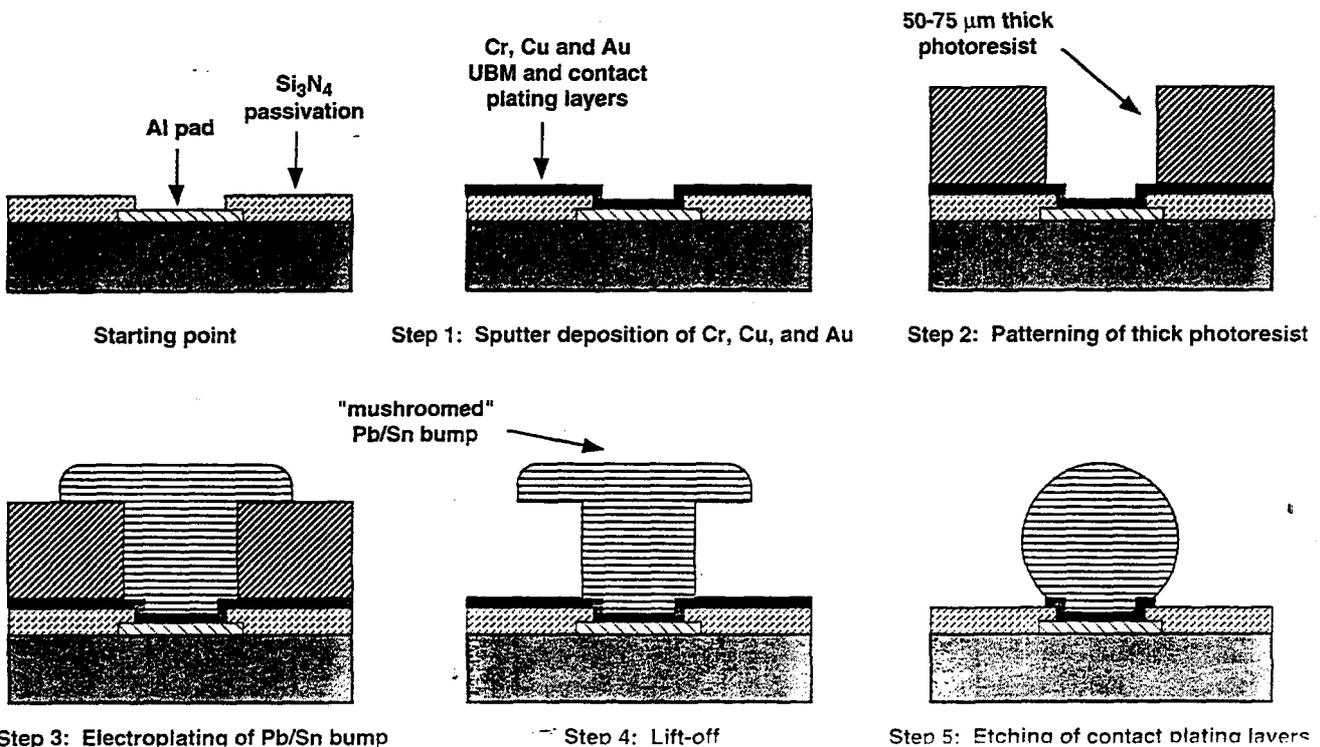
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- **Versatile in the choice of solder alloy composition (reflow temperatures)**
- **Self-aligning and self-planarizing bumps upon reflow**
- **Requires fabrication of solder bump on one side only with an opposing "wetable" pad**
- **Requires a complex under-bump-metallurgy (UBM) - Cu, Ni, Au**
- **May require the use of flux and removal of flux residue**
- **Excellent electrical and mechanical characteristics:**
  - **low resistance electrical path (2-3  $\mu$ Ohms)**
  - **low inductance (~0.1 nH)**
  - **bump shear values in excess of 30 grams for a 50 micron diameter bump**
- **Does not require a highly accurate flip-chip aligner/bonder ( $\pm 10$  microns X-Y)**
- **Currently limited to minimum 35-50  $\mu$ m diameter bumps on a 70-100  $\mu$ m pitch**
- **Alpha particle emission from bumps and susceptibility to high radiation dose**
- **Potentially low-cost in high volume**

# Solder Types and Liquidus Temperatures

Solder Composition	Liquidus Temperature (°C)
Sn(62.5%)-Pb(36%)-Ag(1.5%)	178
Sn(63%)-Pb(37%)	183
Sn(92%)-Ag(5%)-Cu(2%)	210
Sn(95%)-Pb(5%)	223
Sn(100%)	232
Pb(75%)-In(25%)	250
Pb(90%)-Sn(10%)	268
Pb(97%)-Ag(3%)	304
Pb(95%)-Sn(5%)	308
Pb(100%)	327
Sn(3%)-Au(97%)	370

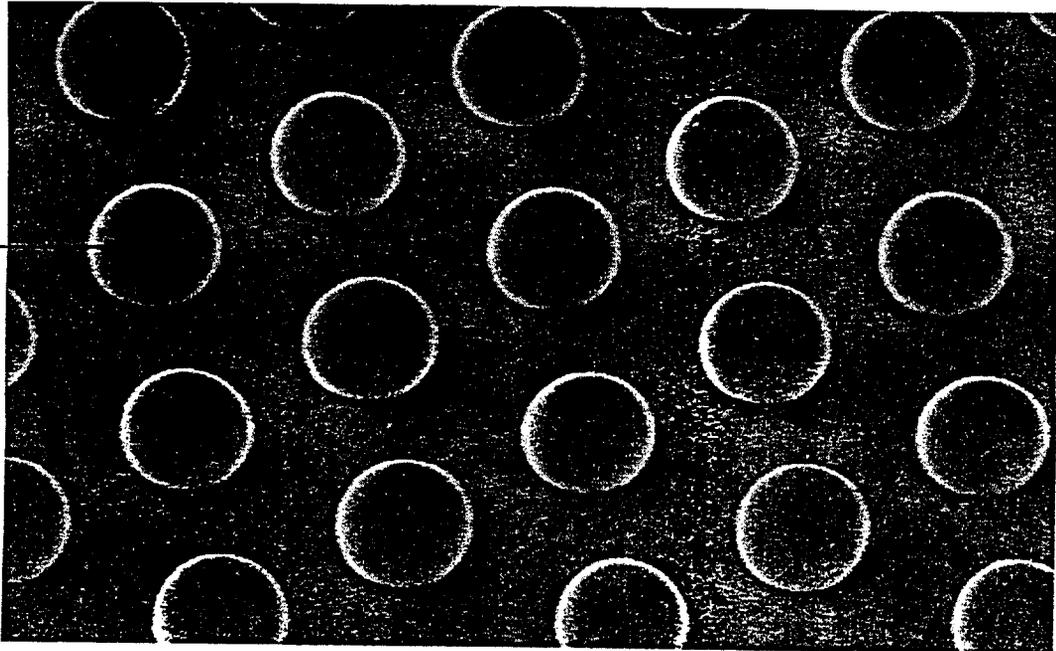
## Fabrication of Lead-Tin Bumps by Electroplating



# Array of Electroplated and Reflowed Eutectic Solder Bumps

(scanning electron micrograph)

50  $\mu\text{m}$  diameter  
50  $\mu\text{m}$  high  
100  $\mu\text{m}$  pitch  
eutectic Pb-Sn  
bump



Advanced Interconnect Technology

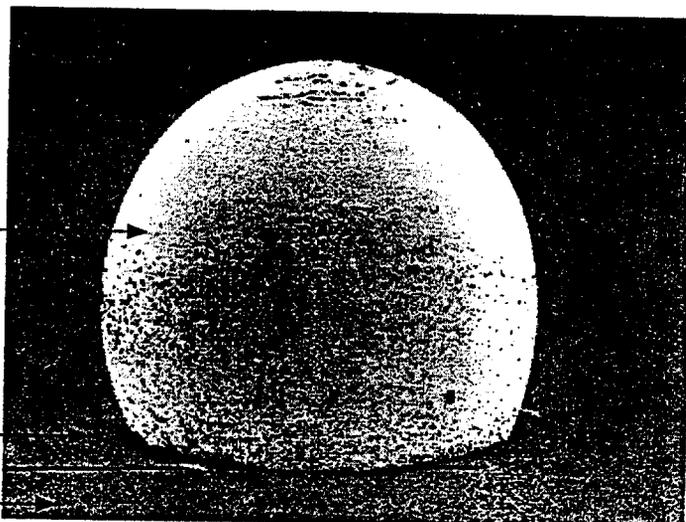
# Electroplated and Reflowed Eutectic Solder Bump

(scanning electron micrograph)

50  $\mu\text{m}$  diameter  
50  $\mu\text{m}$  high  
37/63 Pb-Sn  
solder bump

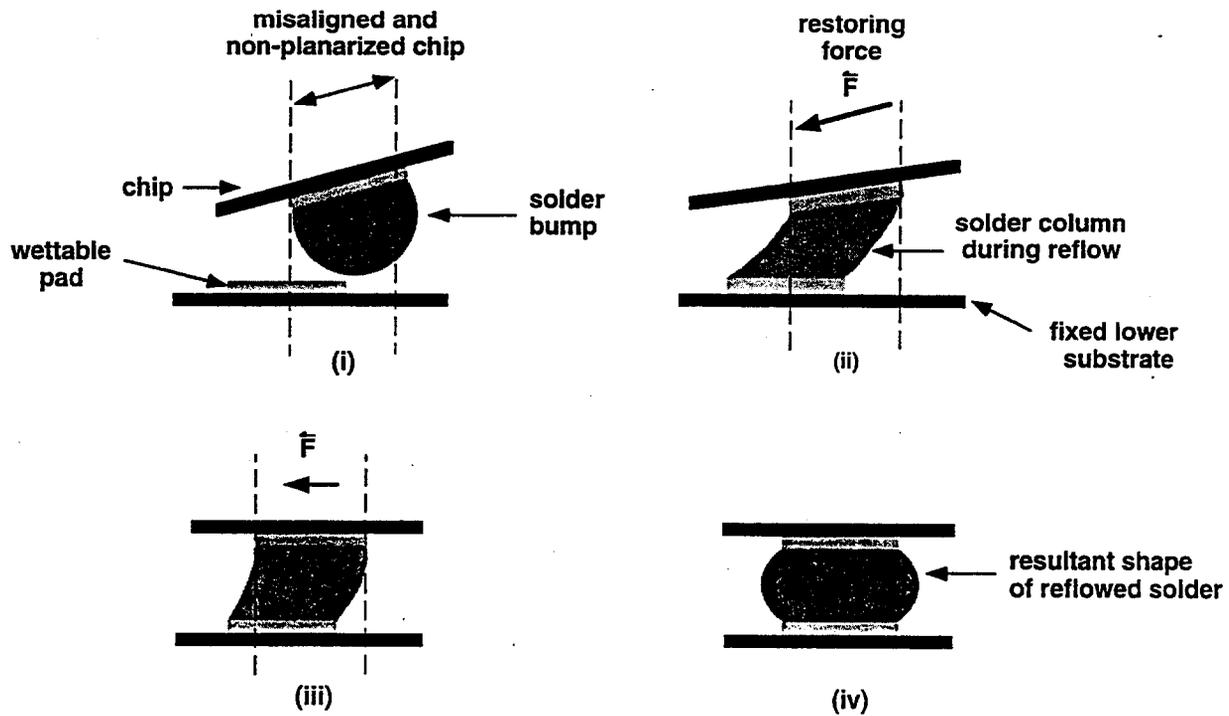
Cu pad

Si substrate

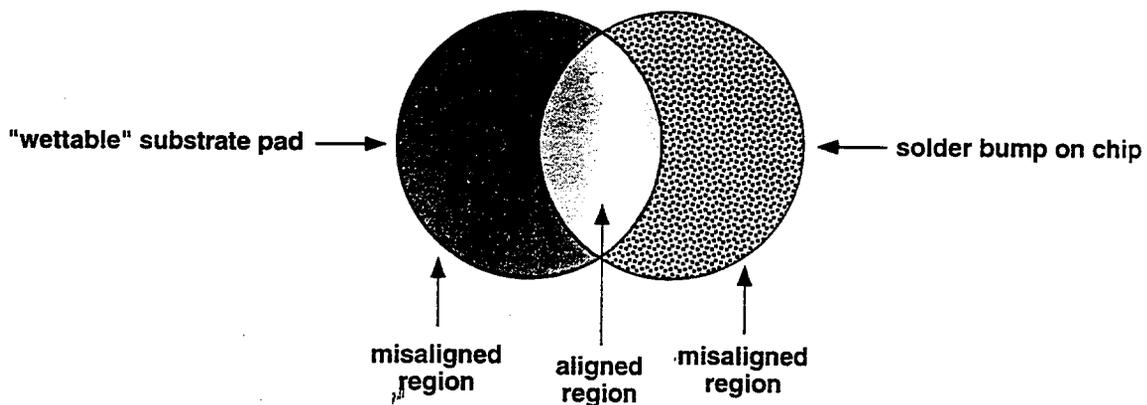


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# Self-Aligning/Planarizing Properties of Pb-Sn Solder Bumps



## Self-Aligning Properties of Pb-Sn Solder



- 1) Can tolerate about a 50% misalignment between the substrate pad and solder bumped chip
- 2) Can be used to self-align a solder bump to a wettable pad to within an accuracy of  $\pm 1 \mu\text{m}$

# **Flip-Chip & Bump Interconnect Technologies for Sensor Applications**

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## **Summary and Conclusions:**

- **Choice of indium or eutectic solder bumps for sensor/detector applications**
- **Indium has been proven effective, able to fabricate small bumps with fine pitch (by evaporation), soft and ductile bump, excellent mechanical characteristics, high-yields for both bumping and bonding, requires bumps on both sides, requires a flip-chip aligner/bonder with planarization, expensive to fabricate**
- **Solder bumps may provide an alternative if smaller bumps and finer pitches are achievable, versatile, eutectic solder has a reflow temperature of ~180°C, excellent electrical and mechanical characteristics, self-aligning and self-planarizing, requires a complex UBM, use of flux, lower fabrication cost in volume**



# Flip-chip Interconnection of 100k Pixel Hybrid Detectors

Dr Giles Humpston  
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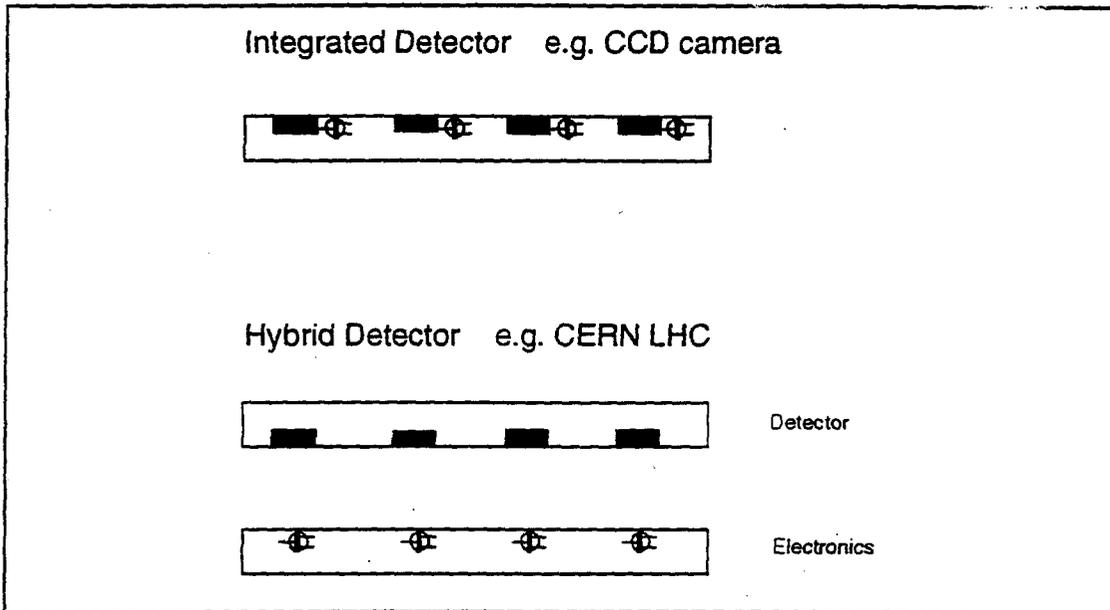
## Abstract

Hybrid detectors use different components for the sensor element and read-out electronics. This approach allows the detector to be optimised for collection efficiency and the read-out electronics for functionality, but places severe demands on the interconnect technology, especially if the detector is pixelated in two dimensions. Interconnection of fine-pitch (<50um), 2D hybrid pixel arrays is usually accomplished by either flip-chip compression bonding or flip-chip solder bonding.

GEC-Marconi Materials Technology offers a commercial portfolio of fine-pitch flip-chip interconnect technologies specifically for pixel detector manufacture. The service includes the option for each interconnect to be sub 10um diameter at below 20um pitch. The technology is discussed and application examples are presented including the CERN Omega-3 device and an advanced infra-red detector array containing over 100,000 elements.

## Introduction

Sensors can be made in two configurations. These are illustrated in Fig 1, below.



Integrated detectors are single component devices that combine the sensing element and the read-out electronics on a single substrate, usually silicon. A common example of this technology is the solid state optical detector (ccd) used in camcorders and digital cameras.

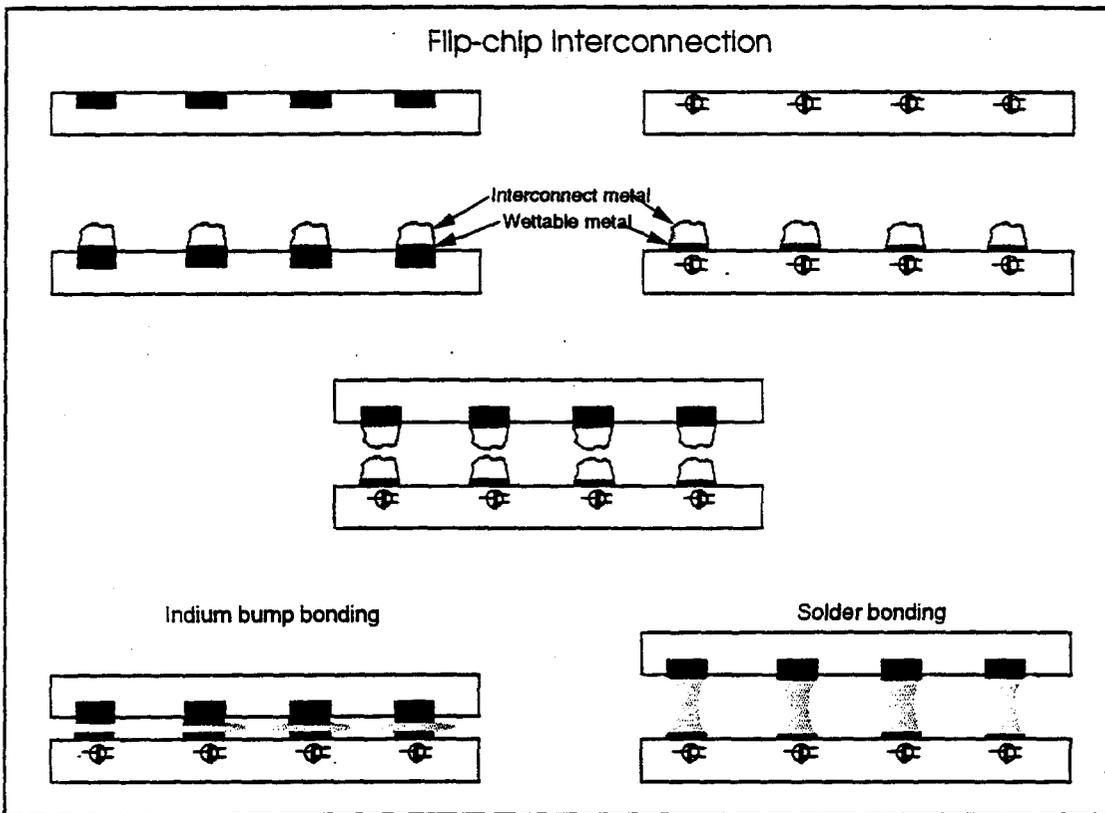
Hybrid detectors use different components for the sensor element and the read-out electronics. This approach allows the detector to be optimised for collection efficiency and the read-out electronics for functionality. A household example of this sensor type is the infra-red detectors used for burglar alarm systems. In these, the detector is a pyroelectric material (i.e. converts thermal energy to electrical charge), while the electronics system comprises a low noise amplifier and threshold gate.

Each pixel element in a hybrid detector needs to be connected to a separate electronics channel. If the hybrid detector is pixelated in two dimensions this places severe demands on the attachment and interconnect technology. Electrical interconnection and physical attachment of 2D hybrid pixel arrays is usually accomplished by flip-chip bonding.

## Flip-chip bonding

Flip-chip bonding is the leading method for attachment and interconnection of high performance semiconductor devices, including multi-chip modules (MCM), monolithic microwave integrated circuits (MMIC) and pixelated imaging detectors.

There are two process variants, flip-chip compression bonding (commonly known as indium bump bonding) and flip-chip solder bonding. The principle of these two process is shown schematically in Fig 2, below.



Both processes involve applying a "wetable metal" to the surface of the components to be joined. This is often a multi-layer metallisation, designed to provide ohmic contact to- and metallurgical compatibility between the contacts on the detector and read-out electronics. To the wettable metal on one or both component is then applied the interconnect metal. One of the die is then inverted (flipped over) and mating pairs of contact pads are aligned. This operation is performed on a flip-chip bonding machine. To perform flip-chip compression bonding the two components are then simply pressed together until interconnect metal welds. For flip-chip solder bonding, the assembly is heated until the interconnect metal melts and wets.

Although flip-chip compression bonding and flip-chip solder bonding superficially appear similar processes, they actually require very different

materials and process conditions, and the interconnects so formed have significantly different characteristics. The key features of each process and properties of the resulting interconnects are given in the following Tables.

	<b>Indium Bump Bonding</b>	<b>Solder Bump Bonding</b>
Process	Solid state diffusion	Solid-liquid alloying
Materials	In, Au, Pb, Pb/Sn	Any solder
Temperature	20-200°C	Solder melting point
Pressure	10 - 100 MPa	0 MPa
Max Height:Pitch	1 : 5	3 : 1

#### Technology Characteristics

<b>Indium Bump Bonding</b>	<b>Solder Bump Bonding</b>
Short (coin) interconnects	Tall (pillar) interconnects
Closed interconnect gap	Open interconnect gap
Fluxless	Flux required
Low residual stress	Residual stress
Service temp > bonding temp	Service temp < bonding temp
Alignment as placed	Self aligning ( $\pm 2\mu\text{m}$ X, Y $\pm 0.5\mu\text{m}$ Z)
Planar substrates	Topology tolerant

#### Fine-pitch Flip-chip

High resolution detectors require large numbers of small and densely packed pixels. If the interconnects can be larger than about 100 $\mu\text{m}$  diameter, a wide diversity of methods can be used to apply the wettable and interconnect metals to the components. The lowest cost option for volume manufacture is predominantly wet plating. For substantially smaller interconnects, especially those below 10 $\mu\text{m}$  diameter, the preferred approach is to exploit conventional semiconductor processing equipment and use photolithography to define features and vapour phase deposition to apply the wettable and interconnect metals.

GEC-Marconi Materials Technology, at Caswell, has over 25 years experience in fine-pitch flip-chip bonding and offers a state-of-the-art commercial service. Highly toleranced interconnections can be made for operation at over 40GHz on either whole wafers or individual known good die (KGD). Bumps can be made as high as 50um, for direct connection of integrated circuits to printed circuit boards, or smaller than 10um diameter for 2D detector arrays. Bump pitches can be below 20um. Equipment and facilities exist to provide advanced flip-chip bonding on a prototype scale through to volume production. This service is underpinned by extensive R&D resources, enabling one-off and highly specialised customer requirements to be met. An outline of this Service is given below.

<b>Process</b>	Indium- and solder-bump bonding
<b>Feature size</b>	10-100um dia., >10um between features, <50um high
<b>Substrates</b>	Single die - 6" wafers (300mm BY 1999)
<b>Interconnect</b>	Any commercially available metal or alloy
<b>Fluxes</b>	Reflow in choice of atm., custom flux design capability
<b>Flip-chip</b>	Full 5-axis alignment, 4 equipments
<b>Component size</b>	0.1mm to 100mm
<b>Underfill</b>	Any commercially available product
<b>Environment</b>	ESD protected Class 100 clean rooms
<b>Modelling</b>	RF, thermal, mechanical, static and transient

GMMT Fine-pitch Flip-chip Service

### Process Yield

Flip-chip is attractive for volume manufacturing applications because it is an inherently high yielding process. As an example, GEC-Marconi manufacturers a pixelated sensor that contains approximately 10,000 elements, in batches of 10 units. Of this batch of ten it would normally be expected that six have all interconnects made and functioning, while the remaining four units have a few isolated dead pixels. The pixel yield per batch therefore routinely exceeds 99.99%.

During process development, or occasionally during manufacture, it is obviously possible to produce pixelated devices with substantial numbers of non-working elements. Because flip-chip assembly is a well understood and characterised process, most failures can be readily diagnosed to a particular process deficiency, enabling corrective measures to be applied.

## Application Examples

### **LHC Omega-3 Pixel Sensors**

CERN has designed a family of pixel sensors to track the path and momentum of sub-atomic particles. These sensors essentially comprise an array of P-N junctions in silicon, GaAs or diamond, each of which is connected to an individual silicon electronics readout circuit. Because the detectors are relatively simple structures they can be physically large yet made with very low defect rates. The readout electronics, by contrast, are extremely sophisticated chips and producing die to the required specifications clearly presents a challenge to the wafer manufacturer. For this reason the sensor has been designed so that six readout die are used to populate each detector and the die are fully probe-tested before bonding.

In the current generation of Omega-3 prime sensor, electrical connection between the detector and the electronics chips requires approximately 13,000 flip-chip interconnects, each 18um diameter on a 50um by 500um pitch. As an additional complication, the interconnects are required to provide the maximum possible physical separation between the two components, to minimise electrical cross-talk. For this reason flip-chip solder bonding, using eutectic lead-tin solder, is employed by GEC-Marconi Materials Technology for the assembly process. Despite the complexity of this product, the yield of useable 'ladders' currently stands at about 75% and it is anticipated that some planned process enhancements will further improve this figure and decrease the cost.

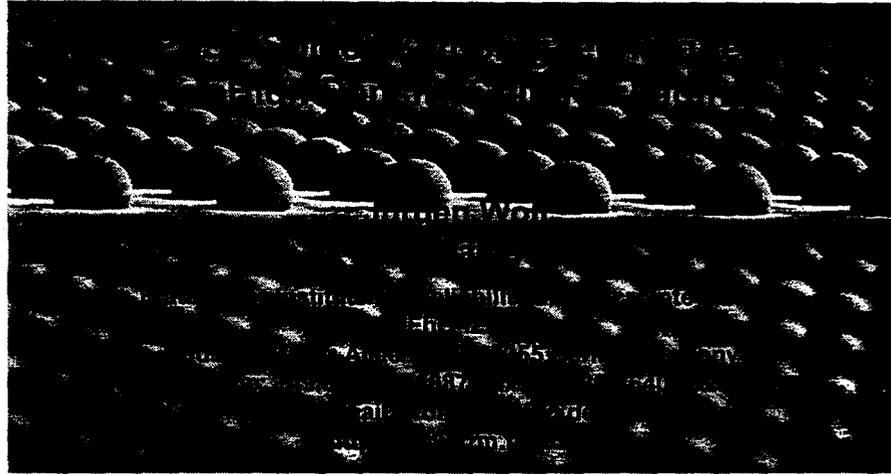
### **100k Pixel Hybrid Detectors**

A thermal imaging camera responds to heat, as opposed to light. The majority of thermal imaging cameras operate in the 8-14um wavelength of the infra-red band because the image is then not degraded by either smoke or rain. The quality or precision of the image that can be obtained from an infra-red camera is simply a function of the number of pixel elements (exactly as for a computer monitor albeit working in reverse!). However, if the sensor is too large then the quality of the picture again degrades due to deficiencies in the camera optics. The technology drive is therefore to pack the maximum number of pixels into the smallest possible area.

The infra-red detector used in this example is a pyroelectric ceramic. This approach has the merit that the camera can operate at room temperature. Traditional infra-red detectors must be cooled to about -200°C in order for them to function. The ceramic is manufactured in large blocks, then sliced and polished to eventually yield 8um thick wafers, which are then diced by laser into individual pixel elements. Electrical connection between each pixel element and the custom read-out electronics is achieved by flip-chip solder

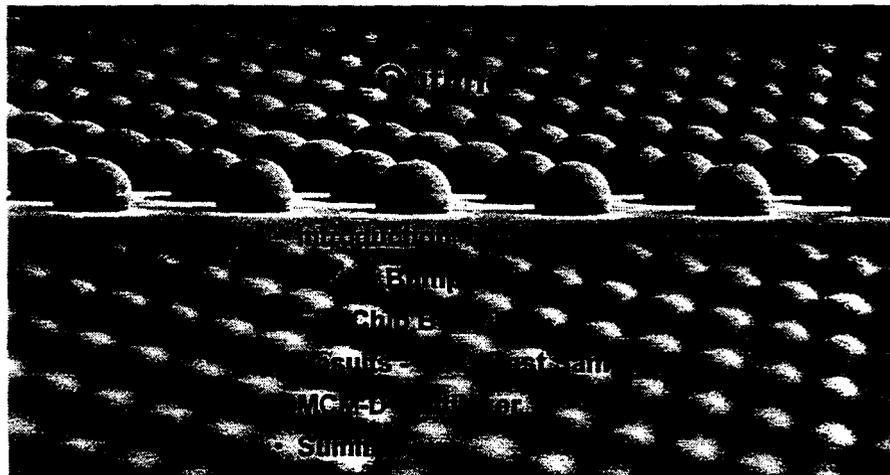
bonding. To minimise thermal leakage from the detector to the electronic die the solder interconnects are made as small as possible, and in this instance below 10um diameter. By exploiting fine-pitch flip-chip as the interconnection and assembly method it is possible to realise sensors that measure no larger than 1cm<sup>2</sup> but which contain in excess of 100,000 individual pixels. A lower resolution variant of this product is sold by GEC-Marconi Infra-red Limited for use by firemen, police and the rescue services.





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- research and development of advanced assemblies and packages
- prototyping and low volume production
- tutorials, seminars and consulting

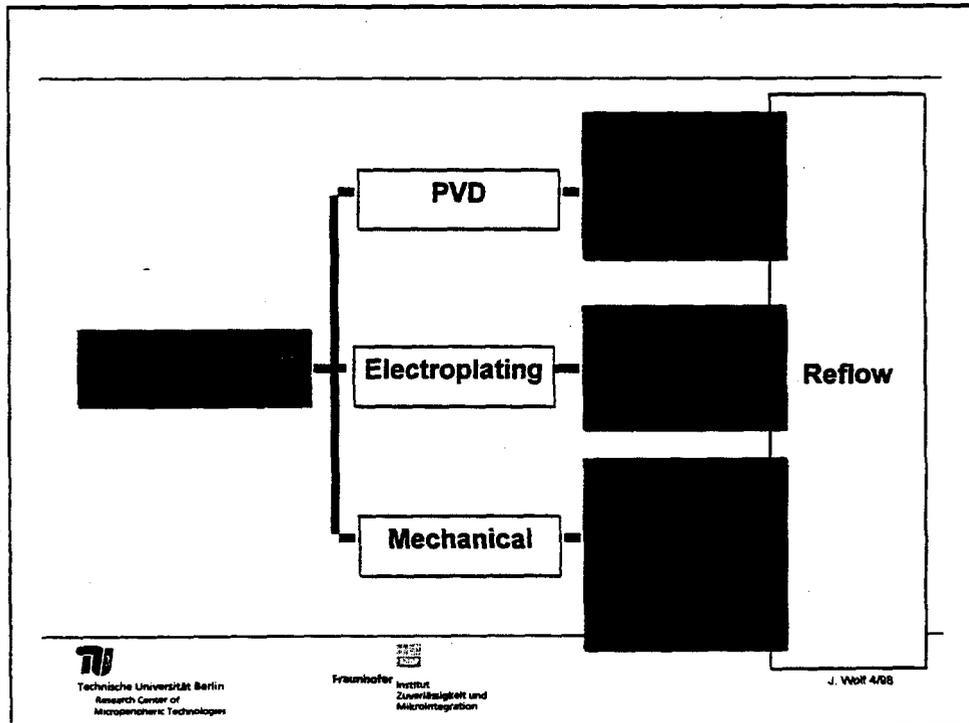
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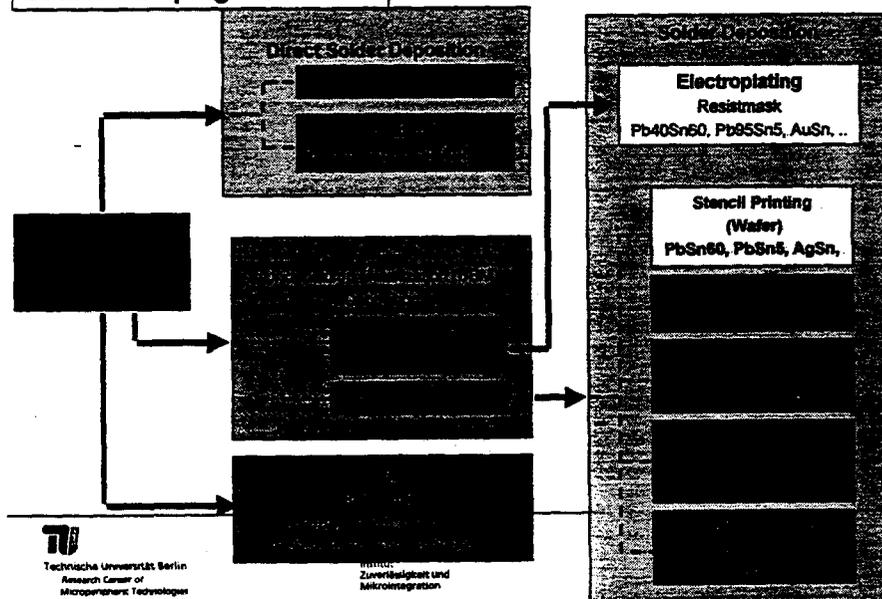


## Flip Chip Bumping

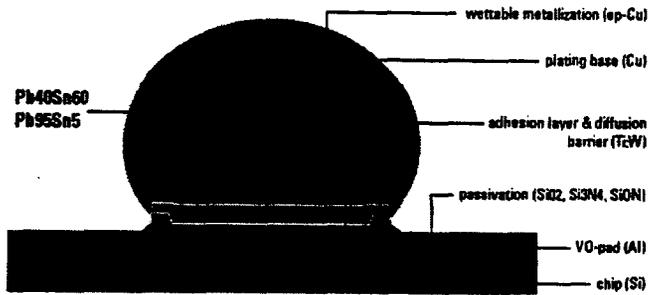
### Bumping Methods

<b>Sputtering / Evaporation</b> → longest experience	➔	<b>C4 Technology</b> CrCu/PbSn5
<b>Sputtering / Electroplating</b> → very fine pitches	➔	<b>Galvanic Bumping</b> Au, PbSn, AuSn etc.
<b>Electroless / Printing</b> → high throughput	➔	<b>Low Cost Bumping</b> NiAu/PbSn
<b>Mechanical</b> → single chips	➔	<b>Stud Bumping</b> Au

## Solder Bumping ROADMAP



## PbSn Solder Bump Structure



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## Solder Bump Structure

### UBM

#### Adhesion-Layer & Diffusion Barrier

- hermetic coverage of the chip pad
- good adhesion to Al chip pad
- minimum interdiffusion between bump metal and chip pad
- low degradation during temperature cycles imposed during reflow, bonding
- low internal stress
- low contact resistance

#### Solder Base

- sufficient wettability to the solder
- tolerable formation of intermetallics at the interface

#### Solder (e.g. PbSn63, PbSn5)

- mechanical contact to substrate
- stand-off chip-substrate
- good electrical contact
- high creep resistance to improve reliability under thermal loading
- high ductility to minimize mechanical stress due to different CTE of substrate and chip



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## Under Bump Metallization (UBM)

Layer	Material	Thickness	C 4 (IBM)	IZM /TUB
Adhesion-Layer Diffusion Barrier	Ti, Cr	(30-200) nm	Cr [150 nm]	Ti:W [200-nm]
(Plating Base)	Cu, Au, Ni, Pd	(200-200) nm	Cr /Cu [150 nm]	Cu [300 nm]
Wettable Layer	Cu, Ni	(1 - 5) $\mu$ m	Cu [1000 nm]	Cu [ 5 $\mu$ m]
Oxidation Protection	Au	(100-200) nm	Au [100 nm]	

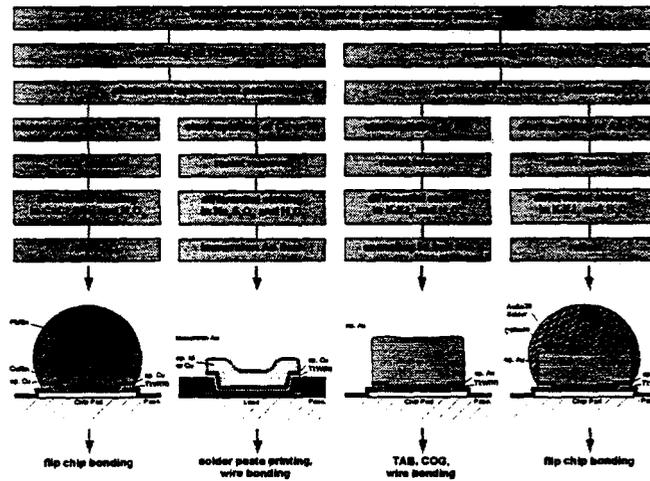


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## Electroplating Bumping Techniques



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## Technology Determination

### Project ATLAS

Si substrate & chip  
Si<sub>3</sub>N<sub>4</sub> / SiON passivation  
I/O-pad: Al  
small I/O-size & pitch (50 μm)  
no 2nd soldering level



Bump Structure:  
eutectic lead/tin solder  
UBM: Ti:W/Cu



Technology:  
Solder Deposition using electroplating and  
photoresist mask technique



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## Processflow PbSn-Bumping using Electroplating

Sputter Etching and Sputtering  
of the Plating Base / UBM



Electroplating of Cu and PbSn



Spin Coating and Printing  
of Photoresist



Resist Stripping and wet Etching  
of the Plating Base



Reflow



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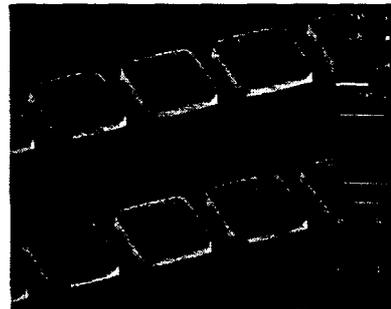
## Electroplating

	Cu electrolyte	PbSn electrolyte
contents	CuSO <sub>4</sub> , sulfonic acid, chloric acid, grain refiner and leveler, wetting agent	Sn(CH <sub>3</sub> SO <sub>3</sub> ) <sub>2</sub> , Pb(CH <sub>3</sub> SO <sub>3</sub> ) <sub>2</sub> , methane sulfonic acid, grain refiner, wetting agent, oxidation inhibitor
metal concentration	20 g/l Cu	total of 28 g/l
temperature	25 °C	25 °C
agitation	2...5 l/min	3 l/min
pH value	< 1	< 1
current density	10...30 mA/cm <sup>2</sup>	20 mA/cm <sup>2</sup>
plating rate	0.22...0.88 µm/min	1 µm/min
current efficiency	nearly 100 %	nearly 100 %
hardness of deposit	80...100 HV <sub>0.025</sub>	around 10 HV <sub>0.025</sub>
appearance of deposit	glossy	mat
anode material	phosphorus-alloyed copper	appropriate Pb/Sn alloys

## AU Bumping



Resist (AZ 4562)  
thickness: 33 µm



Au-Bumps after Deposition  
and Resist Stripping  
Bump Size: 110 µm x 110 µm  
Space: 30 µm

## AU Bumping



Electroplated Au bumps  
height: 20 µm, diameter: 15 µm

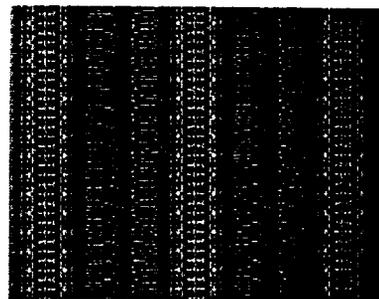
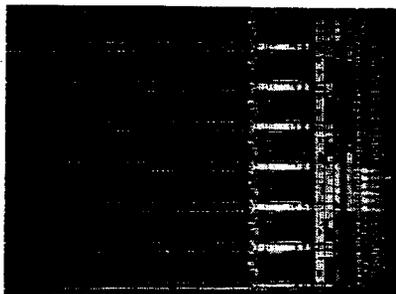


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## Solder Bumping Pb40Sn60



Read out Si-chip (Uni Bonn) with Solder Bumps  
after Reflow  
UBM: Ti:W/Cu / ep.Cu (5µm)



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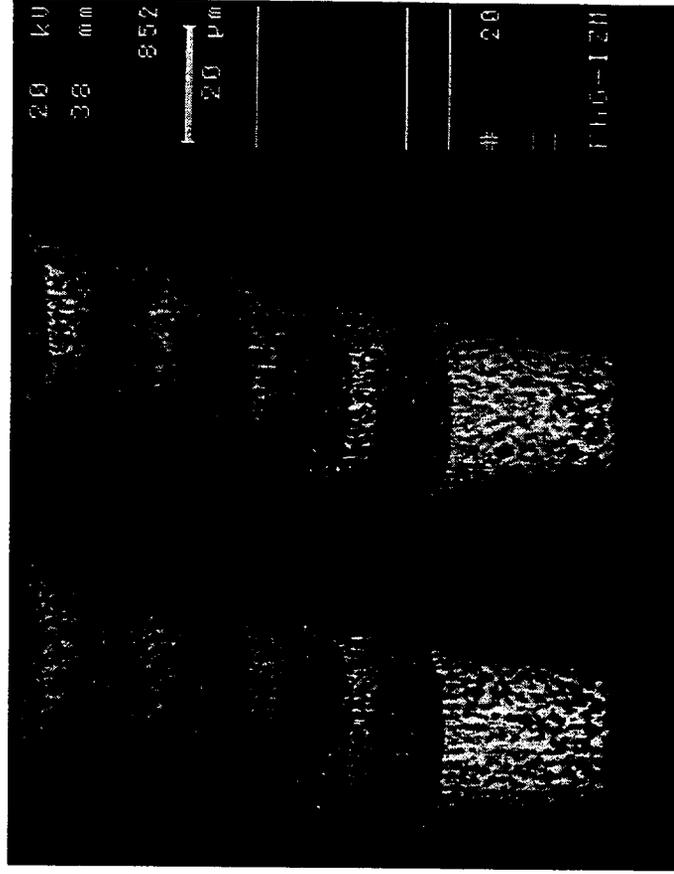
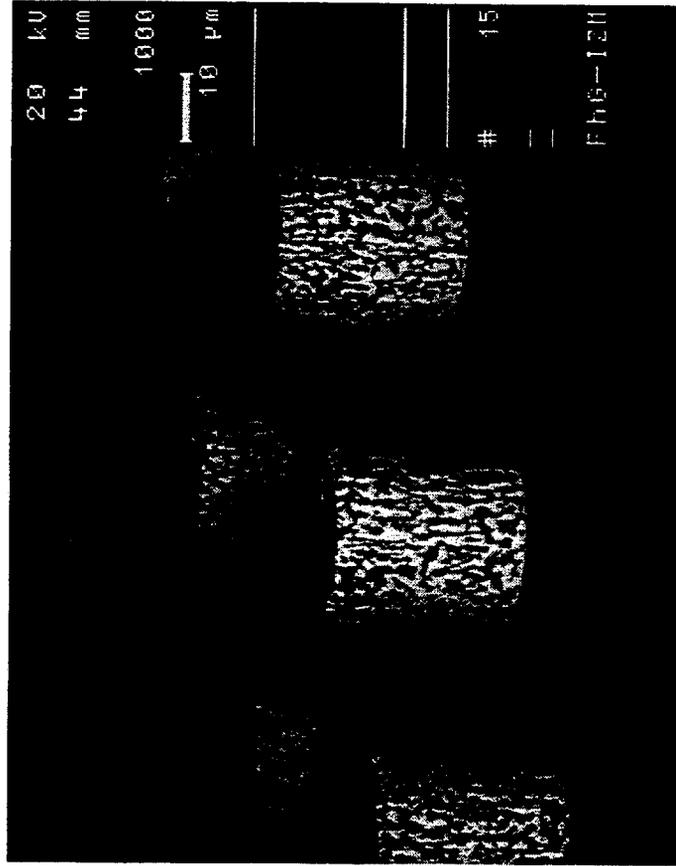


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# Solder Bumping - Pb40Sn60



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**Solder Bumps after Electroplating**  
**UBM: Ti:W/Cu / ep.Cu (5µm)**  
**Solder: Pb40Sn60**



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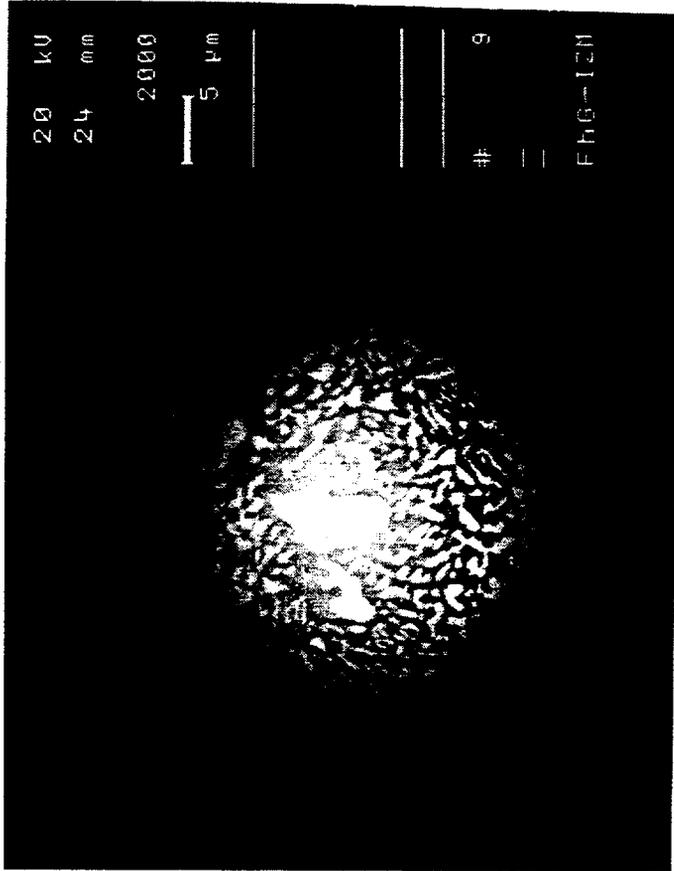
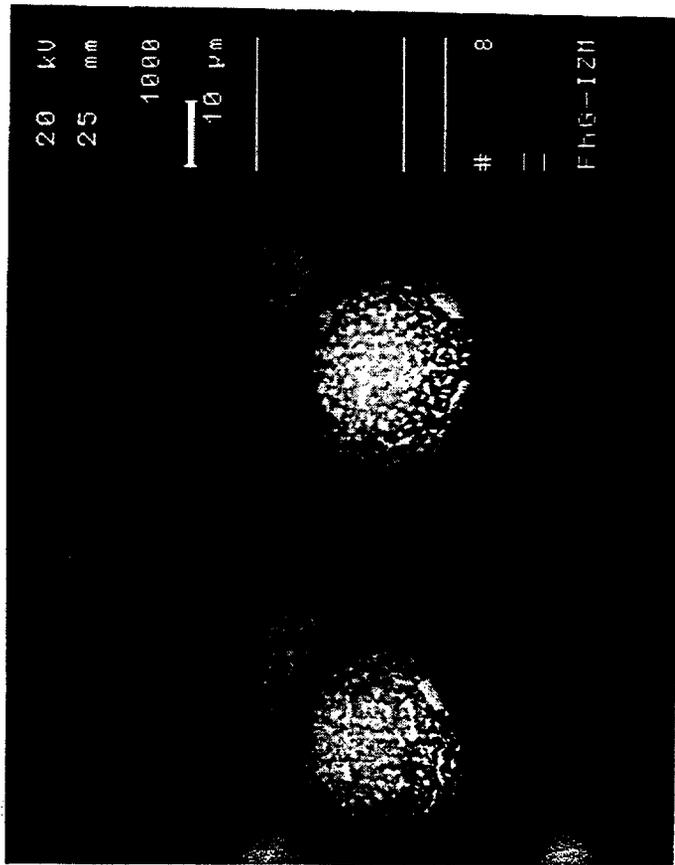
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Department: Multichip Modules  
Bumping  
J. Wolf, I.D.'97

SN60-AT3.DOC



## Solder Bumping - Pb40Sn60



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Solder Bumps after Reflow  
UBM: Ti:W/Cu / ep.Cu (5µm)  
Solder: Pb40Sn60

Department: Multichip Modules  
Bumping  
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SN60-ATT.DOC

## Solder Bump Reflow

Oxidelayers must be removed to allow solderball formation

Use of aggressive fluxes must be avoided

Melting point:  $T_m = 314^\circ\text{C}$  (95/5 wt% Pb/Sn),  
 $T_m = 183^\circ\text{C}$  (37/63 wt% Pb/Sn)

### Reflow methods:

Heating under active atmosphere  
 Using Flux (RMA)

### Some fluxless reflow methods:

Heating under reducing atmosphere  
 - 100 %  $\text{H}_2$   
 - 95 %  $\text{N}_2$  / 5 %  $\text{H}_2$  (not sufficient)  
 (Reflow in vacuum)  
 (Reflow after Sputteretching or RIE)

Process: Pb40Sn60 (PbSn5)

Heating in a organic medium up to 240 (350) °C  
 followed by cleaning procedure

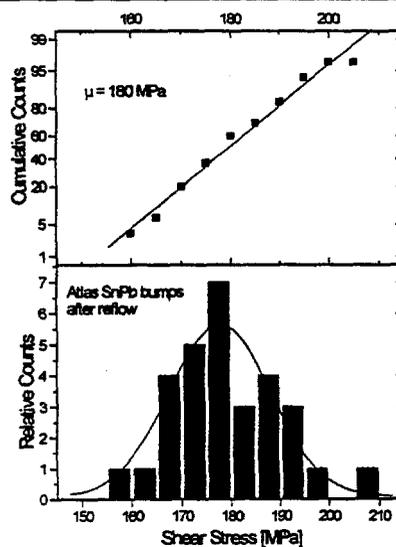


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## Under Bump Metallization (UBM)



### Bump Inspection after Deposition & Reflow (Pb40Sn60)

Wafer #	Chip defect # 61	%	Bump defect # 189588	ppm
2594/56	3	4,92	16	84,39
2594/57	0	0,00	0	0,00
2594/58	3	4,92	18	94,94
2594/60	0	0,00	0	0,00
2594/61	2	3,28	5	26,37
2594/64	2	3,28	3	15,82
2596/16	0	0,00	0	0,00
2596/17	2	3,28	15	79,12
2596/18	3	4,92	6	31,65
2596/21	2	3,28	6	31,65
	1,70	2,79	6,90	36,39

defect rate:  $3.64 \times 10^{-5}$   
 total number of bumps: 1895880  
 bump defects: 69



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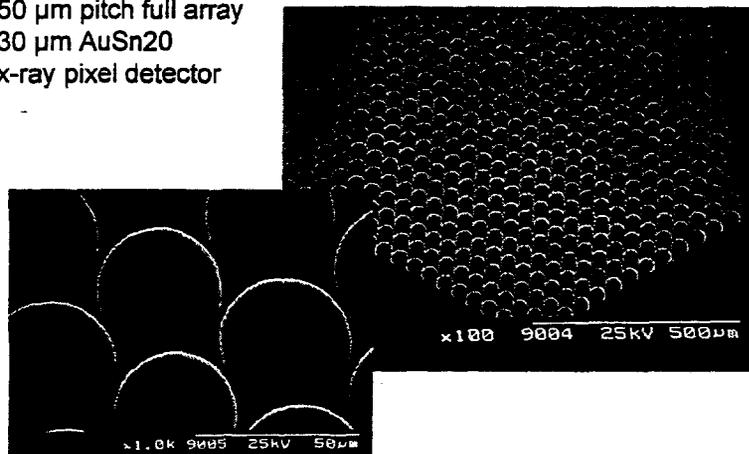


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### Solder Bumping

#### Electroplated Bumps

- 50  $\mu\text{m}$  pitch full array
- 30  $\mu\text{m}$  AuSn20
- x-ray pixel detector

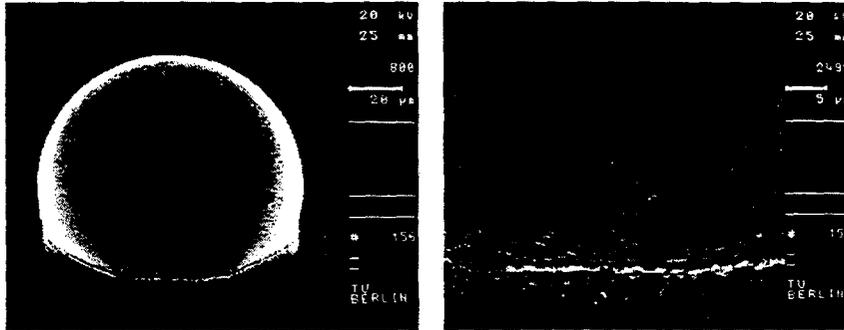


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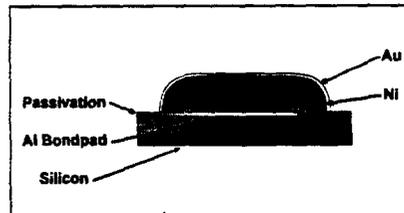
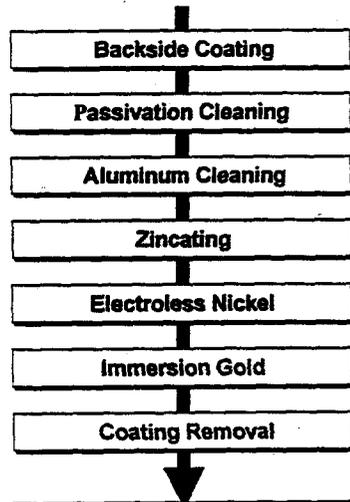
## Solder Bumping Pb95Sn5



Solder Bump (Pb95Sn5) after Reflow  
UBM: Ti:W/Cu / ep.Cu (5μm)

## Solder Bumping

### Process Flow

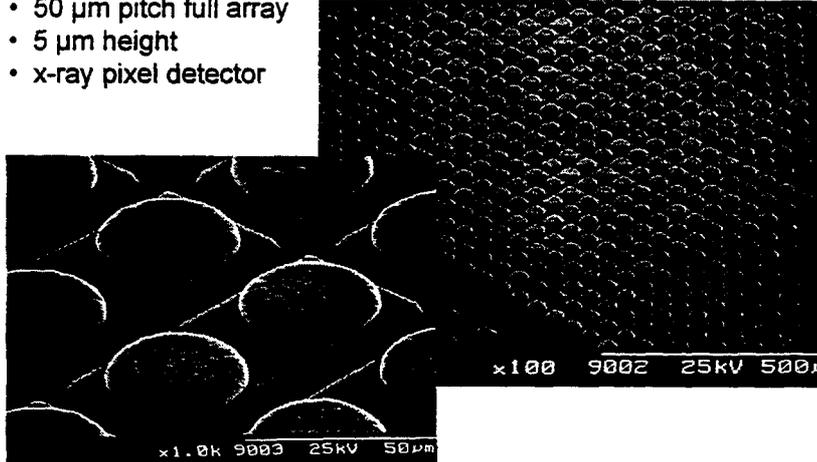


Electroless Ni/Au UBM

## Solder Bumping

### Electroless Ni/Au UBM

- 50  $\mu\text{m}$  pitch full array
- 5  $\mu\text{m}$  height
- x-ray pixel detector

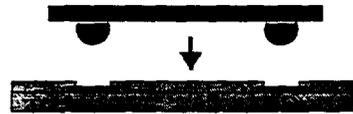


## Flip Chip Assembly

### Flip Chip Techniques

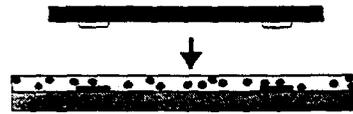
#### soldering

UBMs: TiW/Cu, Cr/Cu, Ni/Au  
solders: Pb40Sn60, Pb95Sn5, SnAg,  
AuSn, In  
substrates: ceramics, FR4, flex



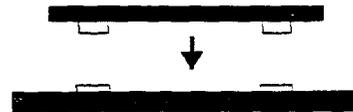
#### adhesive joining

bumps: Au, Ni/Au  
adhesives: isotropic, anisotropic  
substrates: glass, flex, FR4



#### thermo-compression

bumps: Au  
substrate: silicon, ceramics



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## Flip Chip Assembly /1/

### Pixel Detector Module

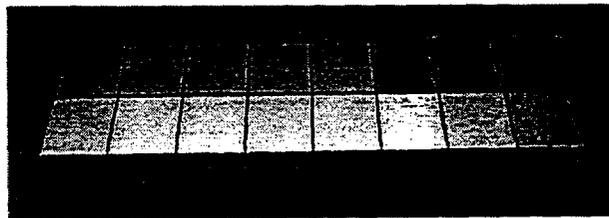
Detector substrate: 61.440 I/Os,

electroless Ni/Au (version 1)  
electroplated Ti:W/Cu (version 2)

### 16 Read-Out Chips

24 rows, 160 I/Os

50  $\mu\text{m}$  x 300  $\mu\text{m}$  pitch  
Solder Bumps: Ti:W/Cu - ep.Cu - PbSn



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## Pixel Detector Module

Detector Tile 1 (Chip-Up)	62.4 x 17.0 mm <sup>2</sup> , chip/detector ratio: 112 %
Detector Tile 2 (Chip-Down)	62.4 x 24.4 mm <sup>2</sup> , chip/detector ratio: 78 %
Read-Out Electronic Chips	7.4 x 10.0 mm <sup>2</sup>
Chips per Module	16
Chip to Chip Distance	200 μm
Pixel Cells per Module	61.440
I/O Pattern (equal to Pixel Size)	50 x 300 μm
Total Numbers (3 Barrels)	2.37 m <sup>2</sup> Module Area, 1,534 Detector Modules 24,544 Read-Out Chips 94,248,960 I/O's



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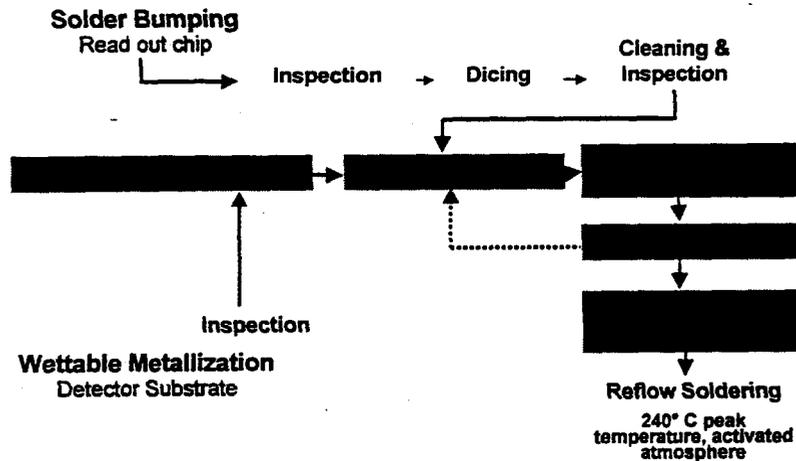


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## Flip Chip Assembly

### Process Flow

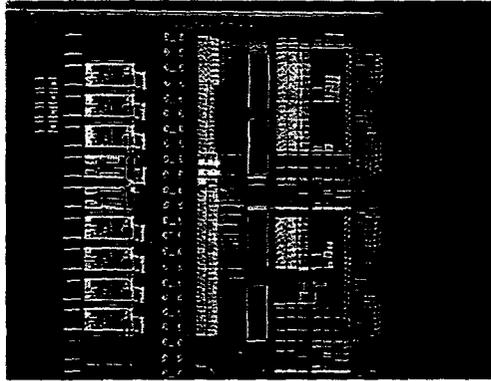


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## Flip Chip Assembly



Read out die flip chip bonded  
on Si-detector substrate

## Flip Chip Assembly



Read out die flip chip bonded  
on Si-detector substrate (single tile)

## Flip Chip Assembly - Yield /1/

### Electroless Ni/Au Metallization

Yield Evaluation of Detector Wafer by CERN partners				
wafer	bumps	failures	failure rate	remarks
-59	96,384	1	10 ppm	passivation failure (cracks)
-21	96,384	29	300 ppm	passivation failure (cracks, scratches)
-57	96,384	0	0	no failures
-22	96,384	0	0	no failures
Total	385,536	30	78 ppm	relevant failures

Electroless Nickel/Gold  
sensitive to passivation failures

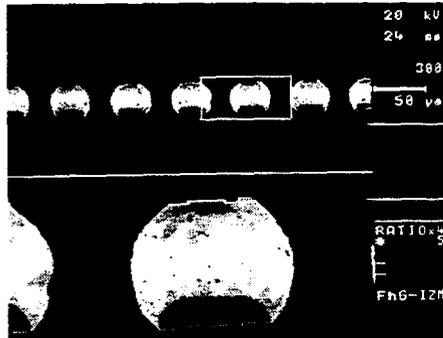


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## Flip Chip Assembly /1/



Chip wafer  
UBM: Ti:W/Cu - ep. Cu  
solder PbSn (eutect.)

Detector Si Substrate  
passivation: Si<sub>3</sub>N<sub>4</sub>  
wettable metallization:  
electroless Ni /Au



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## Flip Chip Assembly - Yield /2/

Overall Yield Evaluation of the Assembled Module by CERN partners				
substrate	metallization	tests points	failures	failure rate
-21	Ni/Au	25,920	2	77 ppm
-22	Ni/Au	25,920	0	0
-59	Ni/Au	25,920	2	77 ppm
-28	Cu	25,920	0	0
-17	Cu	25,920	0	0
<b>Total</b>		<b>129,600</b>	<b>4</b>	<b>31 ppm</b>

Overall yield includes  
substrate, bumping and assembly yield.



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## Flip Chip Assembly - Multilayer Substrate



**Chip**  
Al/(Cu) routing, passivation  
Bump: Solder PbSn (eutect.)  
UBM: Ti:W/Cu - ep. Cu  
**Si Substrate**  
Multilayer of 5 metal & 5 dielectric layers  
Dielectric: Photo-BCB: 5 µm thick, 25 µm vias  
Metallization: Ti:W/Cu - ep. Cu (2 µm)



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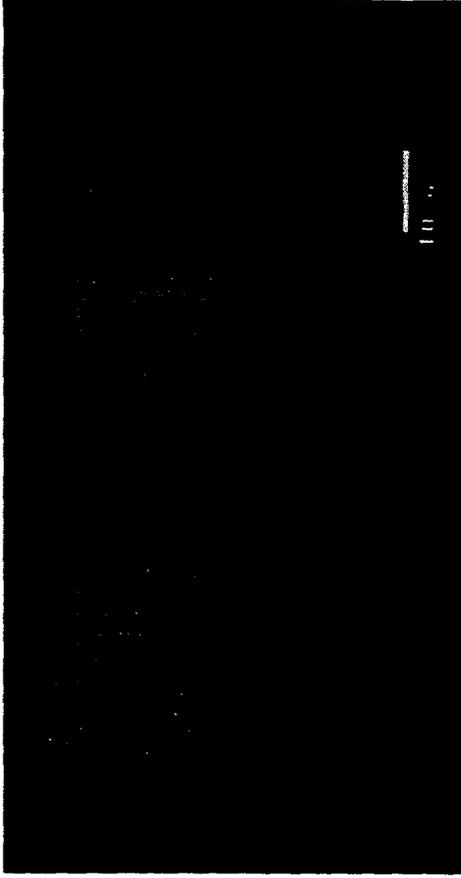
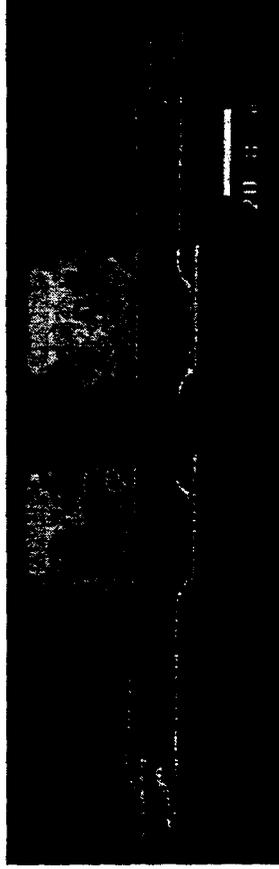




# MCM-D Technology - High Dense Flip Chip



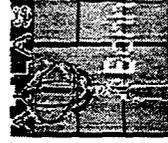
**Multilayer of 5 metal & 5 dielectric layers**  
**Dielectric: Photo-BCB: 5  $\mu\text{m}$  thick, 25  $\mu\text{m}$  vias**  
**Metallization: Ti:W/Cu - ep. Cu (2  $\mu\text{m}$ )**



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Department: Multichip Modules  
JW, OE '98  
FC-AT\_1.DOC



# MCM-D Technology

## Via Yield for Multilayer Substrate

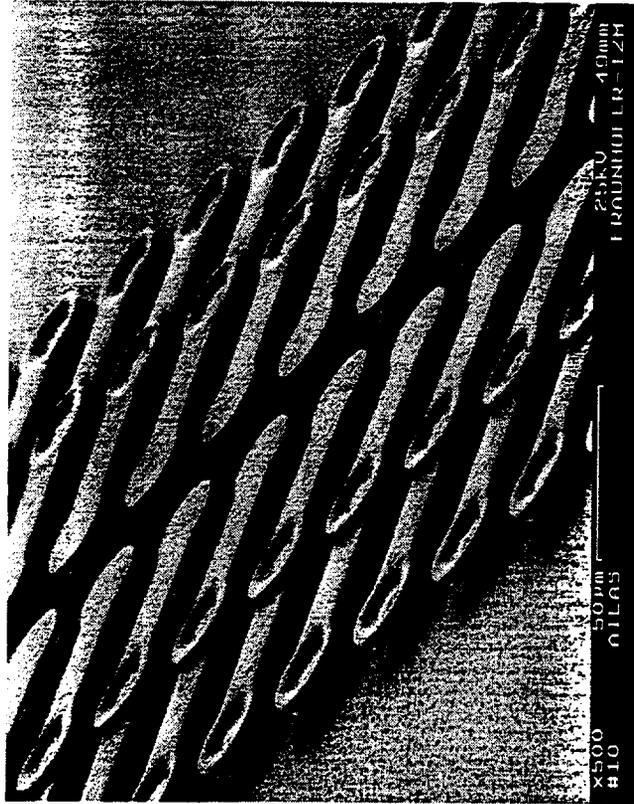
160 substrate contacts per row  
 x 18 rows per chip  
 = 2880 contacts per chip  
 x 16 chips per tile  
 = 46080 contacts per tile  
 x 6 tiles measured  
 = 276 480 contacts  
 x 4 metallization layers

$276\,480 \times 4 = 1\,105\,920$  vias monitored

9 defects



defect rate: 8.13 E-6



**Multilayer of 5 metal and 5 dielectric layers**  
**[dielectric BCB etched for visualization]**



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## Electrolityc Flip-Chip Technology for Large Particle Detector

Dr. Stéphane RENARD - CEO

TRONIC'S MICROSYSTEMS S.A.  
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FRANCE

Phone : +33 4 76 88 56 86

Fax : +33 4 76 88 54 04

e-mail : Stephane.Renard@cea.fr

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## Electrolityc Flip-Chip Technology for Large Particle Detector

CEA/LETI - Flip Chip technology developing since 1991

■ Two different technologies :

- Lift-off            ++ pitch < 50  $\mu$ m    -- high cost
- electroplating    -- pitch > 50  $\mu$ m    ++ low cost

■ Many prototype devices have been achieved :

- Infra-Red detectors
- X and Gamma detectors
- Chip on glass for flat-panel-displays drivers
- High resolution MCM's

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2

605



## Electrolytic Flip-Chip Technology for Large Particle Detector

### TRONIC'S MICROSYSTEMS S.A.

Start up company from LETI, created in May 97.  
Production facilities shared with CEA/LETI.

#### ■ Activities

- Wafer manufacturing of sensing elements (pressure, acceleration, magnetic field...) for microsystems.
- Bumping of IC wafers and high resolution MCM's.
- Medical microsystems under development.

#### ■ Active technologies

- Silicon Bulk Micromachining
- Epi SOI Surface Micromachining
- Electroplating Sn/Pb or In for Flip-Chip Technologies

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## Process Flow Chart (1)

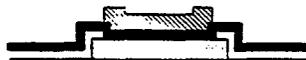
- IC Aluminum Pad Cleaning



- TiNiAu Sputtering Deposition



- Resist Coating, Insulation and Development



- TiNiAu Etching



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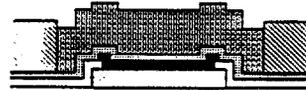
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## Process Flow Chart (2)

- Thin Metallic Layer Deposition
- Thick Resist Coating, Insulation and Development
- Solder Electroplating



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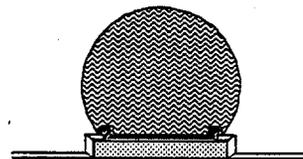
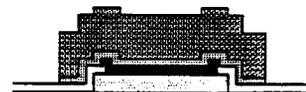
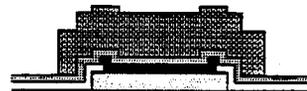
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## Process Flow Chart (3)

- Resist Stripping
- Thin Metallic Layer Etching
- Solder Fusing



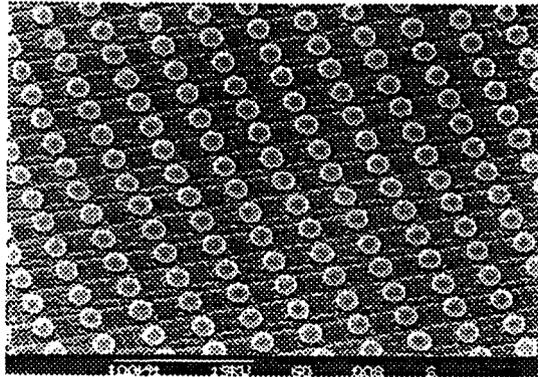
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## Electrolitic Flip-Chip Technology for Large Particle Detector



S.E.M. VIEWGRAPH OF A BUMP ARRAY ON IC

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## Electrolitic Flip-Chip Technology for Large Particle Detector

TRONIC'S / CPPM COLLABORATION FOR ATLAS PIXEL DETECTORS

	Detector size (mm)	Lead-out K. size (mm)	Wire bonding
TRONIC	820 x 100	7.5 x 15	On the read-out chip
CPPM	620 x 100	7.4 x 11	On the detector

Each IC comprises 18 rows of 162 bonding pads

Pad pitch : 50  $\mu\text{m}$       Detector thickness : 300 / 200  $\mu\text{m}$   
Row pitch : 400  $\mu\text{m}$       IC thickness : 500 / 300  $\mu\text{m}$

Number of pads / detector : 46 656

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## Electrolytic Flip-Chip Technology for Large Particle Detector

### Conclusion

- The characterization results show only a few ponctual defects per detector
- Electroplating flip chip technology process is a good candidate for bump-bonding Atlas pixel detector



# Inner Tracker and L1 Trigger Based on Pixel Detectors for DØ33

Sudhindra Mani

*University of California, Davis*

Meenakshi Narain

*Fermi National Accelerator Laboratory*

## 1 Introduction

The upgraded DØ detector [1] for run II will have a new magnetic tracker in the cylindrical volume of 1 m diameter within the calorimeter cryostat. The pattern recognition will be done by the outer scintillating fibers, while the inner silicon strip tracker will be used to reconstruct the various interaction and decay vertices in the event. Both of these trackers contribute to the momentum resolution of the device.

The fiber tracker is also used to form a level 1 (L1) lepton trigger based on the presence of a high  $p_T$  track in coincidence with either an electromagnetic shower or a track-stub in the muon system [2]. The tracker trigger itself is formed by requiring simple coincidences amongst binary signals from the scintillating fibers. It is a massively parallel and pipelined (fully synchronous) system that is implemented in commercial FPGA's [3].

Occupancy related problems for this trigger have been seen in our simulations for luminosities exceeding  $10^{32} s^{-1} cm^{-2}$  at a 396 ns beam crossing interval, or equivalently, an average of 3 or more interactions per crossing. With the proposed increase in luminosity to  $10^{33} s^{-1} cm^{-2}$  in run III (albeit, with a 132 ns crossing time), the occupancy related problems will resurface, even with the so-called luminosity levelling scheme. Furthermore, higher radiation levels will damage some tracker components beyond their tolerance limits.

Introducing silicon pixel detectors into the inner most layers of the tracker solves both problems, namely, radiation damage and high occupancy. The DØ collaboration has proposed a pixel based tracker for the region inside a radius of 10 cm [4]. Figure 1 shows the redistribution of technologies employed within the tracker volume. In this article we discuss some key technical aspects of a strawman design for the inner pixel tracker.

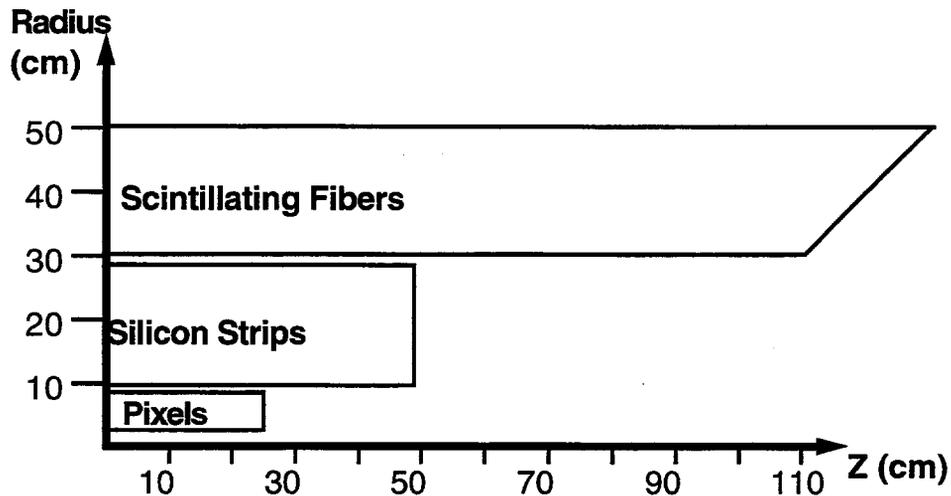


Figure 1: Strawman Tracker for DØ33. The inner fiber layers have been replaced by silicon strips which have themselves moved radially to make room for inner pixel layers. Forward tracker components are not shown.

## 2 Track Trigger Issues

It is desirable to solve the occupancy problems at the *L1 trigger level* as well. Hence, we also examine the possibility of having an L0 trigger pickoff in the pixel detector readout and feeding those data into the fiber tracker trigger electronics to arrive at a composite L1 trigger.

Recent studies within DØ [6] have shown that a silicon tracker based L2 trigger (STT) can be used for selecting events containing secondary vertices, thereby providing samples rich in various physics processes. The data from the silicon can also be used to find the higher  $p_T$  primary interaction vertex along the beam direction in the presence of multiple interactions [7]. Encouraged by these findings, we have been led to consider such a trigger using data from pixels. This will naturally lead to implementing a *b*-quark trigger which in conjunction with the presence of high  $p_T$  jets and/or missing  $E_T$  will be able to recognize, for example, production of top quarks, massive vector bosons, SUSY particles or Higgs.

We note that with adequate segmentation a pixel tracker can maintain the tracking resolution (especially at L1, where only binary data are available) that is provided by the fiber tracker of run II. The fiber tracker has a 30 cm radial lever arm and a 900 micron segmentation along the azimuth in each layer. Simple scaling (ignoring the effects of multiple coulomb scattering for tracks above 10 GeV/c) shows that a pixel tracker

with a 30 micron segmentation will require a 5.4 cm lever arm to obtain the same sagitta resolution. Hence, if the inner detectors are placed at a radius of 2.3 cm, the entire pixel tracker will fit well inside the designated 10 cm radius, leaving about 2.3 cm for cable routing. This is shown in figure 2 and described in detail later. Hence, it can be argued that if the technology can achieve this 30 micron pitch, pixels will be able to augment the fibers as the trigger element for high  $p_T$  leptons. Of course, with at least an order of magnitude more detection elements, the pixels will have substantially higher pattern recognition power compared to fibers.

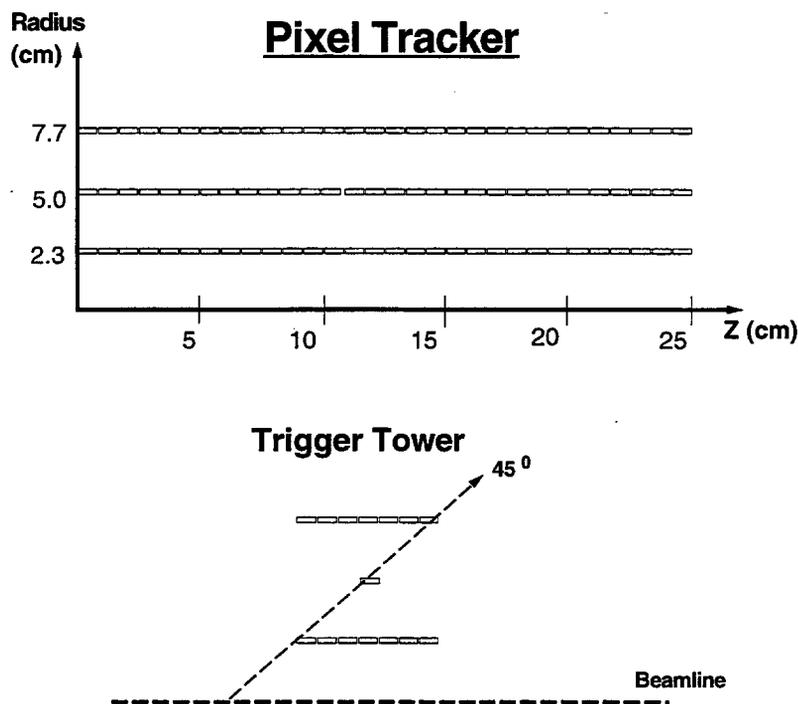


Figure 2: A 3 layer pixel tracker layout composed of  $1\text{cm}^2$  tiles. Logical towers can be defined for triggering purposes.

We further argue that these improvements to the trigger should be implemented at L1 because  $D\phi$  has a limited bandwidth ( $< 10$  kHz design goal for run II) into L2. It is likely that in run III we will continue to use trigger strategies similar to run II, ie, build L1 triggers using information from the calorimeter, muon system and the fiber tracker. The minimal high- $p_T$  trigger menu is expected to require a bandwidth at the L1 trigger close to 5kHz during run II.

Various Tevatron running scenarios during run III indicate a dramatic increase (upto a

factor of 4) in the expected number of events per crossing compared to run II. All triggers which incorporate a term based on calorimeter information are expected to increase by 30–40% for an average of 5 interactions per crossing. However, we expect rather large increases (factors of 4–10) in muon and CFT based triggers. This would result in the high  $p_T$  menu requiring a bandwidth of at least 15–20 kHz at the L1 trigger stage, which is currently a factor of 1.5–2 larger than the design goals of the L1 trigger system. Hence, only a higher rejection at a lower trigger level allows us to avoid prescaling and write all interesting physics events to tape.

The muon and CFT based triggers suffer a loss of rejection power primarily due to high occupancy with increasing number of interactions in the event. Adding information from the pixel tracker will be beneficial in alleviating this problem by improving the pattern recognition at the trigger level.

In summary, a pixel tracker not only eases overall problems due to occupancy and radiation damage but, if exploited at L1, the data from the pixels add rejection power to both the CFT and the STT triggers.

### 3 Physics Motivation and Trigger Concept

As mentioned earlier, various studies [6] have established the usefulness of an impact parameter trigger based on including the information from the silicon tracker at the L2 stage of the trigger during run II. This information also helps achieve gains in the momentum resolution for high- $p_T$  tracks.

The proposed pixel tracker has similar (*or better*) resolution compared to the strip tracker and hence all the studies are applicable. As is the case for tracks reconstructed at L2 in run II, we expect a pixel based trigger to improve the momentum resolution for high  $p_T$  tracks at L1. However, there is one major difference. L2 triggers in run II will operate on all tracks above some minimum  $p_T$  threshold (provided by the CFT) which can be as low as 1.5 GeV/c. The total rate at such a low threshold may be prohibitive for an L1 trigger in run III.

The L1 pixel based trigger, proposed here, is designed to provide additional power to trigger on high  $p_T$  displaced tracks from heavy quark jets. We utilize the “natural”  $p_T$  threshold of the tracker, ie, the  $p_T$  above which the tracker is unable to distinguish the track from an infinite momentum straight line. For the CFT trigger this occurs at about 11 GeV/c. Since we have scaled the pixel tracker to the CFT (see above), we can use this same threshold in our studies. The usefulness of this straight line threshold lies

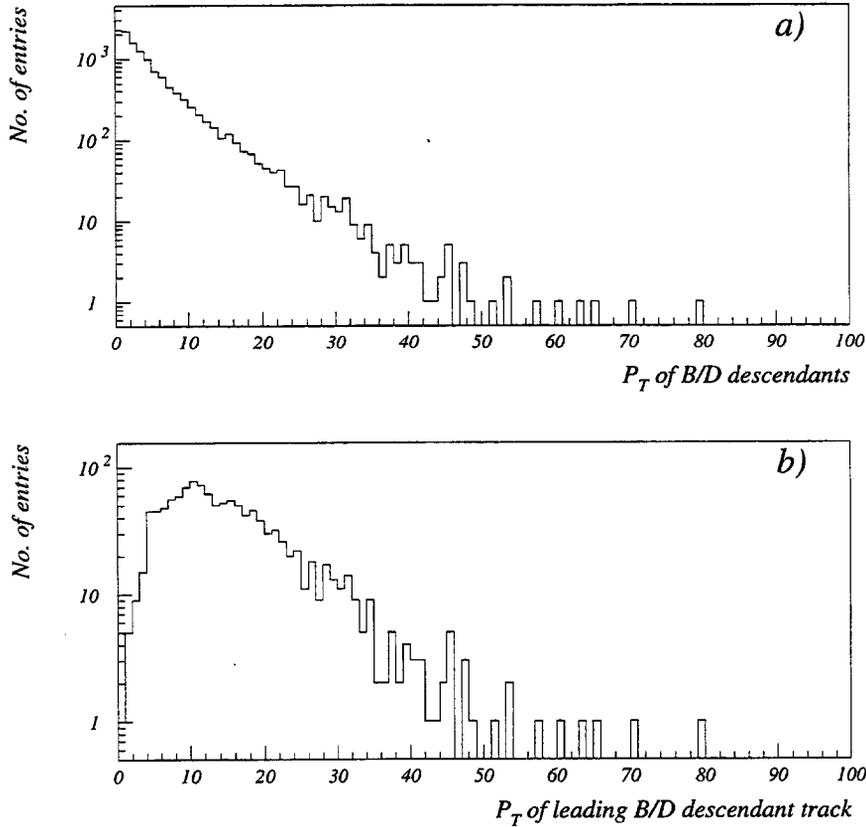


Figure 3:  $p_T$  spectrum of b- and c-quark decay products in a  $t\bar{t}$  event. The top plot is for all decay particles while the bottom plot is for the leading particle.

in the simplicity of the pattern recognition which has to be performed in a few 100 ns, which is what we expect will be available out of the total effective latency of about  $3 \mu\text{s}$ . The remainder of the time is spent initially in collecting the data from trigger sectors and arranging them logically and later on some more time has to be reserved for transmission delays to the trigger framework.

Since the mass scales of new physics are sufficiently high, this 11 GeV/c threshold on the track  $p_T$  does not result in intolerable inefficiencies. As an example of this, we consider the spectrum from the well known top decay. Figure 3a shows the  $p_T$  spectrum of the stable particles in the decay of the  $b$ -quark (or a subsequent  $c$ -quark) while Fig. 3b shows the spectrum for the *leading* particle. A large fraction (58%) of the spectrum is above 11

GeV/c, yielding a  $t\bar{t}$  efficiency of about 82%. The overall tracker acceptance has not been taken into account in this figure.

The available  $q$  in top decay is of the order of 100 GeV, and hence new particles that have mass greater than 100 GeV and decay into  $b$ -quarks will produce a similar spectrum as the one shown in figure 3. Further studies are required to establish the efficiency of this trigger for particular models and specific channels.

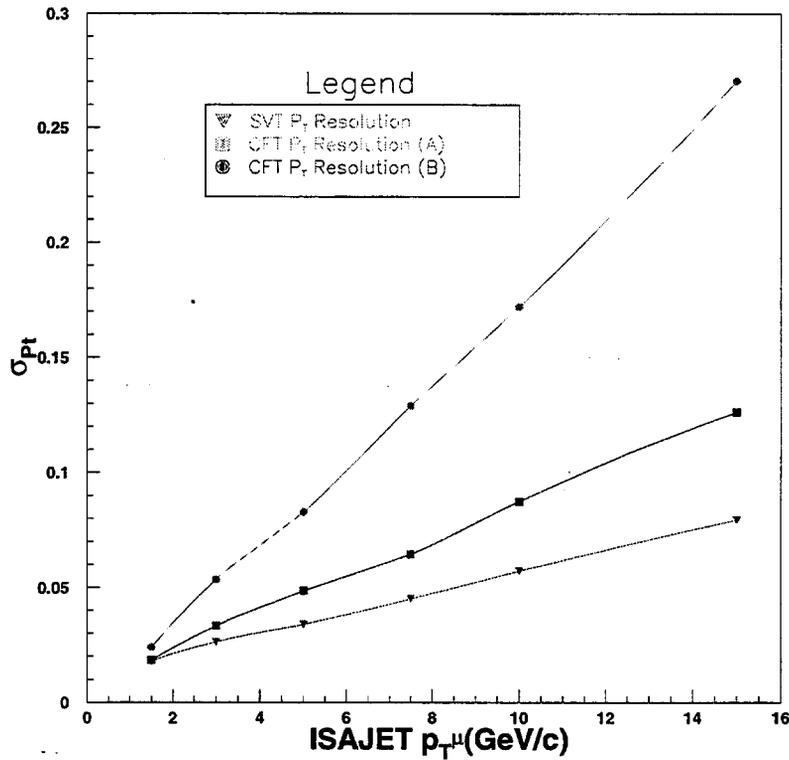


Figure 4: Momentum resolution as a function of  $p_T$  using the fiber tracker signals only (solid squares—best case scenario, solid circles—default case) compared to the resolution obtained by combining the fiber and Silicon tracker signals for DØ run II (solid inverted triangles).

### 3.1 Improvement in Momentum Resolution

The silicon tracker of run II provides significant improvement to the momentum resolution, over that obtained from the fiber tracker alone[6]. This is shown in figure 4. This study employed single muons generated at various values of  $p_T$  in the range 1–15 GeV using full GEANT simulation and digitization of the DØ run II detector. The momentum resolution obtained using only the signals from the fiber tracker are plotted using the solid squares and circles using two different implementations of the momentum determination at the trigger level. The curve with inverted triangles shows the resolution achieved by combining the signals from the silicon tracker at the L2 trigger stage. Compared to the best case scenario, for tracks above 5 GeV, the resolution improves by almost a factor of two after adding the hits from the silicon.

A 30–50% reduction in background rates is easily achieved by this improvement in momentum determination for high  $p_T$  tracks. These studies are directly applicable to the pixel tracker proposed for run III, and demonstrates that tracking points at radii of few cm are very effective in providing the longest possible lever arm within the tracker volume. We expect similar performance by including the pixel information along with the CFT signals at L1.

### 3.2 Displaced Track Trigger

In order to fully exploit the anticipated high luminosity during run III, it would be advantageous to enrich the data in their  $b$  quark content as early as the L1 stage. One of the primary goals of run III is to search for the Higgs or other new particles which could lead to insights into phenomena beyond the Standard Model, be it SUSY or an entirely new mechanism of electroweak symmetry breaking. Most of these models predict particles which strongly couple to  $b$ -quarks and hence lead to final states rich in  $b$ -quarks. In some cases, e.g.  $WH \rightarrow q\bar{q}b\bar{b}$ , triggering on events with  $b$  quark jets is the only way to reduce the trigger rate sufficiently to be able to operate an unprescaled trigger and acquire enough events to observe a signal.

Extensive feasibility studies of a displaced track trigger at the L2 trigger stage for run II have been carried out. For example, one study[6] which focusses on the advantages of such a trigger for new particle searches,  $B$ -meson physics, and measurements of the properties of the top quark, shows that a factor of 2–40 rejection of the background is easily achievable while retaining a signal efficiency of 90%–50%.

The impact parameter resolution curve is shown in figure 5. The plot is obtained from

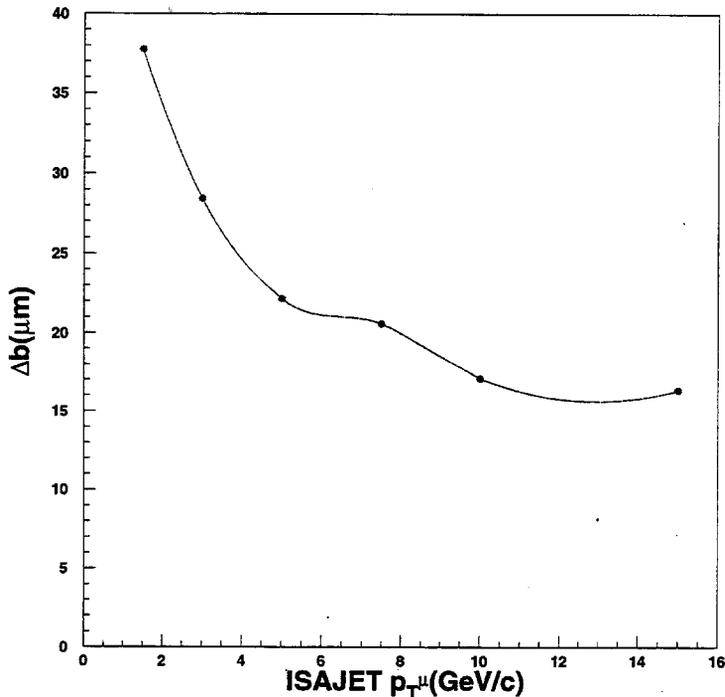


Figure 5: Impact parameter resolution as a function of track  $p_T$  for DØ run II tracker at Level 2 trigger stage. The asymptotic resolution is  $15\mu\text{m}$  for tracks with high  $p_T$ . This study includes the full GEANT simulation of the DØ run II tracker.

the same GEANT sample described in the previous section. For tracks above 10 GeV the impact parameter resolution is better than  $17\mu\text{m}$ , which is expected from the digital resolution of a  $50\mu\text{m}$  pitch. The resolution degrades to  $35\mu\text{m}$  for tracks with 2 GeV  $p_T$  due to multiple scattering. The proposed L1 pixel trigger in this note will give us the same resolution for a  $50\mu\text{m}$  pitch, while for a  $30\mu\text{m}$  pitch, the digital resolution will improve to about  $9\mu\text{m}$ . For the purpose of triggering, we have to also consider an error of about  $30\text{-}40\mu\text{m}$  in the primary vertex position due to the finite width of the beam. As can be inferred, this error will dominate the overall impact parameter resolution at L1.

Table 1, summarizes the rejections expected for 80% efficiency from the impact parameter trigger at L2(L1) for various physics channels for the run II(run III) environments [6].

Trigger	factor from impact parameter trigger
$t\bar{t} \rightarrow \ell + jets$ Use $\ell + jets$ triggers	1.5-2
$t\bar{t} \rightarrow alljets$ Use multijet triggers	1.5-2
$W + Higgs \rightarrow \geq 4jets$ Use 3 calorimeter jet triggers at L1*	10-20
(*Also applicable to any new particle decaying to heavy quark jets in the final state.)	

Table 1: Expected rejections for 80% efficiency from the proposed impact parameter trigger.

### 3.3 Secondary Vertex Determination

Triggering on the track  $p_T$  and impact parameter alone can give us enough rejection within the L1 bandwidth, provided the fake rate can be controlled. There is a component due to overlapping tracks (in the  $r-\phi$  view) within jets which needs to be evaluated for the pixel tracker. We expect this to be small due to the very low occupancy in this detector. However, we propose to further enhance the rejection factor by employing simple algorithms for secondary vertex finding.

Figure 6a shows the impact parameter distribution for all tracks from the  $b$ -quark jet in a top quark decay. Figure 6b shows this for the leading particle only. It is interesting to note that while there is a substantial population above 100 microns, the impact parameter of the leading particle is well contained within about 1 mm. Hence, this track will provide discrimination over other high  $p_T$  tracks coming from light quark jets, but with a loss in efficiency if we cut, say, at 150 microns. However, this track is a very good measure of the  $b$ -quark *direction* and we hope to use this fact in our simple algorithm.

Hence, instead of imposing an impact parameter cut on this track, we propose to use it as a “seed” for secondary vertex finding. Depending on the amount of information available, this can be done only in the  $r-\phi$  view, or in the  $r-z$  view as well. In the  $r-\phi$  view, the computation is more complicated because the other tracks in the decay will have some curvature and the FPGA equation count may be prohibitive.

In the  $r-z$  view, all the other tracks (straight lines) will intersect this track at some

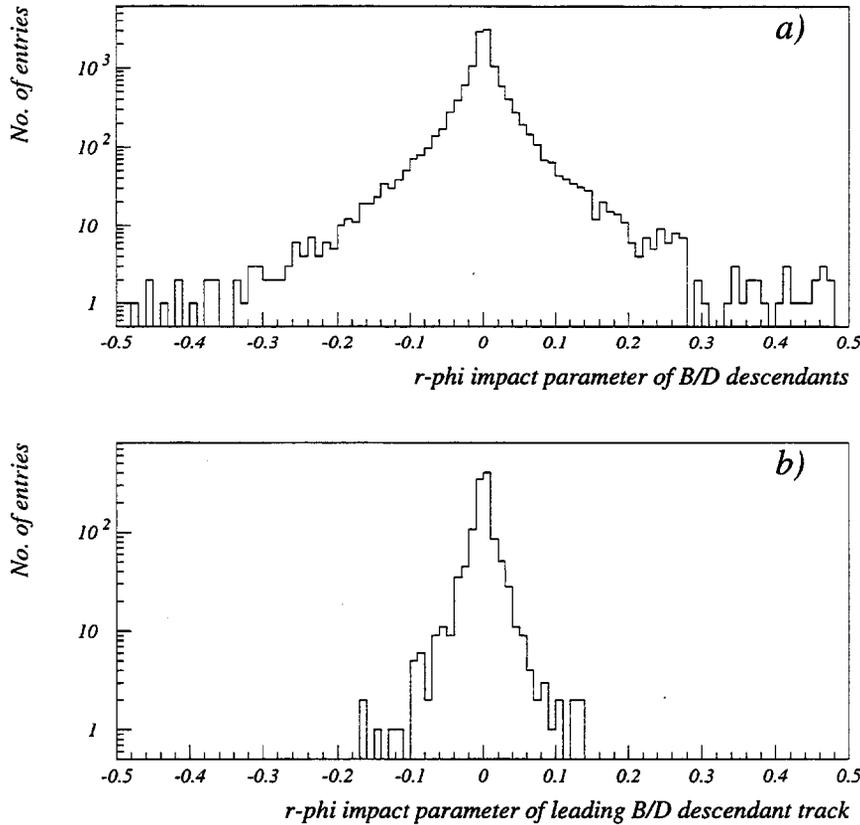


Figure 6: Impact parameter distribution of the decays products in a  $t\bar{t}$  event. The top plot is for all decay particles while the bottom plot is for the leading particle.

point. If we restrict ourselves only to tracks inside a local sector then the sample will be rich with decay products of the  $b$ -quark, if it indeed was the parent of the high  $p_T$  track. The centroid of the intersection points of all tracks with the seed track direction will be a measure of the vertex point, as shown schematically in figure 7. We expect that tracks in light quark jets will average out and the centroid will be formed near the interaction region while the heavy quark jets will produce a displaced centroid. Effects of multiple coulomb scattering will smear the measurement somewhat but we are encouraged by a similar study [7] done for the silicon strip detector which showed promising results.

Other backgrounds to an inclusive  $b$ -quark trigger, mainly from mismeasured light quark jets and from charm jets, have been evaluated in the STT studies and have been

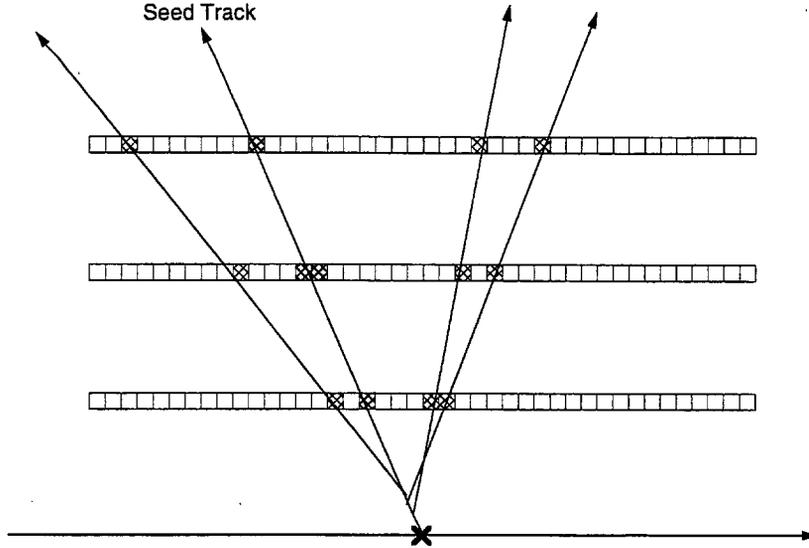


Figure 7: A schematic representation in the  $r$ - $z$  view of a trigger tower after having found the seed track in the  $r$ - $\phi$  view of the pixels. The high  $p_T$  seed track and several secondary tracks are shown to form a secondary vertex.

found to be controllable. The situation only improves at the higher threshold considered here.

Various triggering schemes and electronic designs based on FPGA's and DSP's are being developed and will be the subject of a subsequent note. As will be discussed later, the feasibility of this trigger will to some extent dictate the readout architecture and hence it has to be evaluated in detail. The bare minimum requirements for the necessary readout electronics is described in section 5. Next, we present simulations of the proposed geometry and the expected rates.

## 4 Tracker Geometry and Rate Simulations

The pixel tracker shown in figure 1 has to be constructed using "tiles" of pixel detectors that are limited in area to about  $1\text{cm}^2$  due to the yield limitations of most fabrication technologies. Figure 2 shows this construction using tiles measuring  $11\text{ mm} \times 9.8\text{ mm}$ . These dimensions are based on conservative estimates and will be described later. The figure 2 also shows a typical "logical" trigger tower. These towers are keyed to tiles in the middle layer and combined with 7 tiles each in the other two layers. This geometry provides full acceptance for all straight line tracks produced with an angle within  $\pm 45^\circ$

for all vertices inside  $\pm 22\text{cm}$  along the beamline. There is partial acceptance for vertices outside of this region.

There are two reasons for this tower geometry. First, it reduces the amount of data presented to one unit of trigger electronics and second, it greatly reduces fake backgrounds due to overlapping tracks. Once, the data have been contained within towers the trigger can operate in the  $r-\phi$  view only. Hence, at the minimum, the pixel detectors will be required to provide only two pieces of information at L1, a chip ID and the  $\phi$  coordinate of the hit. This information will be sufficient to construct logical towers in the trigger electronics and finding straight line tracks will be accomplished by forming simple coincidences.

The main goal of the simulations presented here is to answer questions related to data rate, dead-time, inefficiencies etc., parameters that will help in the design of the readout architecture. The plots shown have been generated using the present geometry of the silicon strip detectors planned for the run II upgrade. This geometry is similar enough to the pixel tracker that first order results can be readily obtained from existing simulation runs. Full GEANT has been employed and pile-up of variable number of interactions in a bunch crossing has been simulated.

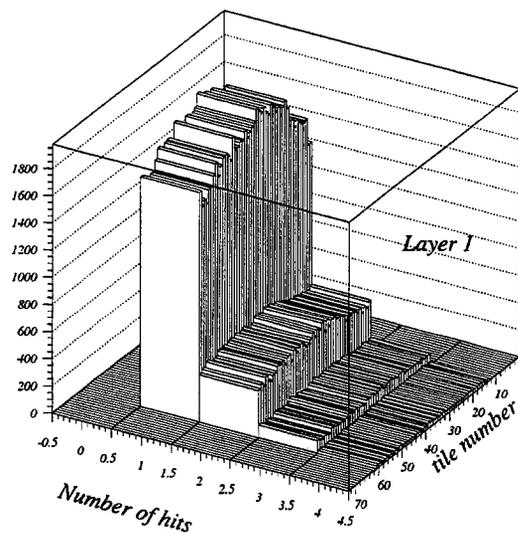


Figure 8: A lego plot of cluster occupancy per pixel tile for the inner most layer. The tiles are numbered from 13 to 60 representing  $z$  positions from  $-24\text{ cm}$  to  $+24\text{ cm}$ . Tiles with zero hits have been suppressed.

Due to the geometry of double sided silicon (50 micron  $\phi$  strips and 150 micron  $z$  strips) a pixel size of  $50 \times 150 \mu\text{m}^2$  is a natural choice. The estimates of hit rates will have only a weak dependence on this choice due to charge sharing among pixels. For example,  $30 \times 300 \mu\text{m}^2$  pixels, proposed in the next section, will have a slightly higher hit rate. In order to avoid this problem, we have used “clusters” to estimate the hit rate and then scaled it by a factor of 3 to obtain the pixel hit rate. As a reference, simulations for CMS have yielded a value of 2.7 for this scaling factor.

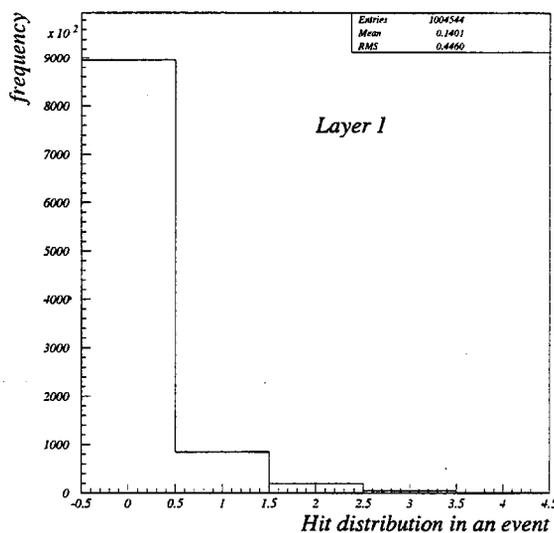


Figure 9: A histogram of cluster occupancy for the inner most layer. The mean occupancy for a tile is about 0.14 per crossing.

The silicon tracker ladders were divided into 12 sections, each 1 cm along the  $z$  direction, to make “tiles”. The width of these tiles is 2.2 cm, twice as wide as the proposed pixel tiles. Figure 8 shows the cluster occupancy for the innermost layer. The tiles have been binned along  $z$  into 72 bins representing 6 barrel wheels of 12 cm length each. The first layer does not have the first and the sixth wheels, hence only tile numbers 13 to 60 are plotted. Tiles with no hits in a given event have been suppressed. It can be seen that there is only a slight  $z$  dependence in the occupancy.

In figure 9, the occupancy is histogrammed after including the zero bins. From this plot we can read that the average occupancy for a tile in the inner layer is about 0.14 clusters. After using the factor of 3 scaling for charge sharing (and 1/2 for twice the area), this amounts to about 0.2 hits per crossing. For the third layer, the average turns out to

Radius	1 Int	3 Int	6 int
2.5 cm	0.15	0.3	0.6
7.5 cm	0.03	0.08	0.2

Table 2: Hit pixels per sq cm for inner and outer layers.

be about 0.15 hits per crossing.

Table 2 contains the data rate as a function of the number of interactions in a bunch crossing and the radial position of the detector. The rate has been averaged over  $\pm 25\text{cm}$  in  $z$ . The scaling factors mentioned above have been included.

As can be seen, for the average case of 6 interactions/crossing (for luminosity levelled TeV33), the number of hit cells is less than 1 at the innermost layer. This implies that if we limit the number of transmitted hits (at L0) from each readout chip to be no more than say, 4, the resulting loss will be negligible. Figure 10 is the same as figure 9, except that the zero bin has been suppressed. As can be seen the distribution has very little population above 4 hits.

Next, we estimate the probability for a pixel unit cell to be hit twice within the L1 latency, ie, 32 bunch crossings. For the worst case of large area unit cells (assuming  $50 \times 400 \mu\text{m}^2$ ) at the innermost radius, we get 0.6 hits being shared by 5,000 cells per crossing. This is a rate of  $1.2 \times 10^{-4}$  hits per cell per crossing. This implies that the probability for being hit twice within 32 crossings is about 0.4%. For the proposed size of  $30 \times 300 \mu\text{m}^2$  this probability drops to about 0.2%.

In summary, we conclude that the pixel detectors can be used as an L1 device provided that they can transmit the digital addresses of an average (maximum) of 0.6 (4.0) unit cells per crossing. Additional information such as the pulse height can be stored in the unit cell provided we are prepared to accept a corruption of 0.2% of the data due to multiple hits. These two numbers have a major influence on the readout architecture discussed in section 6. Next, we discuss more detailed parameters of the pixel detector.

## 5 Pixel Detector Design

The most important design parameter that makes DØ different from other efforts at LHC is the substantially longer bunch crossing interval. Other differences include 1) finer segmentation, 2) L0 trigger pick-off and 3) acceptable deadtime due to L1 readout.

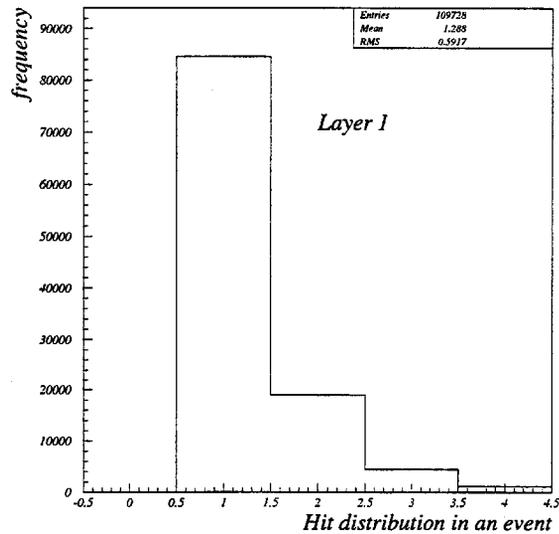


Figure 10: The cluster occupancy per tile for layer 1 where the zero bin has been suppressed. The tail above 4 hits is negligible.

We have arrived at a conceptual layout of the pixel readout chip as shown in figure 11. The chip consists of 32 columns and 256 rows. The row pitch is 30 microns and the column pitch is 300 microns. Four tiles constitute a ladder which is approximately 1.6 cm wide by 4 cm long and shares a common data bus. Below we clarify various design features that were kept in mind in order to arrive at this layout:

- A 30 micron pitch is desirable in order to match the fiber tracker momentum resolution at L1. If bump-bonding or other technical reasons render 50 microns (or higher) as the achievable pitch, we will have to correspondingly (square-root of ratios) increase the lever arm. This results in proportionately higher costs.
- Binary information from the pixels at L0 is desirable. This requires a so-called data push architecture (DPA) design [8]. An asynchronous DPA chip transfers all hits to the outside world much like a wire chamber would except here the data arrive sequentially and in digitized form. Usually, each hit results in the measurement of a 4-dimensional point and transmission of a data-packet consisting of a time-stamp, a column address and a row address. The asynchronous operation also implies that hits are not necessarily transmitted in a time-ordered sequence. Various readout designs exist (for SSC or LHC) that employ a DPA like scheme [9][8] but these were

designed for much higher bunch crossing frequencies. A chip designed for Fermilab should be able to operate *synchronously* as described below.

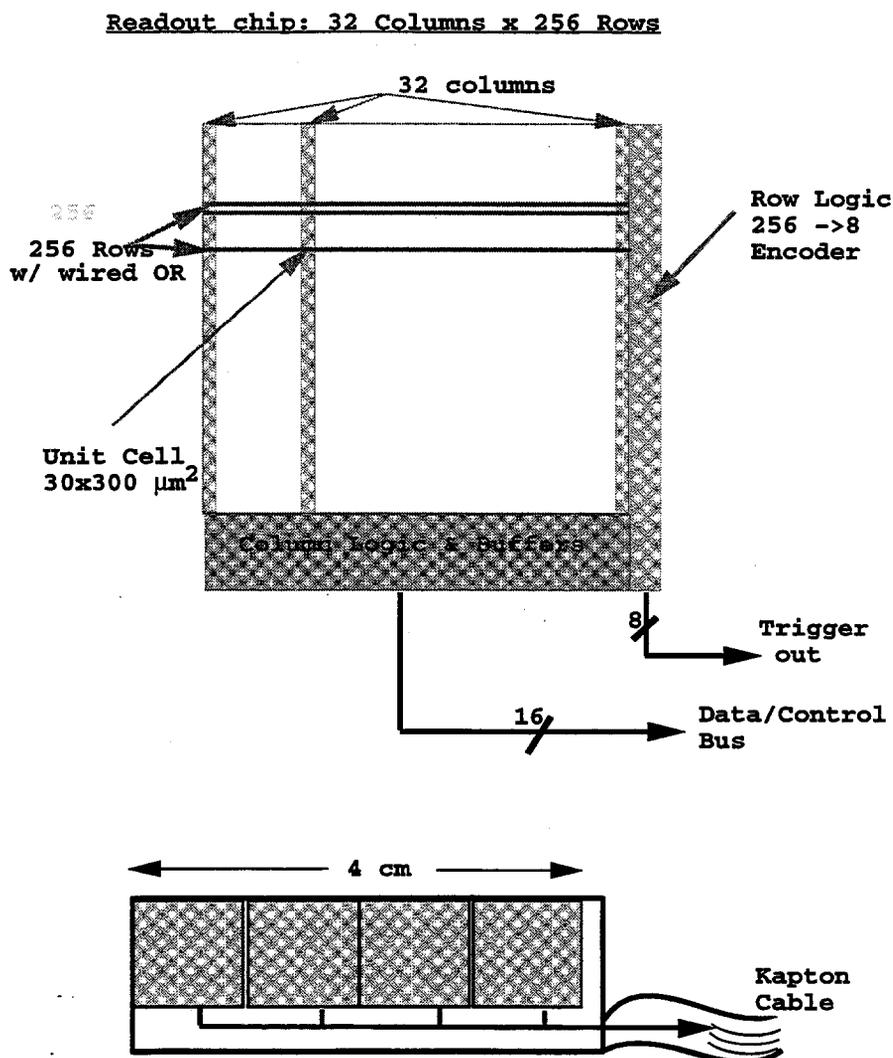


Figure 11: Conceptual design of a pixel readout chip. The architecture is column-based data-push. There is no Column OR signal but a Row OR is implemented for trigger purposes. A ladder using 4 tiles and a common data bus is also shown.

- For DØ a simplification to the DPA design would be to only transmit an OR of pixel row (ie, narrow dimension) addresses. This would reduce the L0 data rate by more than a factor of 2 primarily because of column address suppression and somewhat more because of occasional double hits in a row. The wired OR can in principle be

bridged over say, 4 chips, and be as long as 4 cm. This has led us to consider a 4 cm long ladder; the exact specification will be determined based on data transmission capabilities of the bus.

- Maintaining the fully synchronous nature of the L1 trigger in DØ is essential. For a DPA design, this will result in some loss of trigger data for unusually busy events wherein we will have to truncate the list of hits. An acceptable cutoff, determined from simulations, is at a maximum of 4 hits per crossing per readout chip. Once again, a row OR will suffer much less from these truncations.
- DØ data acquisition is not dead-timeless. Both the calorimeter and tracker incur deadtime of about  $5\mu s$  for every L1 trigger. For an L1 rate of  $< 10kHz$ , this results in no more than about 8% dead-time. Hence, unit cells in the pixel readout can be used for data storage during L1 latency, provided the readout at L1 can be performed in less than  $5\mu s$ . An example of the data stored in the unit cell would be its pulse height and a time-stamp (or equivalently, a pointer to a bunch crossing buffer memory location.)
- Due to limited access for services into the inner tracker, keeping the power load to a minimum is very important. A desired goal would be to keep the dissipation below  $0.25 \text{ watts}/\text{cm}^2$ . This level has been achieved by various groups designing readout chips.
- For reasons of minimizing mass, the number of cables (eg, kapton) also have to be minimized. Hence, a general rule of making all busses bi-directional (for downloading and for readout) is advisable. However, due to speed considerations, the L0 trigger path will probably have to be separate. Hence, we suggest that each readout unit compress (ie, sparsify and encode) its information into 8-bit words for transmission on a common *serial* bus during L1 readout. For now we consider a 16-bit wide bus to the end of the ladder where the conversion to a serial transmission can occur. The trigger bus, however, would be an 8-bit dedicated bus for each ladder.
- Use of fiber optics similar to that planned for the LHC would be very useful. As a rough estimate, the pixel tracker would require one kapton cable per  $1.6 \times 4 \text{ cm}$  ladder as compared to the run II silicon tracker which sends out one kapton cable per  $12 \text{ cm} \times 2.2 \text{ cm}$  ladder. Hence, the cable plant for this pixel tracker would be about a factor of 4 bigger for each barrel. Even though the number of barrels in pixels would be less, and some reduction in number of traces is possible, kapton is a cumbersome medium and fibers are preferable.

Keeping these points in mind, we have designed a readout architecture and generated preliminary specifications. This is described in the next section.

## 6 Readout Architecture

The following architecture is a blend of various designs already being developed. It is a column-based architecture adapted for the longer bunch crossing interval. The column periphery is greatly reduced because the data storage is implemented in the unit cells. The acquisition sequence is broken up into read and write cycles which do not occur simultaneously, and hence avoid interference. Furthermore, the digital and analog parts of the write cycle are also separated in time to reduce cross-talk. Below we describe the architecture. It is useful to remember that the rows are the narrow dimension and the columns are the wide dimension.

### 6.1 Write Cycle

The write cycle is the “live” mode for the detector and consists of the following functions:

Analog Cycle The analog block of the unit cell collects the input charge and fires a discriminator no later than  $T_0 + 38$  ns (two ticks of beam clock). This limitation on allowed time-walk, frees up 5 clock ticks for the digital cycle. Also, it is larger than the 25 ns requirement for LHC detectors and hence, it is hoped that there will be some saving in the power dissipation in the unit cell compared to those designs (time-walk, noise and power dissipation are all related specifications).

Digital Cycle 1 The presence of a discriminator “true” is recorded by the Row-periphery via a hard wired OR along the rows. The digital block of the unit cell latches a 6-bit gray-code number into a local register. This value which corresponds to a bunch crossing number between 0-31 is available to each cell over common bus lines. The number is updated at the start of the 3rd tick (38 ns) of the beam clock in order to avoid interference with the functioning of the analog block. The cell also stores its analog pulse height on a local capacitor.

The “hit” cell can now be dead for the next 32 crossings. The loss due to this is minimal as shown in our rate simulations. In the rare case that the cell has a latched value from some previous crossing, it is overwritten. Meanwhile, a digital comparator compares the latched value to the current crossing number, and resets the unit cell if the numbers match, indicating that 32 crossings have elapsed. Hence, a unit cell stays disabled

for 32 crossings after being hit and then resets itself.

In case an L1 trigger is received during these 32 crossings, all hit cells arm themselves for a "read" cycle. This is described later.

In summary, the digital part of the unit cell has three modes, "set", "reset" and "read". During "reset", it waits for the discriminator to fire and if so, enters the "set" mode. During "set" it checks every bunch crossing to either a) reset itself if 32 crossings have elapsed or b) look for an L1 trigger in which case it arms the token stop circuitry and enters the "read" mode. During "read" it waits for the arrival of the token to initiate readout. During both "set" and "read" the discriminator is disabled. These logical functions are performed by the unit cell between  $T_0+38$  ns and  $T_0+57$  ns (3rd tick).

Digital Cycle 2 This is the trigger cycle which is fully synchronous and occurs between  $T_0+38$  ns and  $T_0+132$  ns. During this cycle, the latched hits in the row-periphery are zero-suppressed, encoded into 8-bit addresses and transmitted off-chip. This sequence has to be especially fast so as to maximize the amount of data that can be transferred in 95 ns (10 ticks for a 106 MHz clock). Since there is no analog activity during this time, the circuitry can be made as noisy and power-hungry as necessary. The output can be on an 8-bit bus, but it is desirable to reduce the number of lines and hence multi-level encoding will be very useful. We have an ambitious goal of encoding and transferring upto 6 hits in 95 ns. Preliminary circuit designs have shown that it is quite feasible.

## 6.2 Read Cycle

The read cycle is the main acquisition mode during which the detector is "dead". It is initiated by the arrival of an L1 trigger. The bunch crossing clock is halted, the discriminators in the unit cells are disabled and a readout token is initiated. Each latched cell compares its value to the crossing number and stops the token if they match. After a token is stopped, the unit cell transmits its own row address and pulse height to the column periphery. The row-address is burnt-in in the silicon layout and the transfer is serial. The column-periphery mainly consists of multiplexing logic. For each row-address it attaches a column-address and sends the data packet off-chip.

The output for digital data is serial. The analog data are sent in parallel on another line. The sequence of data transmission is shown in table 3.

Since the digital data for each hit will take at least 130 ns (14 bits @ 106 MHz), the analog bus should have sufficient time to settle itself to a 5-bit value. This value is digitized off-chip, most likely in a flash ADC at the end of the ladder. Commercial rad-hard ADC's

Transfer No.	Clock Tick	Digital Bus	Analog Bus
1	1	CHIP ID	
2	2	Col Address 1	Pulse Height 1
-	9	Row Address 1	
3	16	Col Address 2	Pulse Height 2
-	23	Row Address 2	
.	.	.	
.	.	.	
n+1	14n+2	Col Address n	Pulse Height n
-	14n+9	Row Address n	
n+2	15n+2	END OF DATA	

Table 3: Data sequence from a pixel tile after an L1 trigger is received.

with a 100 ns digitization time are readily available.

At the end of a read cycle, all chips are fully reset and enter the write (or, “live”) mode. At this point the entire cycle is repeated.

The implementation of such a pixel readout will require the development of a suitable readout chip. A pixel readout chip called FPIX0 has been developed at Fermilab [11]. This chip is designed specifically for 132 ns operation and has a column-based architecture. Preliminary results from testing are very promising and the important specifications related to time-walk, noise and power dissipation have been met. A new chip called FPIX1 is being designed [12]. This chip has a readout architecture that is similar to the one described above in its functionality but the implementation is quite different. Furthermore, it sends both row and column addresses for each hit. As mentioned earlier, this gives us more flexibility in the trigger algorithm but comes at the cost of having to more than double our transmission bandwidth. Efforts are underway to design a chip compatible with the needs of the  $D\emptyset$  trigger.

## 7 Summary

We have shown that an inclusive b-jet sample above a moderate  $p_T$  threshold can be collected in the TeV33 running of  $D\emptyset$  if we employ a trigger based on pixel detectors. Preliminary simulations show that the rates will be manageable. Problems due to occupancy

and radiation damage are well controlled in such a tracker. A conceptual architecture for this readout and trigger has been defined.

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