# Detection of Cosmic Ray Tracks using Scintillating Fibers and Position Sensitive Multi-Anode Photomultipliers

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## 1.0 Introduction

This experiment demonstrates detection of Cosmic-Ray tracks by using scintillating fiber planes and multi-anode photomultipliers (MA-PMTs). In a laboratory like this, Cosmic-rays provide a natural source of high energy charged particle tracks. The experiment also demonstrates that high energy charged particle tracks in a high energy particle physics laboratory can be detected with a high efficiency and with nano-second time resolution.

The scintillating fibers and photomultipliers (PMTs) were used earlier in a Fermilab experiment, APEX, for searching for anti-proton decay. The amplifiers and the scintillating fiber plane couplings were improved for this laboratory experiment.

The majority of the Cosmic particles are muons which are mainly from the decay products of charged pions. The mean lifetime of the pions ($\pi^+$,$\pi^-$) at rest is around 26ns, and they decay into muons and neutrinos 99.987% of the time. Depending on the relativistic $\gamma$ factor, this lifetime can be much longer. The positively charged muons, $\mu^+$ decay into a positron and a neutrino, and the negatively charged muons, $\mu^-$, decay into an electron and an anti-neutrino. The muon lifetime at rest is around 2.2$\mu$s. Again this

time can be longer depending on the relativistic $\gamma$ factor. Decay schemes and the Cosmic-ray fluxes are illustrated in the figures of the appendices.

We expect the largest Cosmic particle flux to reach the Earth's surface from the Zenith (directly overhead). Tracks from this direction travel through a thinner layer of atmosphere, and so less are absorbed by atmospheric Nitrogen and Oxygen. When one does this experiment, one will see the display of the charged Cosmic-Ray particle tracks together with their angular distribution after some time. (Figure 1).

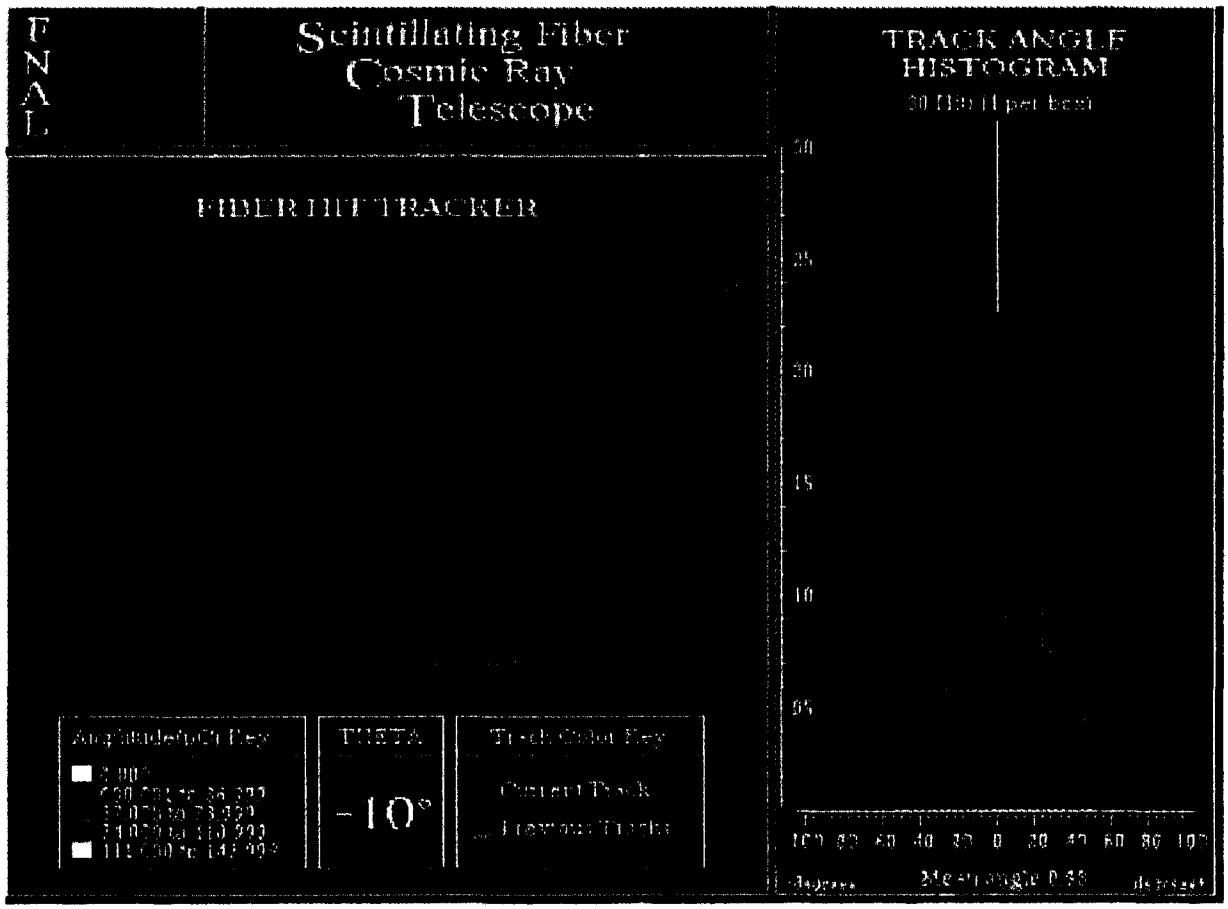



**FIGURE 1.** Screen Display from the Cosmic Ray Telescope

## 2.0 Description

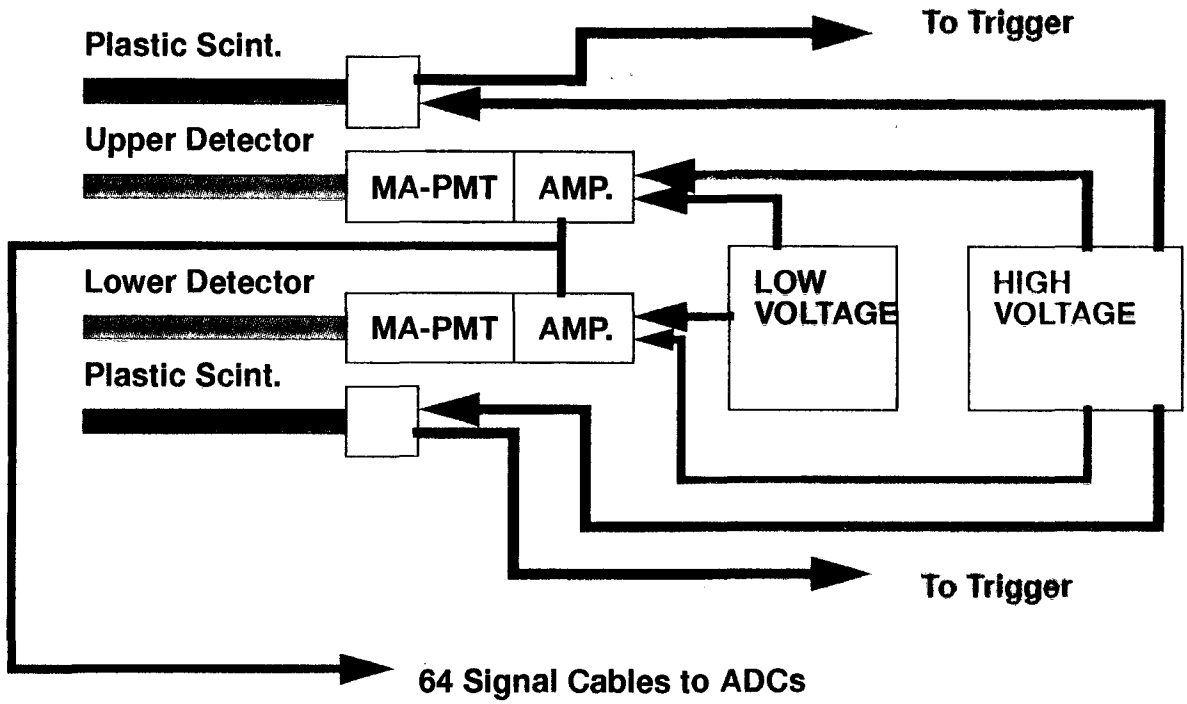



**FIGURE 2.** Block Diagram of apparatus

Figure 2 shows the experimental arrangement as a block diagram. The Cosmic particles are selected at the given solid angle by a pair of plastic scintillators arranged as a telescope. We use the discriminated signals from these scintillators to provide a trigger to the CAMAC read-out system. Outputs of the discriminators are put through a coincidence module to provide a gate to the LeCroy FERA Analog to Digital Converters (ADCs). The fibers inside each detector are arranged in 2 layers of staggered rows which are composed of 2mm, singly clad BICRON fibers (see Figure 3). There are 192 fibers in each detector. The fibers are butted onto the face of the MA-PMTs in an 8 by 24 grid. Each fiber is aligned with the matrix of 8 strips and 24 wire anodes inside the MA-PMT (Figure 4). The signals from the 32 anode

outputs from each MA-PMT are amplified before being digitized by the ADCs. This reduces the (8x24=) 192 fiber signals to (8+24=) 32 anode signals in each detector. A program running in the PC detects the gate generated by the scintillators, and reads the ADCs. It then decodes the 64 ADC values to reconstruct the hit pattern of the 384 fibers.

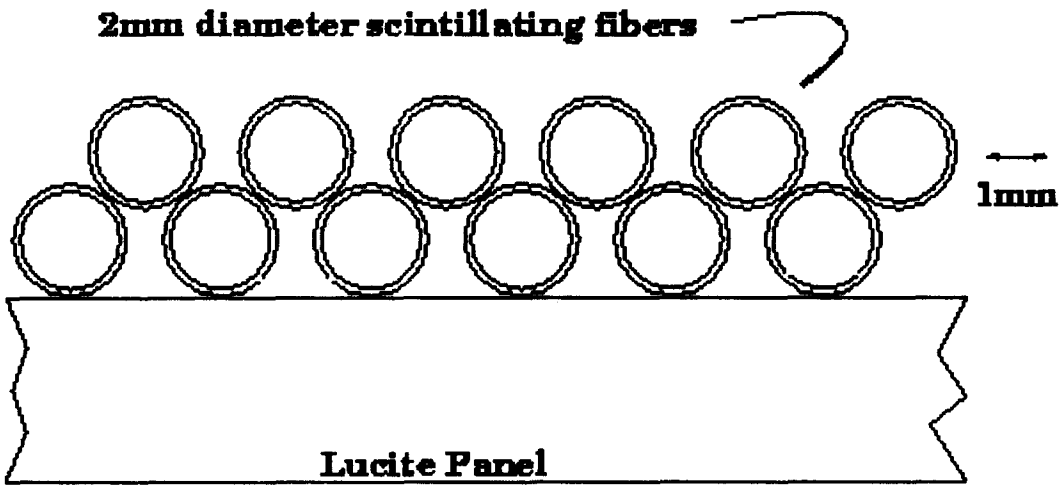



FIGURE 3. Arrangement of fibers in detector.

When studying the display one should note that often more than one fiber is lit. Sometime this is due to Cosmic-Ray showers where a particle has interacted with the ceiling of the building and produced many secondaries. The most common cause if the multiple hits in a single fiber plane is due to cross talk in the MA-PMT. Each wires and strip receives as much as 20% from the charge of its two neighbors. Cross talk between adjacent wires will appear as hits on neighboring fibers on the event display. Cross talk between adjacent strips will appear as hits on every $8^{th}$ fiber.

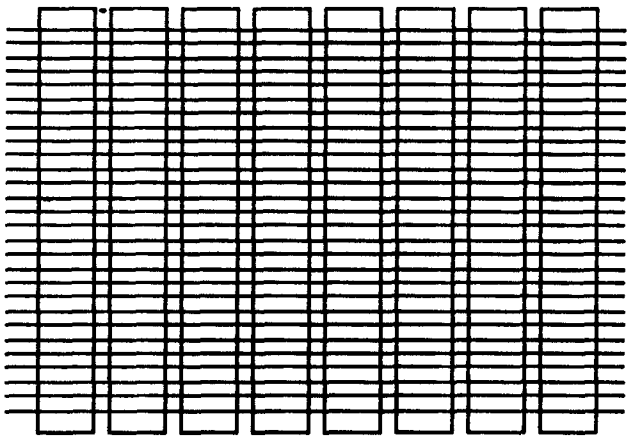


FIGURE 4. Arrangement of 24 wires and 8 strips in MA-PMT

## 3.0 Materials and Equipment

- Butyl PBD and POPOP scintillating fiber planes. Core of the fibers base material is polystyrene, and the clad material is poly-methyl-metacrylate (PMMA, trade name is *Lucite*)
- 64 Channels of LeCroy 4300 CAMAC-FERA ADCs
- Two Hamamatsu R4135 multi-wire anode PMTs
- Two RCA 8575 PMTs
- High Voltage power supplies and distributions boxes (COWS)
- Low voltage bias power supplies for the amplifiers at on the R4135 signals.
- Portable CAMAC crate, with two CAMAC to NIM converters for trigger logic.
- LeCroy 4222 gate generator for pedestals
- LeCroy 622 Coincidence unit and LeCroy 621L discriminator unit for trigger logic
- 100MHz Pentium PC with DSP602 ISA-CAMAC crate interface

# 4.0 Operating Instructions for the SFCRT

## 4.1 Starting Data Taking

1. Turn on the Computer
2. When the computer requests a password, hit CANCEL
3. Turn on CAMAC crate and power supplies.
4. Attach lemo cable from 4222 OUT1 to the GAI input of the 4301. (For pedestal gate)
5. On the Windows 95 screen, there is an icon for the SFCRT. Double click it. The introductory screen will execute, an immediately after, 100 pedestals taken, and average downloaded to the 4300s.
6. When the screen changes to the data taking view (Figure 1), disconnect the lemo cable from the 4301 GAI input, and connect the lemo cable from the 622 OUT to the 4301 GAI input. The system can now trigger on the plastic scintillator coincidence.
7. Hit Enter to start data taking

## 4.2 Getting a Screen Dump of the Display

Press ALT-PRINT SCREEN. This will save the screen in the computer's paste buffer as a bitmap image. You can then start the PAINT utility that comes with Windows 95, select "paste" option under the edit window, and the image will appear on the screen. At this point you can save the image to a file, or to a printer.

## 4.3 Switch Settings

1. DSP controller - On Line / Off line switch is set to On Line
2. Lambda Low Voltage power supplies for the Amplifiers - both set to 7V.
3. 622 QUAD coincidence module - AND/OR switch set to AND

**CAUTION HV supplies must be powered up and down in correct sequence and at correct values. Please do not attempt to change HV setting unless authorized.**

4. Fiber detector HV power supply - set to NEG 1300 Volts
5. Fiber detector HV zener divider (COW) - Channel 1 peg inserted in the 500 NEG HV hole (one detector runs at 1300V, the other at 900V)
6. Plastic trigger scintillator power supply - set to NEG 1700 Volts. Both run at -1700V.
7. Use channels 2 and 3 of the plastic scintillator COW (channel 1 is stuck at 100).

## 4.4 Cabling Hook-up for the SFCRT

#### *4.4.1 Lemo Connections*

1. DSP CAMAC controller REQUEST to GRANT IN
2. TOP PMT gate to 1$^{st}$ section IN of 621L
3. BOTTOM PMT gate to 2$^{nd}$ section IN of 621L
4. Output (lower left) of 1$^{st}$ section of 621L to IN of 1$^{st}$ section of 622
5. Output (lower left) of 2$^{nd}$ section of 621L to the other IN of 1$^{st}$ section of 622
6. OUT of 1$^{st}$ section of 622 to IN of 3$^{rd}$ section of 621L
7. During Data Taking: OUT of 3$^{rd}$ section of 621L to GAI input of 4301
8. During pedestal Calculation (on start-up): OUT1 of 422 to GAI input of 4301

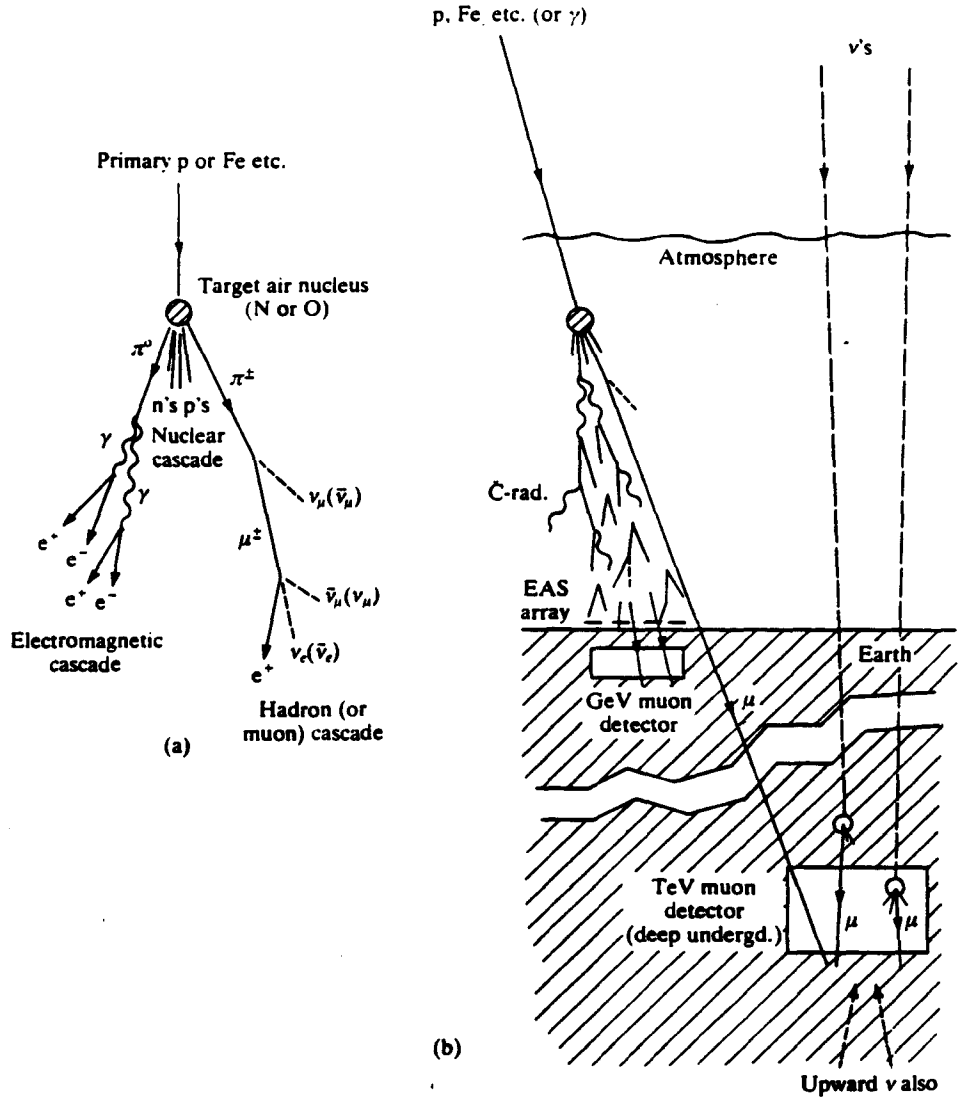
#### *4.4.2 Twist-n-flat cables*

1. Cable 1 tube 4 bottom 34-pin connector to 4300 (slot 20) 34-pin connector IN. Pin 1 marking on header up.
2. Cable 2 tube 4 top 34-pin connector to 4300 (slot 21) 34-pin connector IN. Pin 1 marking on header up.
3. Cable 3 tube 4 bottom 34-pin connector to 4300 (slot 22) 34-pin connector IN. Pin 1 marking on header up.
4. Cable 4 tube 4 top 34-pin connector to 4300 (slot 23) 34-pin connector IN. Pin 1 marking on header up.

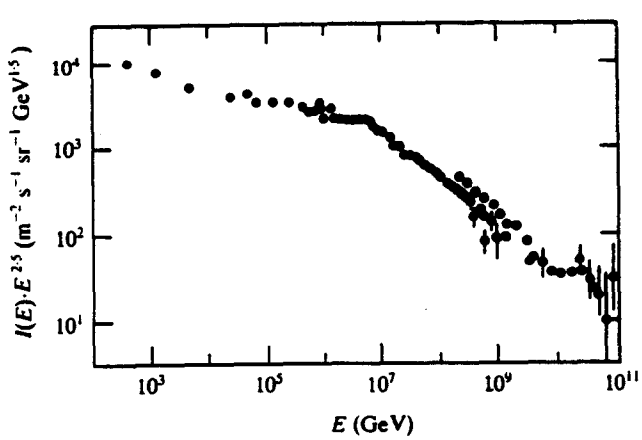
#### *4.4.3 High Voltage cables (RED CABLES)*

**CAUTION HV supplies must be powered up and down in correct sequence and at correct values. Please do not attempt to change HV setting unless authorized.**

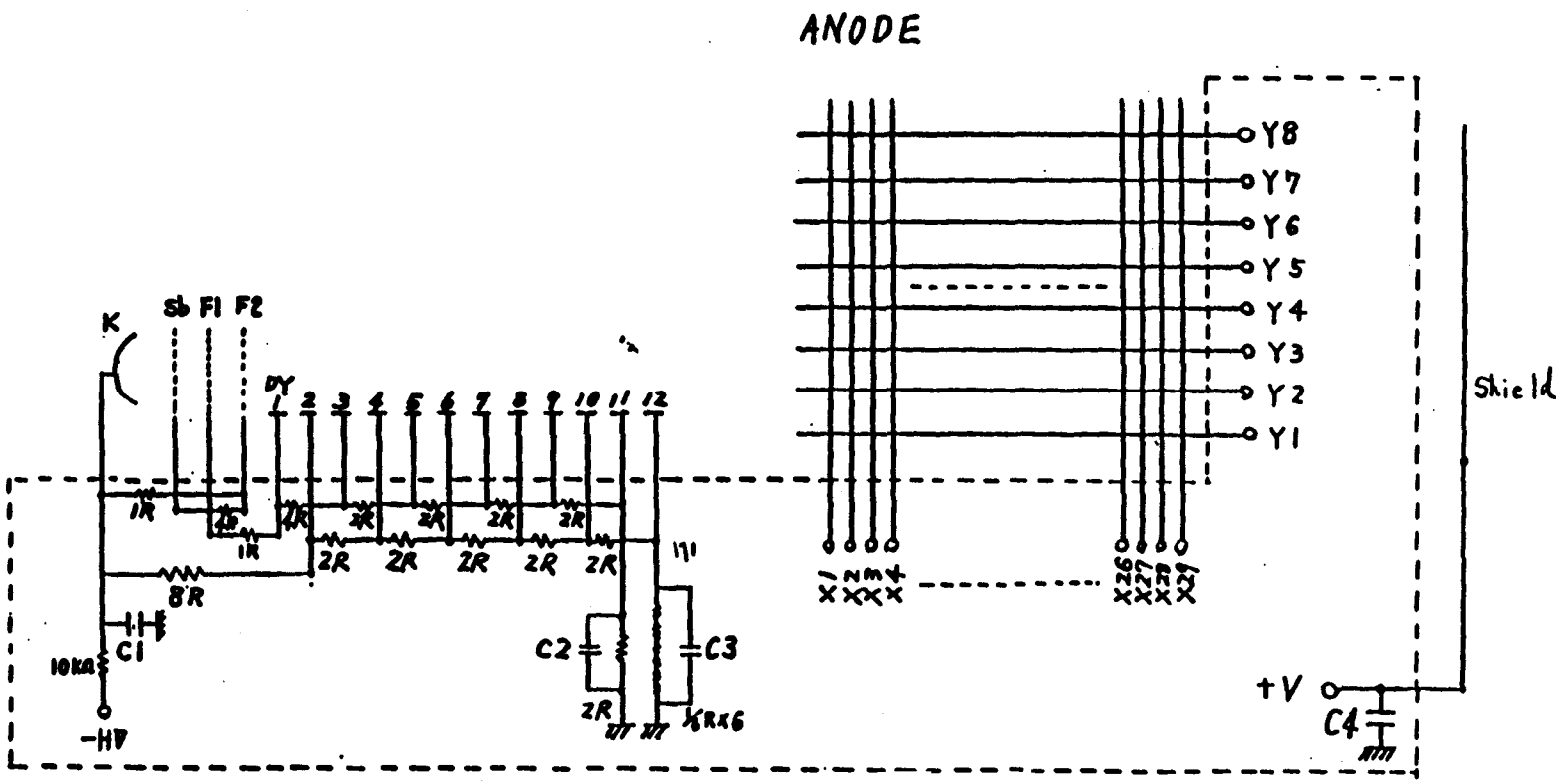
1. From Tube 4 detector to PG1 input of MA-PMT COW (-900V).
2. From tube 9 detector to PG2 input of MA-PMT COW (-1300).
3. From HV output of model 1570 HV supply to -HV input of COW
4. From top gate paddle to regulating HV fan-out panel input (3rd from top)
5. From bottom gate paddle to regulating HV fan-out front panel input (2nd from top)
6. From rear connector of 415B to NEGATIVE input of regulating HV fan-out.




(a) The development of an air shower caused by a primary proton or heavy nucleus hitting an air nucleus, and producing a nuclear cascade of neutrons and protons, as well as pions which subsequently decay and produce electromagnetic cascades (via $\pi^0 \rightarrow \gamma\gamma$) or so-called "hadron" cascades through $\pi^\pm \rightarrow \mu^\pm \nu$. (b) A summary of the techniques used to observe cosmic ray particles.




The all-particle differential cosmic ray spectrum $I(E)$, multiplied by $E^{2.5}$.




1R : 180KΩ
C1 : 0.002μF/2kV
C2~C4 : 0.01μF/500V

$\frac{1500V}{11R}$ = .431mA
ΔV = iR = 79V

| ITEM | NOTE | DATE |
|---|---|---|
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|---|---|
| NAME | R4135 (ZS0405) VOLTAGE DIVIDER (CIRCUIT) |
| DRAWING NUMBER | |
| DATE - | '90.1.10. |

CHECKED BY:
DRAWN BY: S. Muramatsu
SCALE 1/1

**HAMAMATSU PHOTONICS K.K.**

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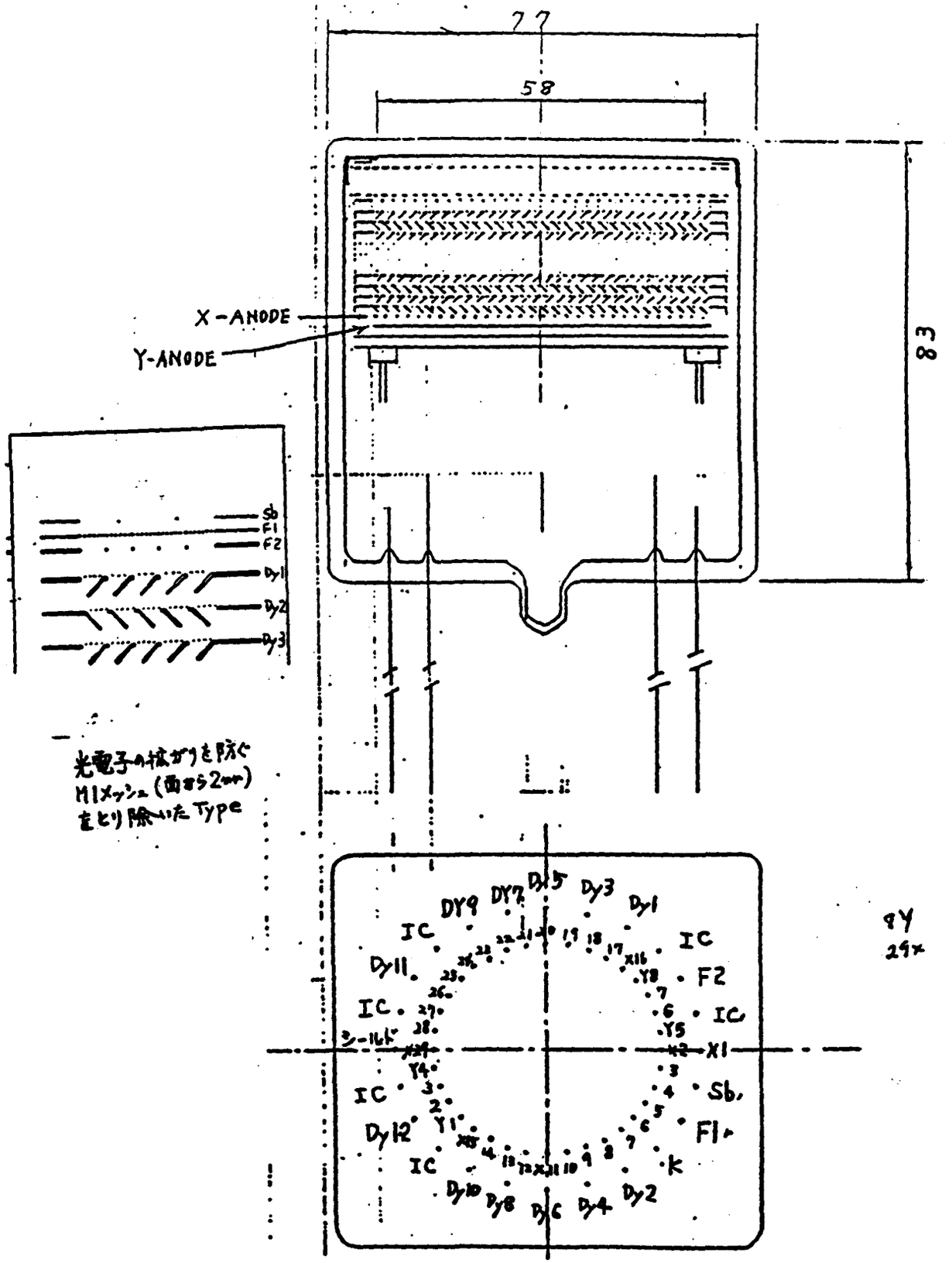



R 4135

Serial No. ZS0405

# 4300B 16 INPUT FAST ENCODING AND READOUT CHARGE ADC
# 4301 FAST ENCODING AND READOUT DRIVER MODULE
# 4302 DUAL PORT MEMORY
# 4303 FERET 16 INPUT TIME-TO-CHARGE CONVERTER

- **Charge and Time Interval Measurements In One System**
- **Dynamic Ranges 10 and 11 Bits**
- **Conversion Time: 4.8 μsec at 10 Bits, 8.5 μsec at 11 Bits**
- **Readout Via CAMAC Dataway or Via Auxiliary Bus at 100 nsec/word**
- **High Density, 16 Channels Per Module**



## FOR FAST AND PRECISE CHARGE AND TIME INTERVAL MEASUREMENTS

The Fast Encoding and Readout ADC (FERA) and Fast Encoding and Readout TDC (FERET) systems consist of modules designed for fast conversion of analog information, either charge or time intervals, into a digital format. They also provide fast readout to a storage memory module or to a computer for further processing. The system modularity allows small as well as large multi-channel ADCs or time digitizing (TDC) systems to be configured and also allows simple memory expansion. These units can be used with other modules to configure energy or time based triggers tailored for specific applications.

The heart of the system is the Model 4300B, a charge sensitive analog-to-digital converter. Other elements in the system include the Model 4301, a utility module for distribution of common signals and regeneration of signals for multiple 4300Bs; the Model 4302, a dual port fast access memory module; and the Model 4303, which converts time intervals into charge signals to be measured by the Model 4300B.

# FEATURES

**Constant Short Conversion Time** - The time for conversion is 4.8 µsec at 10 bits and 8.5 µsec at 11 bits. This is independent of the number of channels or modules making up a system.

**Fast Data Readout** - A readout speed of 10 megawords/sec, associated with pedestal subtraction and zero suppression capabilities, allows a uniquely fast data acquisition rate both for charge and time interval measurements.

**High Resolution** - The least count resolution in charge is 0.25 pC. It is adjustable in time from 50 psec to 500 psec.

**Expandable Memory** - Data can be stored in cascadable, 16 kiloword deep memory modules.

**System Flexibility** - Due to its modular nature, a system can be easily expanded and adapted to measure charge or time intervals or both, and can also be easily interfaced to CAMAC, FASTBUS or GPIB.

**Trigger Capability** - The FERA/FERET systems have been designed so that the digitized charge or time information can be given as an input to second level trigger processors built around the ECLine Data Handler Modules.

# FUNCTIONAL DESCRIPTION



A Fast Encoding and Readout ADC (FERA) system includes the Model 4300B and may also include the Model 4301 FERA Driver and/or the Model 4302 Dual Port Memory.

A Fast Encoding and Readout TDC (FERET) system always includes the Model 4300B and the Model 4303 Time-to-Charge Converter. With the 4303 both common start and common stop operations are possible. It may also include the 4301 FERA Driver and/or the 4302 Dual Port Memory.

The 4301 FERA Driver is a utility module which distributes signals common to the system, such as gate, fast clear, test and handshake signals, via the command bus. It also receives data from the fast data bus, which collects data from all Model 4300Bs in the system, and translates it for transmission to the memory module or to the ECLine logic units.

The Model 4302, a 16 kiloword x 16-bit Dual Port Fast Memory unit, provides data storage by accepting data on the fast access front-panel port. Data can be successively read via the CAMAC dataway. Up to ten 4302 modules can be cascaded to increase the total memory capacity.

Two standard versions of the 4300B are provided. Model 4300B/600 converts charge into 10 bits in 4.8 µsec and the Model 4300B/610 converts charge into 11 bits in 8.5 µsec.

After conversion, the digitized data may be automatically corrected with values contained in the programmable internal pedestal memory.

Digitized data is available first on the front-panel ECL port and subsequently on the CAMAC dataway. The ECL port readout is optional. All zero or zero-and-overflow data words may be suppressed to provide data compression. The compression procedure takes 2.5 µsec irrespective of the number of channels or modules in a system.

The front-panel bus system includes the protocol necessary to allow high-speed sequential readout to the LeCroy series of ECLine Data Handler Modules and to the Model 4302, Dual Port Fast Memory. Cables for these buses can be ordered from LeCroy as Model 4300 DC-N. The same bus system can provide interfacing and data storage in FASTBUS, where data can be received by the Model 1892 FASTBUS Memory, or in VME. (See LeCroy Application Notes AN-4001, AN-4004A, AN-39 and Publication P-2 for examples.)

# SPECIFICATIONS

## Model 4300B ADC

**Analog Inputs:** 16.
**Connector:** 17 x 2-pin front-panel connector (BERG 75789-101-34). The upper 16 pins of the left row are negative signal inputs. The upper 16 pins of the right row are connected to the common virtual ground (AC-coupled to ground). The lower two pins are connected to ground.
**Input Sensing:** Charge (current integrating).
**Impedance:** 50 Ω ±3% within the range 0 to -60 mA DC. Outside these limits, diode protection clamping will affect input impedance.
**Protection:** ±25 V for 1 µsec transients; (clamping diodes to ground and -3 V).
**Limitations:** Maximum current for linear response: -30 mA. The linearity is degraded to typically ±(1% of reading + 0.25 pC) for -60 mA.

### ANALOG-TO-DIGITAL

**Resolution:** Two factory options: 10 or 11 bits.
**Conversion time:** Typically 10 bits in 4.8 µsec, 11 bits in 9.5 µsec.
**Typical Range:** 10 bits, 256 pC minus ADC pedestal; 11 bits, 480 pC minus ADC pedestal.
**Sensitivity:** 0.25 pC ±3%.
**Integral Linearity:** Typically ±0.5 pC, at worst ±(0.25% of reading + 0.5 pC) for signals of slew rate < 2 mA/nsec. For signals of slew rate 4 mA/nsec, the linearity is degraded to typically ±(1% of reading + 0.25 pC).
**Differential Linearity:** Typically ±10%, worst case ±20%.
**Residual Pedestal:** From 1 pC to 13 pC for gate width from 50 to 500 nsec, all inputs open. Adjustable with an internal potentiometer for gate width > 500 nsec. Subtracted from data by CAMAC command.
**Pedestal/Gate Width Coefficient:** Better than ±8 pC/µsec, typically ±3 pC/µsec.
**Operating Temperature:** 0° to 40°C.
**Temperature Coefficient:** Typically (-0.05% of reading ±0.1 count)/°C for a gate width of 500 nsec. The coefficient may vary slightly for other gate widths.
**Long Term Stability:** ±(0.25% of reading + 0.5 pC)/week at constant temperature and voltage.

## Models 4303 (and 4300B) TDC

### SIGNAL INPUTS

**Common Start (STRT)/Common Stop (STOP)/Test:** Three front-panel 2-pin connectors. 100 Ω input impedance, accept complementary ECL pulses of 5 nsec minimum width.
**Individual Inputs:** 16 inputs in a front-panel 17 x 2-pin connector (BERG 75789-101-34), 100 Ω input impedance, accept complementary ECL pulses of 5 nsec minimum width.
**Input Sensing:** Time, common start or common stop.

### ANALOG-TO-DIGITAL

**Typical Range:** 100 nsec to 1 µsec.
**Sensitivity:** 50 psec to 500 psec adjustable through a front-panel potentiometer.
*Note:* Other TDC specifications are identical to the ADC specifications when applicable.

## Model 4301 FERA Driver

### INPUT/OUTPUT

**Gate (GAI & GATE):** Two inputs. Inputs are OR'd and available on the Command ECL Bus (GATE) for distribution.
**Clear (CLI & CLR):** Two inputs. Inputs are OR'd and available on the Command ECL Bus (CLR) for distribution.
**Write Acknowledge (WAI & WAK):** Two inputs. Inputs are OR'd and available on the Command ECL Bus (WAK) for distribution to the Model 4300B FERAs. The WAK may also echo the WST signal after a fixed time delay.
**Write Strobe (WST & WSO):** Input via Command Bus (WST) from the Model 4300B FERAs. Two outputs. For synchronous operation, the WSO signal may be connected directly to the WAI via a fixed delay cable or an active delay.
**Inhibit Readout (IRI):** Two inputs. Inputs are OR'd and act as a veto for the REO signal described below. Since the REO is usually connected to the first Model 4300B FERA to be read out, the IRI inhibits the readout and may be used to block the readout process until the receiver module is ready.
**Readout Request (REQ, RQO & REO):** Input via Command ECL Bus (REQ) from the Model 4300B FERAs. Following a fixed delay, three outputs are generated. (The delay is set to 200 nsec in the factory. It may be adjusted via the internal potentiometer RQ DEL). The two outputs (RQO) may be used to signal a request to read out data. The third output (REO) can be vetoed by the IRI signal and is normally connected to the REN or Readout Enable input of the first Model 4300B FERA to be read out; one 2-pin connector generates differential ECL signals into 100 Ω.
**ECL Data Bus (IN & OUT):** 16 inputs via 17 x 2-pin connector (IN). Accepts single ended ECL signals from the ECL Ports of the Model 4300B FERAs. Generates differential ECL outputs on the 17 x 2-pin connector (OUT) for all 16 signals.

**Note:** Paired signals are made up of one Lemo-type connector accepting NIM signals (50 Ω input impedance), and one 2-pin connector accepting differential ECL signals (100 Ω input impedance).

## Model 4302 Dual Port Fast Memory

### INPUT

**Data Inputs:** Front-panel 34-pin connector which accepts complementary ECL signals, 100 Ω input impedance; up to 16 parallel bits can be accepted and stored in the memory word addressed at the strobe pulse arrival time; the memory address is automatically incremented by one at the end of the strobe pulse.
**Strobe Veto (VETO):** Front-panel 2-pin connector accepts complementary ECL pulses, 100 Ω input impedance; an input signal acts as a veto on the Write Strobe Input (WSI). Connecting the FULL output to the VETO input in adjacent Model 4302s permits simple cascading of memory units. WSI and Data Inputs must also be connected.
**Write Strobe (WSI):** *NIM:* two bridged Lemo-type connectors with high input impedance accept NIM level pulses; the unused input must be terminated. *ECL:* front-panel 2-pin connector accepts complementary ECL pulses; 100 Ω input impedance. The leading edge of the strobe pulse must fall inside the data pulse and must arrive at least 10 nsec after the data are valid; minimum width 20 nsec; maximum frequency 10 MHz for both NIM and ECL.
**Clear Address Counter (CLR):** NIM: Lemo-type connector, input impedance 50 Ω, minimum pulse width 20 nsec, accepts NIM level pulses; an input pulse resets the memory address and clears the LAM.

### OUTPUT

**Overflow (OVF):** *NIM:* Lemo-type connector; generates NIM level pulses when terminated in 50 Ω. *ECL:* front-panel 2-pin connector generates complementary ECL levels. When the ECL port is enabled, a signal is generated as long as the memory address is equal to or exceeds the value that has been preset by switches on the side of the module; the output is active until the memory address is changed by CAMAC. The two side panel switches permit the selection of 12288, 14336, 15360, or 15872 as the overflow address.
**Acknowledge (ACK):** Front-panel 2-pin connector generating a complementary ECL signal; the echo of WSI with 35 nsec delay time; it is inhibited if the address counter has reached the full memory capacity.
**Memory Full (FULL):** Front-panel 2-pin connector generating a complementary ECL signal; active as long as the address counter has not reached the full memory capacity.

## General Specifications

**Power Requirements:**

| | +6 V | -6 V | +24 V | -24 V |
|---|---|---|---|---|
| 4300B | 2.1 A | 2.74 A* | 0.1 A | — |
| 4301 | 0.1 A | 1.2 A | 20 mA | 30 mA |
| 4302 | 2.2 A | 0.2 A | — | — |
| 4303 | — | 1.5 A | — | 0.2 A |

* When all output pull-down and input matching resistors are removed, the current at -6 V is reduced to 2.4 A.

**Packaging:** RF-shielded, CAMAC #1 modules conforming with the IEEE Standard 583.

## FERA BUS SIGNALS

### COMMAND BUS

**Connector:** 8 x 2-pin front-panel connector. The input matching resistors and output pull-down resistors may be removed for high impedance inputs and outputs. When these resistors are in place, a front-panel LED (PD ON) is lit.
**Input Levels:** Differential ECL levels, 100 Ω impedance differential.
**Output Levels:** Differential ECL levels (into 100 Ω differential).
**Gate Input (GATE):** One; common for all ADCs. Non-retriggerable. Gate width 50 to 500 nsec (> 500 nsec is possible after pedestal adjustment). Gate must precede input signals by at least 20 nsec.
**Clear Input (CLR):** One; common for all ADC front ends and associated digital logic. May be executed at any time. Minimum clear width: 5 nsec. CLEAR settles to within 1 count in less than 2 µsec during conversion. The action is immediate after conversion.
**Request Output (REQ):** One; An ECL port readout request indicates that this module is ready to take control of the ECL port data transfer. After conversion, the REQ is set only if the ECL port readout is programmed and the module contains valid data.
**Write Strobe Output (WST):** One; indicates when the data are valid on the ECL port output. WST is set within 10 nsec after the data are presented to the ECL port (setting time) and released when the write acknowledge is received. The ECL port data are stable during the entire WST pulse. The minimum write strobe width is 40 nsec.
**Write Acknowledge Input (WAK):** One; acknowledges the signal from the ECL port receiver indicating that the data have been loaded and that the next data word may be sent. The next WST is set 50 nsec after the release of WAK. The minimum write acknowledge width is 30 nsec.
**Test Reference Voltage Input (TRV):** Two paralleled front-panel 2-pin connectors, high input impedance (200 kΩ), accept the Test Reference Voltage; the second connector can be used for monitoring or daisy chaining. The gate and charge pulses are generated at the input of all ADCs by the CAMAC function F(25)•A(0). The test charge pulse is proportional to the DC level at the TRV input. Channel-to-channel matching of the proportionality constant is ±1%. TRV input range: 0 to +10.24 V, equivalent to 512 pC ±0.1% on each ADC. The common virtual ground offset is automatically compensated.

### ECL PORT ENABLE/PASS

**Readout Enable Input (REN):** 1 x 2-pin front-panel connector. Accepts differential ECL levels. Input impedance 100 Ω differential. REN indicates to the receiver that it can take control of the ECL Port Bus. The REN signal must be maintained during the entire readout time. REN enables the ECL port outputs, the WST output and the WAK input if the module is ready for data transfer (REQ output ON).
**Pass Output (PASS):** 1 x 2-pin front-panel connector, generates differential ECL levels (into 100 Ω differential). Indicates that the sender has finished using the ECL port or is not ready. The PASS output is activated by the REN input signal and closed by the REQ output internal command. The transit time between the REN input and the PASS output is typically 3 nsec if the module is empty.

### ECL PORT OUTPUT

**Connector:** 17 x 2-pin front-panel connector; (BERG 75789-101-34). The last 2 pins are not connected.
**Output Levels:** Differential ECL levels (into 100 Ω differential). The pull-down resistors may be removed for high impedance outputs. When these resistors are in place, a front-panel LED (PD ON) is lit.
**Specifications:** Data word size: 16 bits. Sequential data readout with maximum output frequency 10 MHz (see Readout Block Format).

### TEST REFERENCE VOLTAGE SPECIFICATIONS

The TRV output on the Command Bus is driven by an internal CAMAC controlled Digital-to-Analog Converter (DAC). The DAC uses a control register which may be set and read via CAMAC commands. WARNING: The register content is randomly set at power on.
**Range:** 0 to 10.2375 V corresponding to inputs for the Model 4300B FERA of 0 to 511.875 pC.
**LSB:** 2.5 mV corresponding to inputs for the Model 4300B FERA of 0.125 pC.
**Integral Linearity:** ±0.5 LSB.
**Full Scale Error:** ±1 LSB.
**Settling Time:** 5 µsec.
**Current Limit:** 3 mA.

## FERA STATUS WORD REGISTER FORMAT

**R1 to R8:** VSN; Virtual Station Number: index source for sequential readout with zero suppression.

**R9:** EPS; ECL port Pedestal Subtraction: when EPS = 1, pedestals are subtracted for ECL port readout.

**R10:** ECE; ECL port data Compression Enable: when ECE = 1, data zeros or zeros-and-overflows are suppressed for ECL port readout.

**R11:** EEN; ECL port ENable: when EEN = 1, ECL port readout is permitted.

**R12:** CPS; CAMAC Pedestal Subtraction: when CPS = 1, pedestals are subtracted for CAMAC readout.

**R13:** CCE; CAMAC data Compression Enable: when CCE = 1, data zeros or zeros-and-overflows are suppressed for CAMAC sequential readout.

**R14:** CSR; CAMAC Sequential Readout: when CSR = 0, CAMAC random access readout is enabled; when CSR = 1, CAMAC sequential readout is enabled.

**R15:** CLE; CAMAC LAM Enable: when CLE = 1, LAM is enabled.

**R16:** OFS; OverFlow Suppression: when OFS = 1, data overflows are suppressed during ECL port readout in conjunction with ECE = 1 and for CAMAC sequential readout in conjunction with CCE = 1.

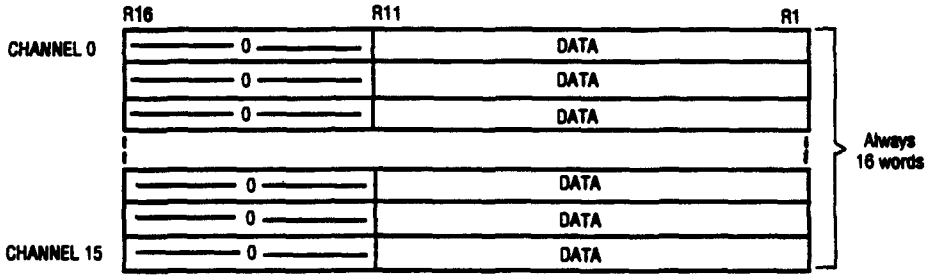
**Note:** The 8 bits, EPS to OFS, are set to 1 by the CAMAC Z function.

CAMAC

## Model 4300B Readout Block Format

Without Zero or Zero-and-Overflow Suppression:

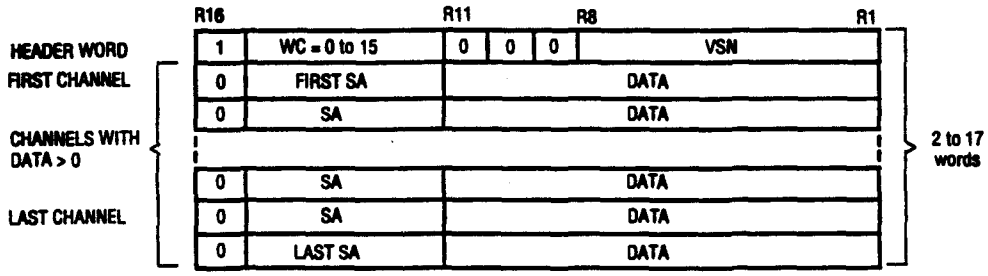
ECL port readout: EEN=1, ECE=0, OFS=X
CAMAC readout: CSR=1, CCE=0, OFS=X




DATA: 10-bit resolution: 0 to 1023; overflow=2047
11-bit resolution: 0 to 1919; overflow=2047.

With Zero or Zero-and-Overflow Suppression:

ECL port readout: EEN=1, ECE=1, OFS=0 or 1
CAMAC readout: CSR=1, CCE=1, OFS=0 or 1




VSN: Virtual Station Number Loaded in the Status Register.
WC: Number of data words following the header word, 0 indicates 16 data words.
DATA: 10-bit resolution: 0 to 1023; overflow=2047 (only with OFS=0);
11-bit resolution: 0 to 1919; overflow=2047 (only with OFS=0);
SA: Channel Subaddress

## Model 4300B

### CAMAC COMMANDS

**Z:** Initialize module; clear module and set status register's eight command bits to 1.

**C:** Clear the module.

**I:** Inhibit the front-panel gate when present.

**X:** Generated for all valid functions.

**Q:** Generated if a function can be executed.

**L:** LAM is set, if enabled, after the end of conversion (or ECL port readout) if there are valid data to be read.

### CAMAC FUNCTION CODES

**F(0)•A(0):** Read status word register. Q = 1 if BUSY = 0.

**F(1)•A(0-15):** Read pedestal memory (8 bits) for the 16 channels. Q = 1 if BUSY = 0.

**F(2)•A(0-15):** Random access or sequential readout of the 16 ADC values. Q = 1 if BUSY = 1.

**F(8)•A(0):** Test LAM. Q = 1 if LAM is present.

**F(9)•A(0):** Clear module.

**F(10)•A(0):** Test and clear LAM.

**F(16)•A(0):** Write status word register. Q = 1 if BUSY = 0.

**F(17)•A(0-15):** Write pedestal memory (8 bits) for the 16 channels. Q = 1 if BUSY = 0.

**F(25)•A(0):** Enable test. Q = 1 if BUSY = 0.

CAMAC

## Model 4301

### CAMAC COMMANDS

**X:** Generated for all valid functions.

**Q:** Generated if a function can be executed.

### CAMAC FUNCTION CODES

**F(0)•A(0):** Read DAC control register content (12 bits).

**F(9)•A(0):** Generates a clear signal on the COMMAND ECL bus.

**F(16)•A(0):** Write DAC control register content (12 bits).

## Model 4302

### CAMAC COMMANDS

**Z:** Reset memory address to zero and clear the LAM.

**X:** Generated for all valid functions.

**Q:** Generated if a function can be executed.

**L:** LAM is generated on overflow (OVF).

### CAMAC FUNCTION CODES

**F(0)•A(0):** Reads 16-bit data at the current memory address, and increments the address by one at S2. No Q response is generated when the address pointer exceeds the memory capacity.

**F(1)•A(0):** Read memory address (16 bits). The presence of the two most significant bits indicates an address overflow.

**F(1)•A(1):** Read the port enable register (2 bits).

| R2 | R3 | |
|---|---|---|
| 0 | 0 | All ports disabled. |
| 0 | 1 | CAMAC enabled. |
| 1 | 0 | Reserved. |
| 1 | 1 | ECL front panel enabled. |

**F(2)•A(0):** Reads 16-bit data at the current memory address. Decrements the address by one at S2. No Q response generated after word at address zero has been read.

**F(8)•A(0):** Test LAM. Q = 1 if LAM is present.

**F(10)•A(0):** Test and clear LAM.

**F(16)•A(0):** Write 16-bit data at the current address. Increments the address by one at S2. No Q response is generated when the address pointer exceeds the memory capacity.

**F(17)•A(0):** Write memory address (14 bits).

**F(17)•A(1):** Write the port enable register (see F(1)•A(1) table).

**F(24)•A(0):** Disables LAM.

**F(26)•A(0):** Enables LAM. LAM is generated on overflow.