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Readout System in the Fermilab KTeV Experiment**

Juliana Whitmore

*Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510*

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The performance of a high speed pipelined photomultiplier readout system in the Fermilab KTeV experiment

Juliana Whitmore

Fermi National Accelerator Laboratory, Batavia, IL USA

The KTeV fixed target experiment at Fermilab is using an innovative scheme for reading out its 3100 channel CsI electromagnetic calorimeter. This pipelined readout system digitizes photomultiplier tube (PMT) signals over a 16-bit dynamic range with 8-bits of resolution at 53 MHz. The crucial element of the system is a custom Bi-CMOS integrated circuit which, in conjunction with an 8-bit Flash ADC, integrates and digitizes the PMT signal charge over each 18.9 nsec clock cycle (53 MHz) in a deadtimeless fashion. The digitizer circuit is local to the PMT base, and has an in-situ charge integration noise figure of 3 fC/sample. In this article, the readout system will be described and its performance including noise, cross-talk, linearity, stability, and reliability will be discussed.

1 Introduction

KTeV is a fixed-target experiment at Fermilab which is currently collecting data to reach two main physics goals. The first is to search for direct CP violation in 2π decays of neutral kaons by measuring the $\text{Re}(\epsilon'/\epsilon)$ via the double ratio

$$R = \frac{\Gamma(K_L^0 \rightarrow \pi^+ \pi^-) / \Gamma(K_S^0 \rightarrow \pi^+ \pi^-)}{\Gamma(K_L^0 \rightarrow \pi^0 \pi^0) / \Gamma(K_S^0 \rightarrow \pi^0 \pi^0)} \quad (1)$$
$$\approx 1 + 6\text{Re}(\epsilon'/\epsilon)$$

with a precision of 1×10^{-4} . The second is to search for and study rare K_L^0 decay modes, especially CP violating decays such as $K_L^0 \rightarrow \pi^0 \ell \ell$, with a single event sensitivity of 10^{-11} for the charged lepton modes and 10^{-8} for the neutrino mode.

To achieve these goals, the electromagnetic calorimeter must have an energy resolution of 1% for 15 GeV photons. The calorimeter electronics is required to have better than 1% resolution and a non-linearity that is understood at the 0.1% level over 16-bits of dynamic range. The noise contribution from the electronics must be less than 5 fC. The readout system is designed to operate at 53 MHz (the Tevatron RF frequency), in order to reject out-of-time activity in the calorimeter. The front-end continuously integrates energy from the calorimeter in deadtimeless fashion, buffering the information until Level-1 (800 nsec) and Level-2 ($2.5\mu\text{sec}$) trigger decisions. A previous report¹ discussed the performance of an early prototype version of the calorimeter readout. This article concentrates on the performance of the electronic readout system in the KTeV environment and the

production, integration, and reliability issues that have been encountered while assembling the system for the KTeV experiment.

2 Calorimeter Readout System

Pure CsI was chosen because of its radiation hardness, high light output and fast response time. Light from the CsI is measured with either a 5 or 6 stage Hamamatsu photomultiplier tube (R5364, R5330) which is optically coupled to each of the 3100 crystals. The signal from the PMT is then digitized by a “Digital Photomultiplier Tube” (DPMT) board. The primary features of the DPMT are a high-voltage divider for the PMT, a charge integrating and encoding (QIE) custom integrated circuit, an 8-bit Harris FADC (HI1386), and a driver/buffer/clocking (DBC) custom integrated circuit. The system operates at 53 MHz, corresponding to an 18.9 nsec clock cycle.

The operations of the digitizing circuit are shown in Figure 1. The crucial component of the circuit is the QIE.^{2,3} The QIE divides the current from the PMT (0-30 mA) into 8 binary-weighted ranges ($1/2, 1/4, \dots, 1/256$). The divided currents are then added to bias currents and integrated simultaneously onto eight parallel 1 pF capacitors. An appropriate sensitivity range is chosen based on the total integrated charge for each clock cycle, and the voltage from that capacitor is multiplexed to the FADC. The QIE operation is pipelined, requiring 4 capacitors per sensitivity range for continuous integration of the PMT signal. The QIE chip is fully differential, having identical signal and reference circuits and differential output for ex-

ponent and capacitor identification information. The differential design reduces the temperature dependence of the electronic gains and the coherent noise input from the PMT. The QIE output is an analog voltage, 3-bits of exponent information, and 2-bits for capacitor identification. The QIE and FADC produce an 11-bit floating-point output plus 2-bit capacitor tag data every clock cycle, spanning 16-bits of dynamic range with 8 to 9 bits of precision. The output response of the FADC for a single clock cycle is shown in Figure 2.

The DBC performs several functions. It receives a 53 MHz clock and generates copies for the FADC and the QIE with up to a 7 nsec programmable phase delay in 1.0 nsec steps. It terminates and synchronizes digital data from the QIE and the FADC, storing the data in two FIFOs, a 40-slice deep Level-1 FIFO and a 32-slice deep Level-2 FIFO, until receipt of Level-1 and Level-2 triggers. The data is then sent through a parallel to serial converter and transmitted at 26 MHz (RF/2) onto 4 differential lines to a VME-based buffer.

3 Production Issues

The QIE and DBC ASICs were produced with the Orbit Semiconductor 2.0μ Bi-CMOS process. The wafer real estate was shared between the QIE and DBC chips. Multiple processing runs were required to generate the KTeV production order. Rather than choosing a chip-on-board scheme, KTeV decided to package the DBC and QIE into 64-pin thin-quad-flat-pack devices, thus facilitating replacement of bad chips. No degradation of chip performance was seen from packaging the devices. Packaged devices were individually tested⁴ before mounting on the DPMT board and fully-stuffed DPMT boards were tested before installation into the calorimeter. Average chip yields were 61% and DPMT board yields were 75%. Gain variations for the QIE of 2% were measured within a process batch, whereas variations of up to 20% were seen between process batches. The DBC phase trim for the QIE/FADC clocks varied by ± 2 nsec and the DBC maximum operating frequency varied between 45-70 MHz between process batches of the DBC.

4 System Performance and Reliability

The KTeV detector has been collecting data since summer 1996. The noise performance of the calorimeter electronics is demonstrated in Figure 3 by the online plot of the pedestal RMS from the sum of four clock cycles, corresponding to 4 capacitors in the QIE, for all 3100 channels in the KTeV calorimeter. The typical pedestal RMS for a single capacitor is 0.36 counts (~ 3.6 fC). Crosstalk between adjacent channels is less than 0.1%. Calibration of the electronics is performed *in-situ* using a YAG laser/dye system with similar spectral and time properties as CsI scintillation pulses. Light is distributed to each of the PMTs through individual quartz fibers. The laser light is monitored by four PIN-diodes, the signals of which are digitized by Burr-Brown 20-bit ADCs (DDC101). For calibration runs, the light intensity is varied using neutral density filter wheels over the entire dynamic range of the DPMTs. Because the DPMT response is linear within each of its 8 ranges, it can be characterized by 2 constants (a slope and an offset) per range per capacitor, for a total of 64 constants per channel. Figure 4 shows the fractional residuals for a typical channel which are less than 0.2% over the full dynamic range. One measure of the stability of the electronics is the frequency of updating constants required to maintain better than 1.5% ($\sigma(E/P)$) resolution for online event reconstruction. The electronic constants for the spring 1997 data taking were updated once during the 2 month running period. A single constant relates DPMT charge response to energy which is derived by comparing the electron response in the calorimeter with the momentum information derived from the magnetic spectrometer. In offline analysis, we have achieved a calorimeter resolution ($\sigma(E/P)$) of 0.78% for electrons from $K_L^0 \rightarrow \pi^\pm e^\mp \bar{\nu}$ decays.

Although the calorimeter electronics' performance has been quite impressive, the reliability of its ASICs in field operation has been marginal. KTeV has successfully dealt with many of the problems it has encountered because of the relative ease in accessing the electronics to replace failed channels. During the course of commissioning and initial operation of the calorimeter, several pathological problems developed with the ASICs. The first chip problems were termination resistor failures on the DBC. These failures were likely caused

by large voids that were discovered in the Metal-1 traces of failed parts. The presence of these voids effectively reduce the current carrying capacity of the Metal-1 traces to significantly less than 1 mA/ μm . These Metal-1 failures in the DBC circuit lead to unacceptably high failure rates in the field. This failure mode was addressed by modifying the DBC layout to decrease the Metal-1 maximum current to less than 0.25 mA/ μm . With this new layout, the failure of these circuits in the DBC has been virtually eliminated.

The QIE performance also varied significantly with Orbit fabrication batch. During the commissioning phase of the calorimeter readout, it was discovered that parts from one particular QIE fabrication batch would occasionally (0.1%) generate erroneous exponent codes when operated at 53 MHz. Due to the performance limitation of this particular fabrication batch, the fall 1996 data set was collected at 18 MHz (RF/3). During this commissioning phase, QIE failures linked to Metal-1 voids began to occur at 3 channels/day after ~ 1 million channel hours of operation. After this commissioning run, the slow QIE batch was replaced and the DPMT boards were modified so that the QIE part would remain functional against the previously mentioned Metal-1 failure. After these modifications, the readout system operated successfully at the 53 MHz design speed through the duration of the 1997 data taking. Because the QIEs were not refabricated with larger Metal-1 traces, chip failures continue to occur at a rate of 1 per 60K channel hours. It is expected that layout modifications to the QIE will increase the reliability to that of the modified DBC part.

5 Conclusions

The KTeV experiment has been collecting good physics data since October 1996. The calorimeter has excellent energy resolution, due in part to the performance of the DPMT. Although the two ASICs on the DPMT have been plagued with problems, the failures primarily have been linked to processing problems rather than design flaws. KTeV has been the proving ground for the QIE readout technology. Because of KTeV's success, modified versions of the KTeV QIE chip are being developed for the CDF calorimeter and the CMS hadron calorimeter.

6 Acknowledgements

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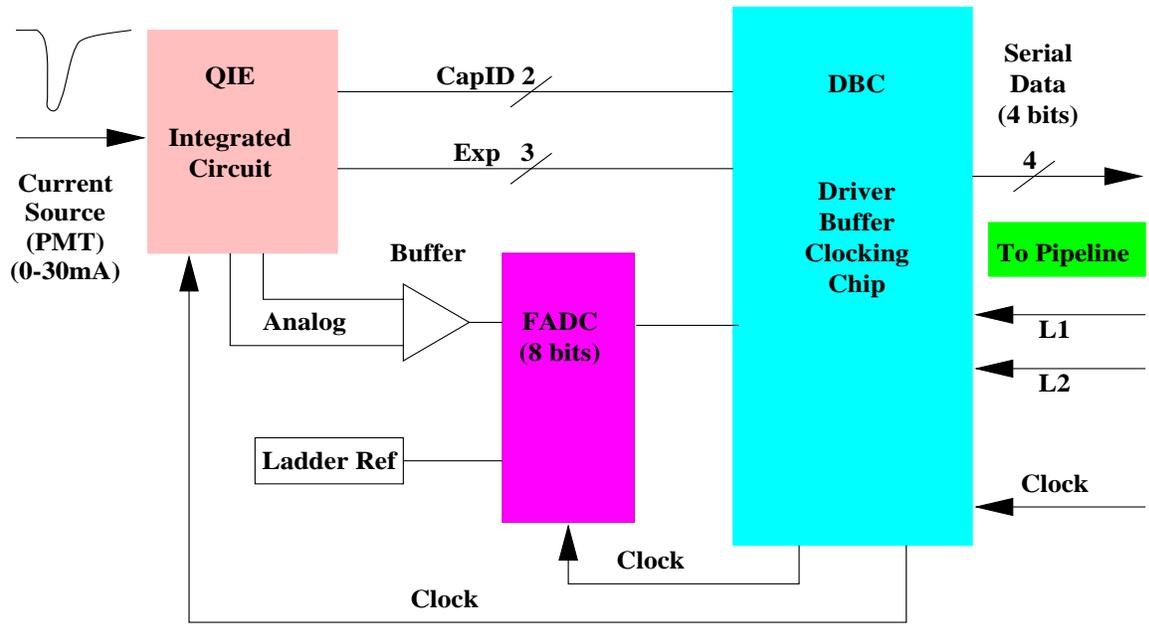


Figure 1: Block diagram of the operations for the DPMT.

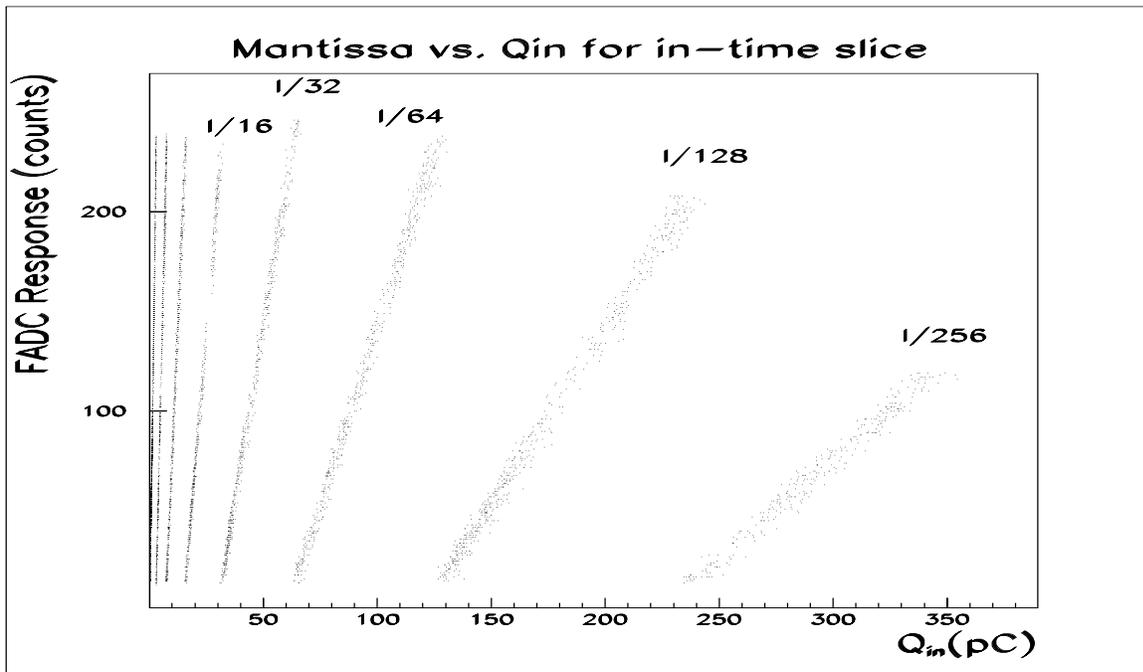


Figure 2: FADC response for the first in-time integration period versus increasing input charge.

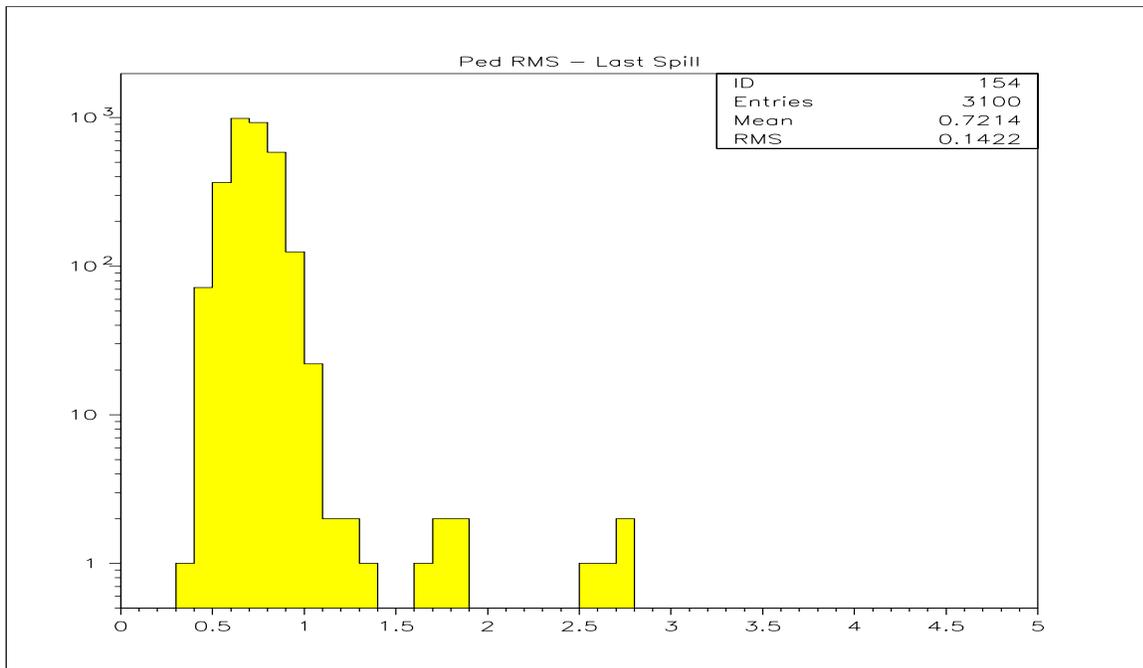


Figure 3: Pedestal RMS from the sum of 4 clock cycles for all 3100 channels of the KTeV calorimeter.

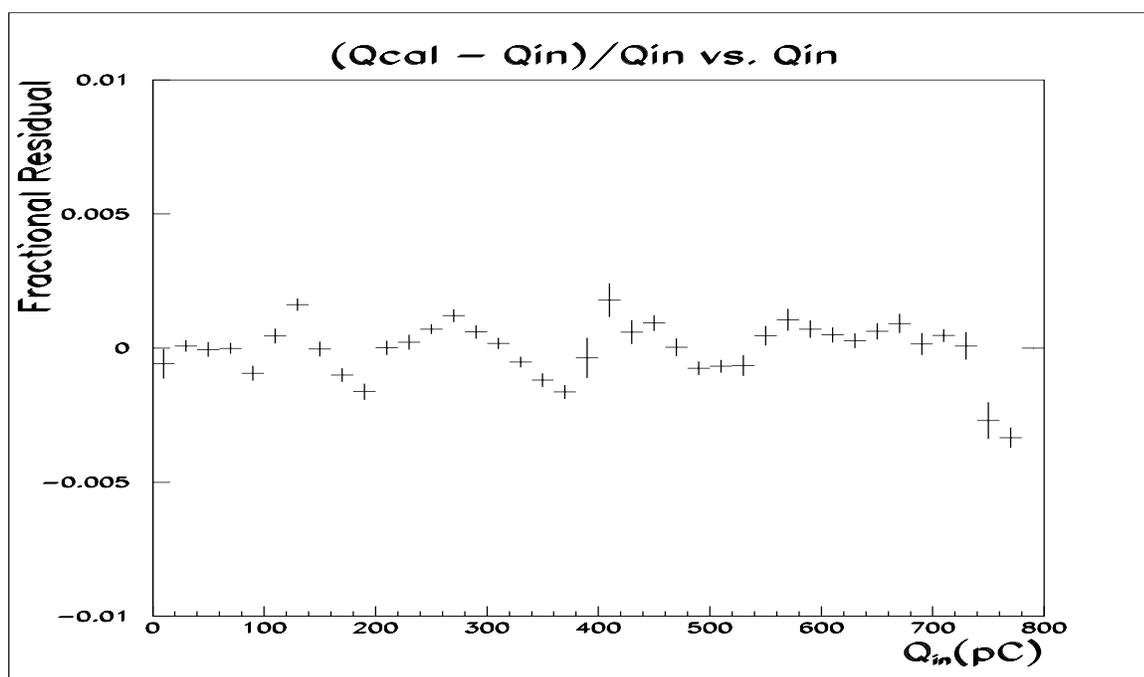


Figure 4: Deviations from expected response after linearizing the DPMT output.