Chapter 4

Central Outer Tracker (COT)

4.1 Overview

As in Run I, tracking at large radii in the region $|\eta| \leq 1.0$ is done with a large open cell drift chamber. The goal of the Central Outer Tracker (COT) is to reproduce in the high luminosity Run II environment the positive characteristics of the Run I Central Tracking Chamber (CTC), improve upon identified deficiencies in the CTC design, and fit into an integrated tracking plan. In this Chapter, we discuss the detailed design of the COT and some performance expectations based on a straightforward scaling of CTC data.

The simplest strategy for operating a wire chamber in Run II is to ensure that the maximum drift time is less than the 132 nsec bunch spacing. The COT is designed to operate with a maximum drift of 100 nsec (compared with 706 nsec for the CTC) by reducing the maximum drift distance and by using a gas mixture with a faster drift velocity. A gas mixture containing 50:35:15 Ar-Et-CF_4 has drift velocity of ~ 100 μm/ns which implies a maximum drift distance of ~ 1 cm, about 1/4th that of the CTC. The simplest COT geometry would then be reminiscent of the CTC, but with 4 times the number of cells.

The similarity of the COT and CTC geometries implies that the COT and CTC performance should be similar at equal occupancy. Since both chambers integrate just one crossing, equal occupancy occurs for equal luminosity per bunch, and to lowest order the COT is expected to perform as the CTC, but at luminosities higher by the ratio of the number of bunches. An additional factor for increased luminosity reach comes from faster electronics and an advantageous geometry for more uniform charge collection. In Run I, the CTC performed well in 6 bunch operation at luminosities exceeding 2×10^{31} cm^{-1}s^{-1}. In 36 bunch operation, the COT would be expected to have the same performance at luminosities approximately eight times greater. In 108 bunch operation, the COT will expected to provide similar performance at a luminosity of $\sim 4 \times 10^{32}$ cm^{-1}s^{-1} – well above the anticipation for Run II.

We emphasize that this extrapolation from CTC performance does not include the effects of changes and improvements in the COT design. An accurate performance measure requires a detailed simulation, and we present the results of such a study in Chapter 7. However, the simple data driven nature of the scaling argument gives us deep confidence in this design.

One improvement in the COT is to remedy the weak stereo in the CTC. CTC r-z (stereo) reconstruction has four superlayers each having only six stereo wires, and Sec.3.2 discussed its weakness relative to the axial layers. At higher Run II luminosities, the stereo reconstruction in such a design would be further degraded by the presence of overlapping hits from multiple interactions. To improve the robustness of the COT stereo capabilities, the four stereo COT superlayers each consist of 12 sense wires, just like the axial layers. This design commonality also allows all superlayers to use the same electronics, wire guides, etc.

Besides a larger number of cells and additional stereo wires, several other geometric features of the CTC are modified in the COT design. In the CTC, the electrostatics of a cell is shaped by field wires whose potential varies to account for the tapered shape of the cell. In the COT, the field wires are replaced by a cathode "field panel" which is gold on a 0.25 mil thick Mylar sheet. Figure 4.1 illustrates the cell geometry using SL2 as an example. To adjust the electrostatics for the cell taper, the COT adjusts the voltage on the sense and potential wires within the cell. With a solid sheet for the cathode, the drift

field and cathode surface field are the same, which allows for a much higher drift fields than is possible with the CTC. With the smaller drift length it is advantageous to use a smaller tilt. We therefore raise the electric field to $\sim$ 2.5 kV/cm (compared with 1.3 kV/cm in the CTC) for a 35° Lorentz angle (compared with 45° in the CTC).

The ends of each cell are closed, both mechanically and electrostatically, by Mylar strips with field-shaping wires attached. These are referred to as inner (smaller radius) and outer (larger radius) "shaper panels." This is the electrostatic equivalent of the CTC's "shaper wires." The field and shaper panel design has an additional advantage of being able to contain a broken wire within one cell, minimizing the loss. The cell design with field and shaper panels also allows for a smaller gap between superlayers so that eight superlayers each with 12 wires can fit between the radii of 40 and 137 cm.

Between the field panels, sense wires alternate with potential wires in a plane. Wires are held and positioned by epoxying and soldering to a G10 board. We use 1.6 mil gold-plated tungsten wire for both sense and potential wires. Limitations in the range of gains and drift fields imposed by this choice of wires is discussed in the electrostatics section.

Figure 4.2 shows the (East) endplate layout. The longer slots are for field sheets, the shorter ones with a notch are for shaper panels and sense wires.

Table 4.1 summarizes the differences between the CTC and COT. In short, the design of the COT is guided by our experience with the similar CTC. The technology of operating such a wire based tracking chamber in a hadron collider environment is proven. The design differences of the COT allow for overall improvements and include straight-forward modifications of proven principles while allowing for operation in a Run II environment. We now turn to detailed descriptions of the design specifics.

4.2 Mechanical

The mechanical construction of the COT uses a combination of similar techniques used in the CTC construction and improved techniques to achieve better intrinsic precision as well as provide needed support for the COT specific geometry. Aluminum endplates are precision-machined with slots which hold pre-made field panel sheets and sense/potential wire planes.

4.2.1 End Plates

The design of the COT calls for precision-machined endplates as shown in Fig. 4.2. Compared with the CTC beginning at a radius of 27 cm from the beam axis, the COT covers a radial span beginning at 40 cm and ending at 137 cm.

A detailed drawing of sense and field slots is shown in Fig. 4.3. The number of precision edges with tolerance at 1 mil is small – only one surface of the slot edge for both sense and field slots and one edge of the notch on the sense slot. These edges define precision surfaces onto which sense wire planes and field sheets can be positioned. This intrinsic precision aids the track trigger resolution and minimizes the size of offline-determined alignment corrections.

The two endplates will be machined as mirror images. A stereo angle is generated analogous to the CTC: stereo cells will be strung using an offset between slots on opposing endplates. The CTC used a two cell offset and the COT will use an eight cell offset. Since each COT cell is a quarter the size, the COT eight cell offset will provide the same nominal 3° stereo angle as with the CTC. The stereo angle varies slightly with superlayer due to the quantization of cells.

The total force on the end plates from a single cell is given in Tab. 4.3. Each plate is made from 1.625" 6061-T651 aluminum. Finite element analysis (FEA) shows this is sufficient to support the 40 ton load with 300 mil maximum deflection, which is substantially more compared with the CTC's estimated deflection of 55 mil. The endplate deflection has no effect on the axial layers but causes a small change for the stereo layers. The stereo angle for each superlayer will be calculated accounting for the deflection.

The large deflection and use of pre-made parts requires we accurate pre-tensioning of the endplates to have them in their final position before installing wires or sheets. The COT's tungsten wire and Mylar sheets have approximately the same stretch as the CTC wires, so we need comparable precision on the pre-tension. We will use the same technique as the CTC: spring-loaded "piano wire" through each sense wire slot, with tension set by hanging a 15 kg weight on the wire. The procedure is iterative with each iteration obtaining a higher precision on the pre-tension. The first pre-tension with a 1" spring gives at worst 250 mil/1" = 25% precision. The pretension process repeats until an accuracy of 1% (3-4 mil in deflection)

	CTC	COT	
Gas	Ar-Et (50:50)	Ar-Et-CF_4 (50:35:15)	[1]
Max. Drift Distance	3.6 cm	0.88 cm	[2]
Max. Drift Time	706 ns	100 ns	[2,3]
Lorentz Angle	45°	35°	
Drift Field	1.35 kV/cm	2.5 kV/cm	
Radiation Lengths	1.7%	1.6%	
Total layers	84	96	
Layers/SL	12-6-12-6-12-6-12-6-12	12-12-12-12-12-12-12-12	
Stereo angle	±3°	±3°	
Total sense wires	6156	30,240	
Total wires	36,504	63,000	
Endplate Load	25 ton	40 ton	

1. Can also operate with Ar-Et-CF_4 at 2.34 kV/cm or Ar-Et at 1.9 kV/cm
2. Typical at center of superlayer.
3. Assuming Ar-Et-CF_4; 200 ns with Ar-Et.

Table 4.1: Comparison of CTC and COT.

Number of Layers	96
Number of Superlayers	8
Stereo Angle	+3 0 -3 0 +3 0 -3 0°
Cells/Layer	168 192 240 288 336 384 432 480
Sense wires/Cell	12 12 12 12 12 12 12 12
Radius at Center of SL	46 58 70 82 94 106 119 131cm
Sense wire Spacing	0.3″ (7.62 mm) in plane of wires
Wire Diameter	1.6 mil gold plated Tungsten
Wire tension	135 g
Tilt Angle	35°
Length of Active Region	310 cm
Total number of Wires	63000
Endplate Load	∼ 40 metric tons
Drift Field	2.5–3kV/cm (depending on gas)

Table 4.2: COT Mechanical Summary.

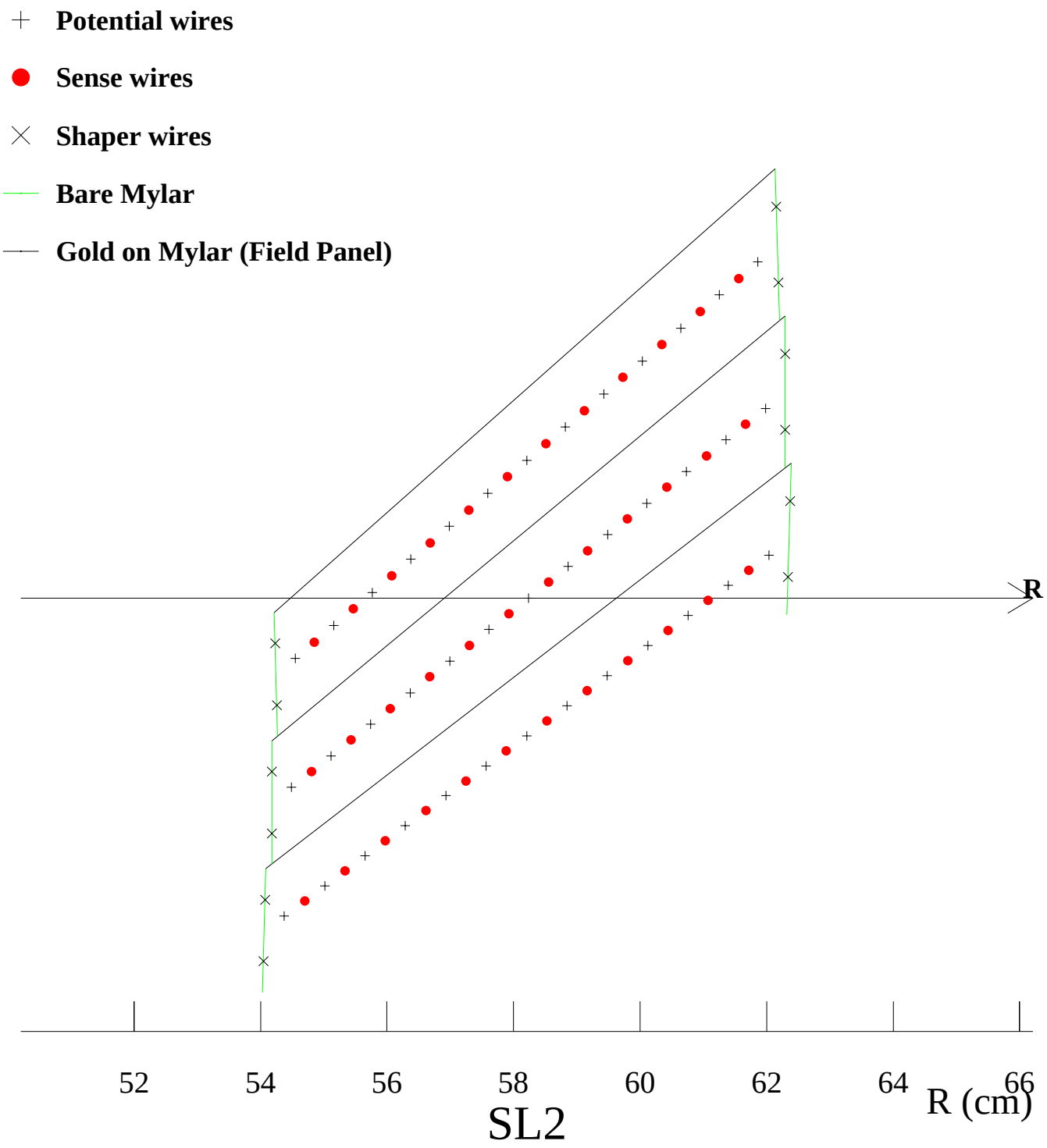

Figure 4.1: Nominal cell layout for SL2. Other superlayers — including stereo — are similar except for the taper.

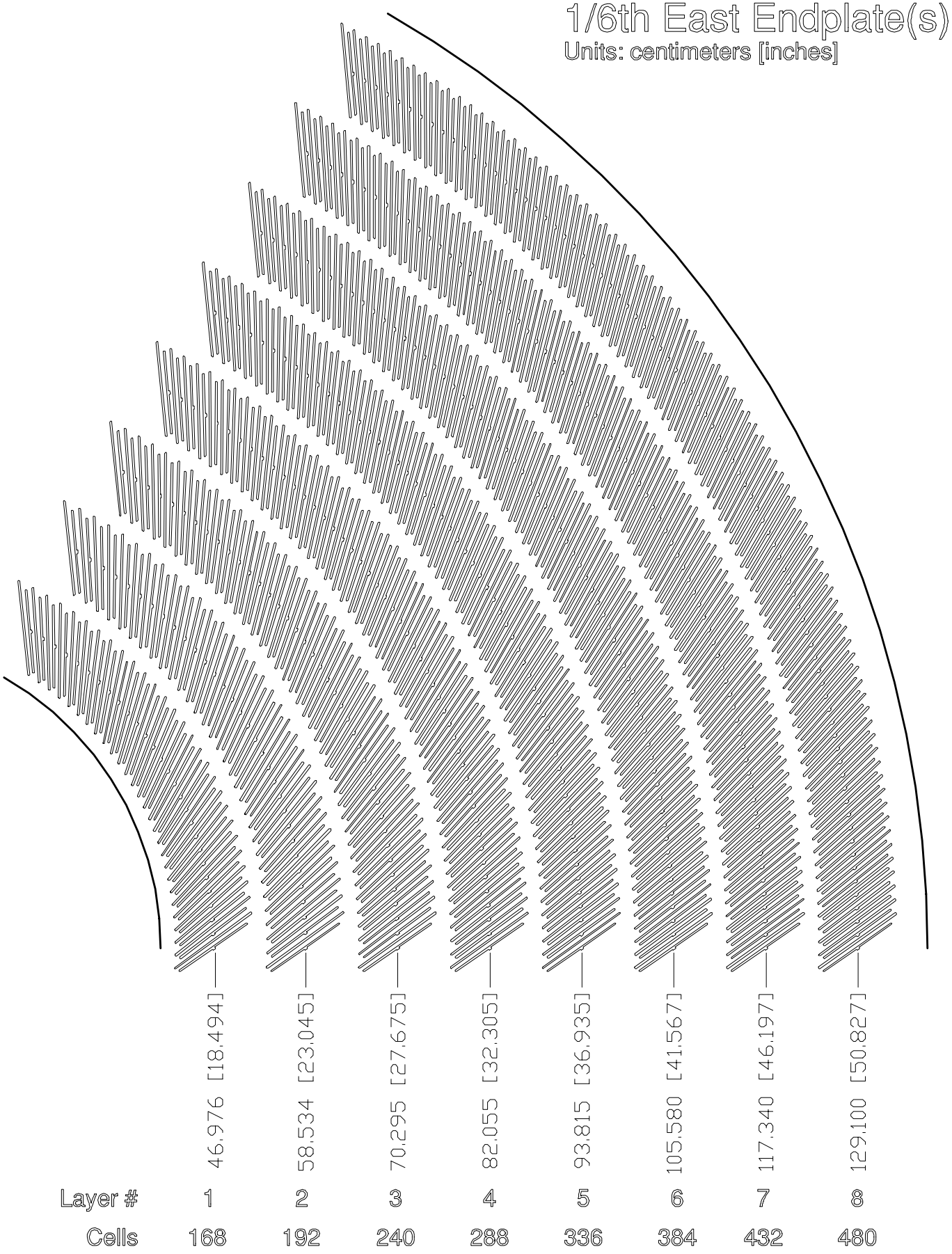

Figure 4.2: East endplate slots Sense and field planes are at the clock-wise edge of each slot.

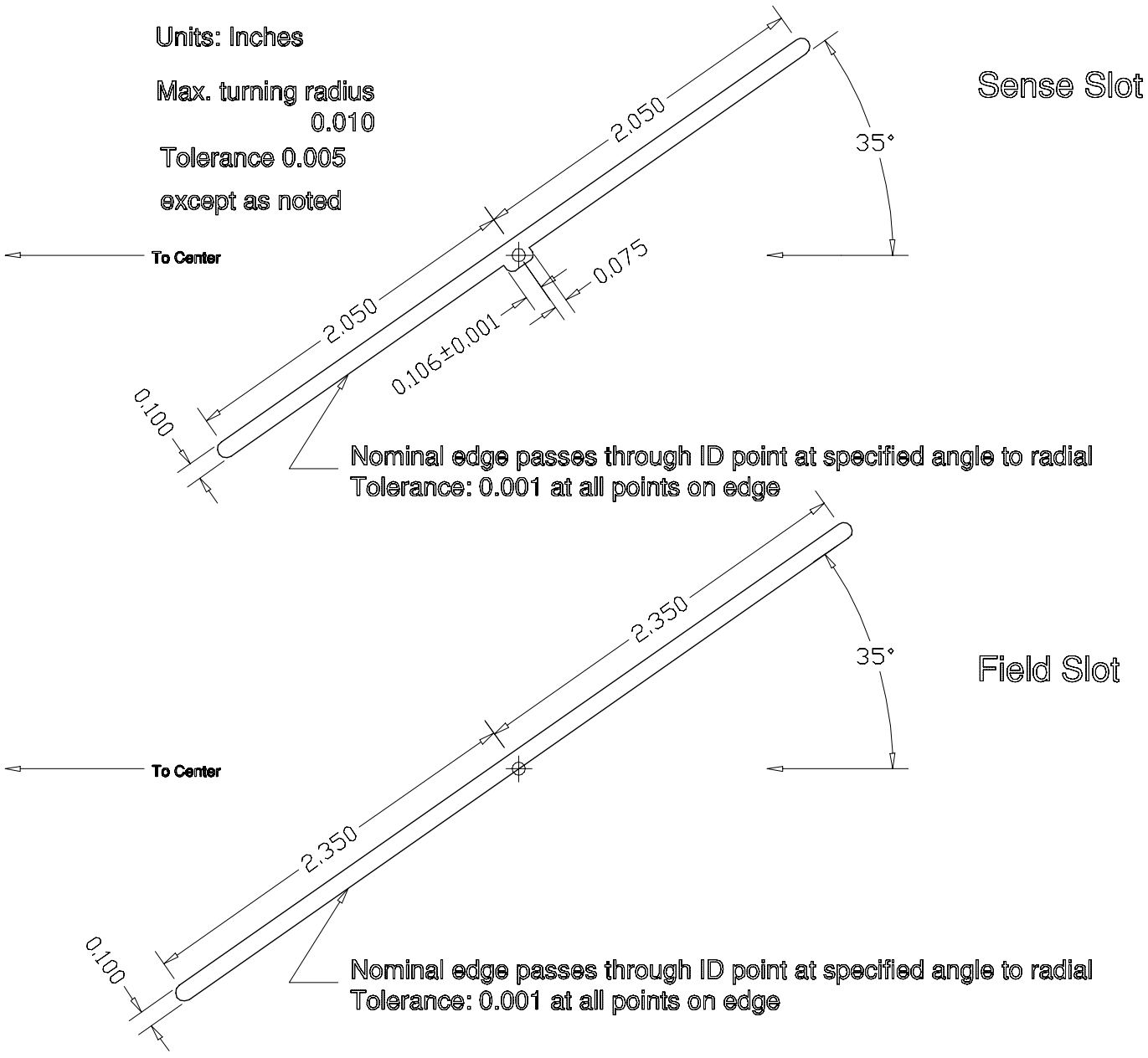

Figure 4.3: Slot details

			Cell Area (cm^2)	Density (g/cm^3)	Cell Density (g/cm)	Sag (cm)	Cell Tension (kg)	Modulus (Mpsi)	Stretch (inch)	Stress (kpsi)	X_0 (g/cm^2)	$<L>/X_0$
Field Sheet					**0.023069**	**0.0278**	**9.98**		**0.40**			**0.61%**
0.25	*mil*	Mylar	0.006452	1.39	0.008968			0.67		2.12	39.95	0.10%
4.50E-06	*cm*	Gold	0.000091	19.32	0.001767						6.44	0.12%
12	*mil*	SS wire	0.001459	7.75	0.011310			28.00		88.65	13.84	0.37%
		Epoxy			0.001025						40.00	0.01%
Wire Plane					**0.006572**	**0.0234**	**3.38**					**0.44%**
1.6	*mil*	Tungsten	0.000324	19.30	0.006259					148.0	6.76	0.42%
5%		Gold			0.000313						6.44	0.02%
Shaper Panel					**0.005224**	**0.0445**	**1.40**		**0.38**			**0.11%**
0.25	*mil*	Mylar	0.002250	1.39	0.003127			0.67		2.03	39.95	0.04%
4.50E-06	*cm*	Gold	0.000016	19.32	0.000308						6.44	0.02%
		Rohacell+Epoxy			0.000375						40.00	0.00%
3	*mil*	SS wire	0.000182	7.75	0.001414			28.00		84.93	13.84	0.05%
Total (2520 cells)							**37,187**					**1.15%**
			Fraction	**Length (cm)**							**X_0 (cm)**	**$<L>/X_0$**
Gas												**0.54%**
		Argon	50%	92.49							10,983	0.42%
		Ethane	35%	92.49							34,035	0.10%
		CF_4	15%	92.49							64,000	0.02%
Total												**1.69%**

Table 4.3: Material in COT active volume

is achieved.

4.2.2 Field Panels

The field panels consist of 0.25 mil Mylar with 450 Å gold completely covering both sides. The edges have 12 mil stainless steel (SS) wires epoxied to the Mylar in a parabola (very small curvature), as shown in Fig. 4.4. The parabolic shape of these edge wires converts wire tension to a uniform lateral tension on the Mylar. Mass, tension, and radiation lengths are given in Tab. 4.3. Note $> 90\%$ of the load is carried by the stainless steel wire.

For prototyping the field panel and its manufacturing process, we have used ~ 500Å aluminum on 0.25 mil Mylar, as well as with gold-on-Mylar sheets. With these prototypes we have investigated a number of areas of potential concern and have found that the gold on Mylar field panel design should work well with the COT.

A mechanical concern associated with the field panels is whether a constructed panel is stable after installation so that a drift cell experiences uniform and understood electrostatic properties. The elongation of the sheet is 0.35 cm, or 0.11%. We have checked published creep properties of Mylar and find the creep of Mylar is small, and most of it occurs within a few days. We have checked the flatness of field panels as a function of time over a period of several weeks and find no measurable variation.

The measured sag in the longitudinal direction is 300 μm with an additional 100 μm sag along the lateral direction, in agreement with the expected properties of the sheet. The lateral variation cannot be matched by the wires, resulting in $\sim 1\%$ variation in drift field. Note this uniform shift does *not* affect wire gain since the sheets on both sides sag the same amount, and the (small) effect on drift parameters can be mapped out.

Ripples of ~ 100 μm amplitude (~ 200 μm peak-to-peak) are also observed on some sheets. We have simulated the effect of such ripples on drift trajectories and wire gain using an electrostatics program which varies the amplitude while keeping the spacing fixed. Based on this, we find up to ~ 300 μm ripples cause $< 10\%$ variation in sense wire gain and no measurable effect on resolution.

The electrostatics program also shows that ~ 100 μm variation in sag (where two sheets adjacent to a wire plane move in opposite directions) gives $\sim 10\%$ variation in gain. This effect, rather than ripples, is expected to dominate potential gain variation. Unfortunately, it is difficult to distinguish sag from ripple in a simple test fixture. Therefore, for mass production, we define a ± 100 μm envelope around the nominal sheet position using a large grid of test

probes, and require all sheets lie within this window.

We have also done qualitative checks for the effect of local damage to the sheet by creating small tears in it. We found no visible impact on the surface quality beyond the tear itself. Visual inspection (using the mirrored surface) allows us to check for ripples at the 20 μm level.

We are also investigating the use of slightly conductive epoxies in order to prevent a possible charge-up problem on the Mylar. Adhesion to the epoxy to the material has been shown to be more than adequate in several tests at full tension.

4.2.3 Shaper Panel

The shaper panel consists of 0.25 mil Mylar coated on one side with 450 Å gold, plus two 3 mil stainless steel wires. The metalized Mylar is kept at ground, while the wires are connected to their nearest potential wires. Electrostatically, this gives adequate closure of the cells' end-effects.

By varying the assumed position in an electrostatics program, we have determined that 1000 μm uncertainty in the position of the side panel has less effect on the drift trajectories and sense wire gain than the 100 μm uncertainty in the field plane.

Because the shaper panel is narrow, and its position is not critical, it is held by simple tension on the Mylar and wires (no curve like that of the field panels). Electrostatic attraction between the wires (at $\sim$ 2 kV) and metalized Mylar (at ground) is counteracted by three evenly spaced Rohacell spacers. The mass of the Mylar-epoxy spacers is a negligible 6 mg per spacer (including epoxy).

4.2.4 Wires

The sense and potential wire planes are designed for precision placement and for having uniform electrostatic properties over the length of the chamber. Sense and potential wires are gold-plated tungsten (450 Å gold on 1.6 mil diameter tungsten) strung at 135 g tension.

The smaller drift length in the COT requires a correspondingly smaller "differential sag" than allowed in the CTC (600 μm sag on field wires, 230 μm on sense wires, 370 μm differential sag). We design for 300 μm nominal sag on sense wires and field wires which is equal to the sag expected for the field panels, i.e. zero differential sag. We allow no more than 100 μm variation in distance between the wires and the field panel.

To improve electrostatic stability at drift fields up to 2.5 kV/cm, the wire plane includes a wire support at the center. The wire support mechanically ties the wires to each other, removing "stepping" arising from wire-to-wire repulsion.

The 135 g tension per wire is required to assure stability against the coherent motion (i.e., all wires together) of the wire plane toward the field sheets. The wire sag at this tension is slightly less than the field sheets (Tab. 4.3); we deliberately increase the mass of the wire support until the wire sag matches the field sheet sag.

Wire planes are manufactured by winding $\sim$ 40 cells worth at one time on a large winding machine, analogous to the procedure used for MWPC construction. The winding machine has attached precision fixtures to define the location of the wires relative to a reference pin (for position along the wire plane) and a support rib (for position perpendicular to the plane) on the wire plane end-boards. These precision fixtures duplicate the geometry of the endplate and will allow wire planes to be inserted into the precision machined endplate with $\sim$1 mil accuracy. There will be some adjustment on the wire plane winding fixtures to allow for slightly different lengths due to the 300 mil expected endplate deflection.

Two additional advantages of the wire plane manufacturing procedure are that the wire planes can be built in advance of the chamber and that the completed wire planes can be tested prior to installation. We plan to expose each wire plane to a β-source to emulate high-rate operation. We expect this will substantially reduce the burn-in time and failures during data taking.

4.3 Material Count and Radiation Lengths

The contribution of each material is given in Tab. 4.3. We use:

$$L/X_0 = \underbrace{\frac{L}{A}}_{1/\text{width}} \times \frac{\varrho}{X_{0,\text{g/cm}^2}}$$

where ϱ is the linear density in g/cm. The "width" of a cell is simply the circumference of the superlayer divided by the number of cells; this is $\sim$ 1.76 cm

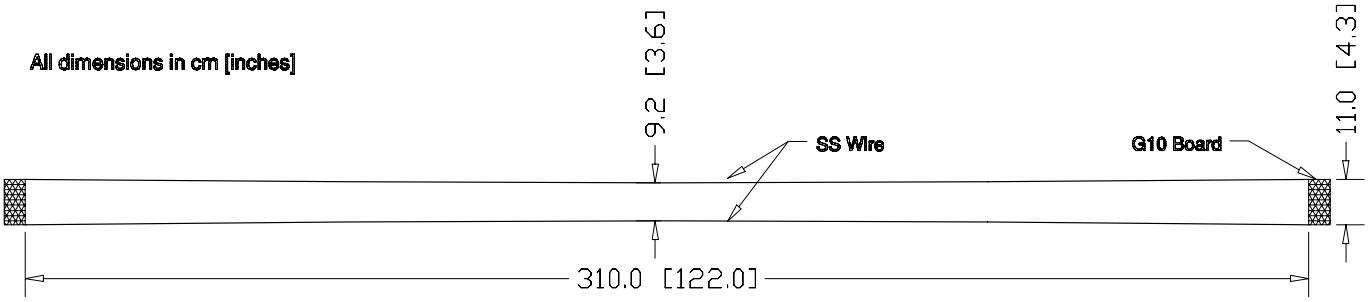

Figure 4.4: Field panel construction Curved string introduces a lateral force.

(twice the drift distance).

The various materials are combined by summing L/X_0 contributions and we find a total L/X_0 of 1.69%.

4.4 Electrostatics and High Voltage

In setting actual voltages, a full electrostatics calculation and fitting program is used. However, the following simple relations are useful in designing the HV system.

Treating the wires as lines of charge and ignoring edge effects, the drift field (E far from the line charges) is related to the wire surface field by

$$E_d = \frac{\pi}{s}(E_s r_s + E_p r_p)$$

where: s is the spacing between sense wires; E_s (E_p) are the surface fields of the sense (potential) wires; and r_s (r_p) are the radii of the sense (potential) wires. For uniform gain, E_s must be the same for all wires. The above relation assumes E_p are also the same, but by treating this as operative over a subset of the wires, we see that uniform E_p (given uniform E_s) is a requirement for a uniform E_d.

For uniform E_s (E_p), the field in the vicinity of each sense (potential) wire is the same; by design, far from the wires, $\vec{E}_d$ is also everywhere the same. Then the voltage of a wire is

$$V = V_0 + dE_d$$

where: d is the distance along $\vec{E}_d$, i.e. perpendicular to the field panels; and V_0 is a constant for all sense or potential wires.

We can immediately get the variation of voltage across the sense or potential wires as being

$$\Delta V = \frac{\Delta R}{R} E_d d_0$$

where: R is the radius at the center of the superlayer (varies); $\Delta R \sim 4.3$ cm is the radial extent of the superlayer; and $d_0 \sim 0.75$ cm is the distance between the wires and the field panel at the center of the superlayer. SL1 (smallest R) and $E_d = 3$ kV/cm (a reasonable safety margin over the anticipated operating point of 2.5 kV/cm) has a ΔV of 210 V.

4.4.1 Currents (Voltage sags and space charge distortions)

The field panel design has been examined for potential electrostatic problems. We consider the expected current on the field panels. The resistance of 450 Å gold is $\sim 0.36\ \Omega$/cm for our $\sim$10cm wide sheet. We can estimate the expected current on the field panels by extrapolating from the sense wire current observed with the CTC. The sense wire current in SL1 of the CTC at $\mathcal{L} \sim 10^{31}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ is $\sim 0.5\mu$A/wire. Extrapolating to $\mathcal{L} = 10^{33}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ to be conservative, with one quarter the drift length, the maximum expected current per sense wire is 12.5μA. Most of the ions end up at the field panel for a total current of 75μA at each surface. Based on the VTX experience, we expect this current is spread uniformly in z along each wire. Then the voltage drop from the end plates to $z = 0$ is

$$\Delta V = \tfrac{1}{4} \times 75\ \mu\mathrm{A} \times 0.36\ \Omega/\mathrm{cm} \times 160\ \mathrm{cm} = 1.1\ \mathrm{mV}$$

which is certainly not a problem.

At most, half the ions from the inner and outer most sense wires will go to the wires on the shaper panels. Therefore the voltage sag here will be at most half that along the sense wire.

Due to the higher drift field (about 2.5 kV/cm versus 1.3 kV/cm) and much shorter maximum drift length (0.88 cm versus 3.5 cm) of the COT compared with the CTC, space charge distortions in the COT should be less than a few percent of those in the CTC

for the same sense wire current. Since the COT sense wire current is a factor of four less than the CTC's at the same luminosity, space charge distortions will be very small in the COT during Run II.

4.4.2 High Voltage System

The high voltage system is similar to the system used for the CTC. Supplies and crowbars are located in the first floor counting room; filtering and fanout is done in the collision hall off of the chamber face and voltage is delivered to the chamber by superlayer and by quadrant. The precision required and high current draw (12.5 μA maximum) for the sense wires rules out a resistor divider chain. Current draw on the potential wires is low, but for simplicity and flexibility we will distribute these voltages in the same way as sense wires.

4.4.2.1 First Floor

High voltage will be supplied by VME-based pods. 200 HV channels are required, 25 per superlayer (12 sense wires and 13 potential wires). Each pod delivers up to 3 mA at 3.5 kV. The system is controlled by a PC.

Short RG-58 cables bring the voltage from the power supplies to the crowbar system. The crowbar system discharges the cables in the event of a trip in order to minimize the amount of energy dumped into the chamber. The crowbar relays are in-hand from the existing system, but a new crowbar driver board will need to be built.

After the crowbar system, the 200 channels fanout 1-to-4 for distribution by quadrant. 800 RG-58 cables carry the HV from the fanout to the collision hall.

4.4.2.2 Collision Hall

The 800 RG-58 cables connect to eight different filter boxes within the collision hall, one filter box per quadrant. The filter boxes electrically isolate the chamber ground from the first floor, as well as perform the transition from RG-58 to ribbon cable.

Although the sense wires are run at $\sim$ 3 kV, and potential wires are run at $\sim$ 2 kV, the voltage difference from wire-to-wire for all sense, or all potential, is $<$ 300 V; difference between neighboring wires is $<$ 25 V. Therefore, a 300 V rated ribbon cable is used for all sense wires, a second ribbon cable for all potential wires. The cables are isolated from ground by kapton wrap and plug in to mass-terminated connectors on both ends. The cables are also covered by copper cloth to eliminate shock hazard. There is one sense wire ribbon cable and one potential wire ribbon cable per superlayer per quadrant. The voltage for the wires on each the shaper panel is the same as for its neighboring potential wire; they will be tied to the corresponding potential wires.

An interlock ensures that the ΔV across any cable does not exceed the cable rating. This is done by putting a 1.5 kW, 200 V "transient suppression" diode per line, which absorbs a large energy dump in a short time period and causes a high voltage supply trip.

4.4.2.3 Chamber End Plate

High voltage is distributed to the chamber on the end opposite the readout. The ribbon cables plug into a $4'' \times 2''$ two-layer printed circuit board. This board brings the HV into the chamber and has 25 capacitors, 25 HV feed resistors, 12 termination resistors (sense wires only), two headers for the ribbon cables, and pin receptacles to mate to the gas seal board.

4.4.2.4 Failure Modes

In the case of a "bad" (*e.g.* glowing) wire, without access to the chamber face, it is possible to drop the gain of one layer of the quadrant by a factor of 2–4 by reducing the sense wire voltage by 100–200 V. Also, it is possible to drop the gain of any two layers of the quadrant by a factor of ~ 8 by raising the voltage of the intermediate potential wire. For a broken wire without access to the chamber face, the entire quadrant must be turned off.

With access to the chamber face, any one wire can be disconnected by clipping the HV feed resistor. It is also possible to disconnect an entire cell by pulling the connector from the termination board. This kills one cell and degrades the two neighboring cells because of the electrostatic pull on the field sheets.

4.4.3 Electrostatics

Figure 4.5 shows equi-potential and equi-$|E|$-field surfaces for the preferred drift field (2.5 kV/cm), wire size (1.6 mil) and gain setting (180 kV/cm surface field). The field along the drift trajectories is found to be very uniform. In this case, the electrostatics program used only 4 free parameters: the voltages at

SL	1	2	3	4	5	6	7	8
%/fb^{-1}	64	54	36	28	23	18	15	12

Table 4.4: Ageing rate vs SL. Assumes same gain loss per unit charge at sense wire as CTC toward end of Run-1B and chamber gain equal to CTC outer layer. We consider this an overly conservative projection, as explained in the text.

the inner and outer most sense and potential wires. Shaper panel voltages were set the same as the neighboring potential wire, and intervening wires were set by uniform steps. More uniform gain is possible by fine-tuning the individual wires.

The 2.5 kV/cm drift, 180 kV/cm surface field solution gives a potential wire surface field of 118 kV/cm (positive charge). So, it will have negligible gain. The sense wire gain changes a factor of two for every 6 kV/cm change in surface field, and the simple model given earlier tells us the potential wire charge has to change an equal amount in the opposite direction to keep the drift field fixed. Since the gain on the potential wires does not change by much, a wide range of drift fields and sense wire gains are accessible.

4.5 Gas System and Wire Ageing

4.5.1 CTC Wire ageing CTC in Ar-Et

The CTC drift gas was Argon/Ethane (50/50) bubbled through ethanol during the entire operation. We have made measurements of ageing effects in the CTC and in "Magic Chambers," drift tubes located at the gas input and output. We consider measurements beginning in March 1995 (after the gas system was cleaned). Table 4.4 scales the ageing effects to COT operation using charge collection rates of the CTC superlayers, scaled down a factor of four for the reduced drift length. We further scale the rate of the SL1 and SL2 by a factor of two (the chamber gain of the CTC is a factor of two lower in these layers). The effect of ageing is to reduce the sense wire gain.

The estimates shown in Tab. 4.4 are pessimistic for several reasons. First, they assume that the chamber gain is kept at the value used in the CTC outer layers, whereas the inner CTC layers were at approximately half that gain. Second, there is reason to believe the ageing in standard Ar-Et alcohol mixtures can be substantially improved by further cleaning of the CDF gas system and more effort to reduce alcohol mist entering the CTC. For example, the ageing of SL3 was twice as high before the gas system cleanup began. Also, a Magic Chamber at the CTC gas input showed a factor of two reduction in ageing in the last few weeks of Run IB, after the cleanup was complete.

Further improvements were observed in the input Magic Chamber (another two orders of magnitude) after the system was modified so that only a small fraction of the gas was run through the alcohol bubbler and heated copper filters were added. Both changes were intended to reduce alcohol mist arriving at the Magic Chambers and CTC. Unfortunately, there is insufficient integrated luminosity to get a direct measurement of the effect on the CTC. However, chemical analysis of CTC and Magic Chamber sense wires show they have similar contaminants after ageing so that we hope that the CTC ageing rate was also significantly reduced by the changes to the alcohol delivery system.

Additional cleaning of the CDF gas system will be done. However, since there is not a conclusive demonstration of a substantially lower ageing rate in the CTC with Ar-Et alone, the ageing rates for the COT would be worrisome in Run II if Ar-Et alone were to be used (without CF_4).

4.5.2 COT Wire Ageing in Ar-Et-CF_4.

Adding as little as 5% CF_4 has been found to reduce or eliminate wire ageing in Ar-Et [2]. Therefore, for operation with 396 ns bunch spacing, we have measured the drift velocity and Lorentz angle at 14.1 kG for the gas mixture of Ar-Et-CF_4 (50:45:5) bubbled through isopropyl alcohol. The expected COT operating point in this mixture is 2.3 kV/cm drift field and 64 μm/ns drift velocity.

For 132 ns bunch spacing, we require a much faster drift velocity in order to resolve crossings and minimize the occupancy. The gas mixture Ar-Et-CF_4 (50:35:15) bubbled through isopropyl alcohol was also measured at 14.1 kG. It has an operating point of 88 μm/ns at 2.5 kV/cm, giving a 100 ns maximum drift time in the COT. We have measured the ageing properties of this gas mixture using a realistic prototype COT cell, including field panels constructed from vapor deposited gold on 0.25 mil Mylar. Sense wires in the chamber were irradiated using a range of beta source intensities corresponding to instan-

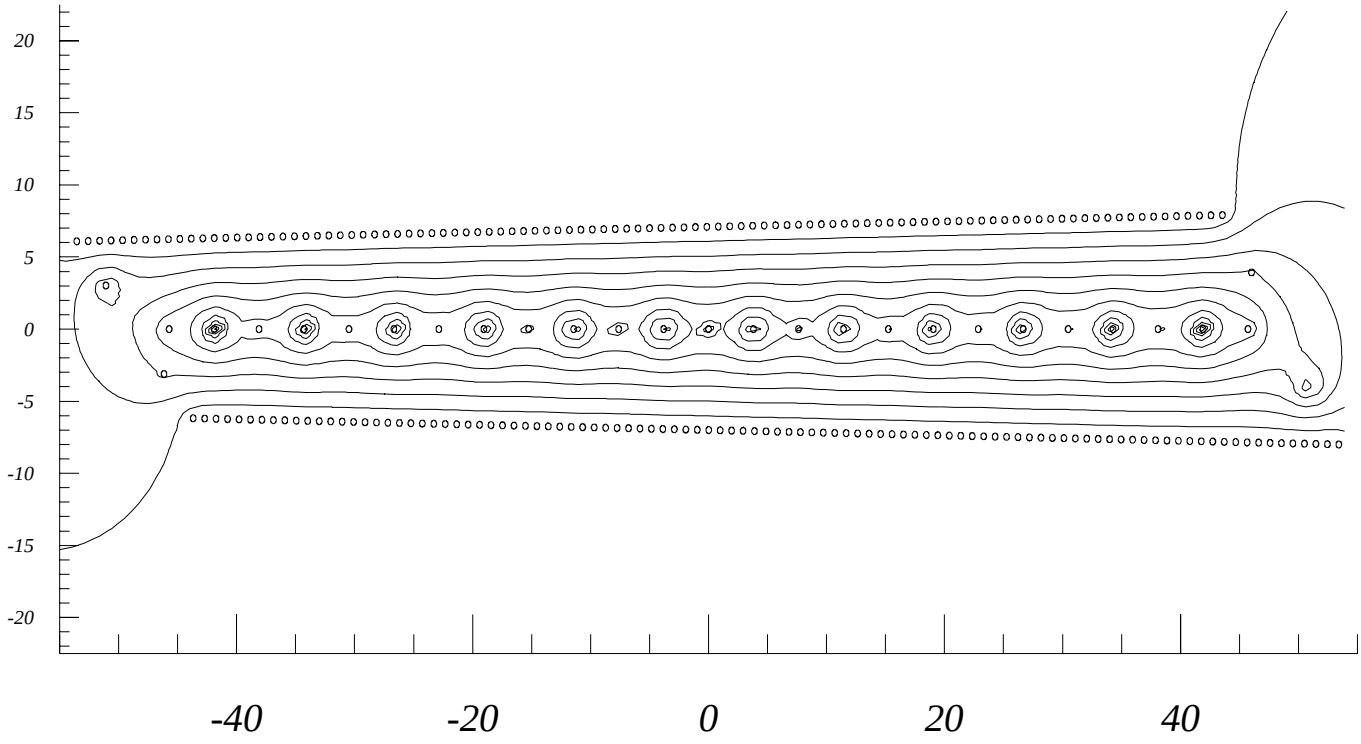

Figure 4.5: Equi-potential lines in SL1 (the superlayer with the largest taper).

taneous luminosities of approximately 10^{32} $cm^{-2}s^{-1}$ to 10^{33} $cm^{-2}s^{-1}$ resulting in charge accumulations of 0.05 Coul/(cm of sense wire) to 0.5 Coul/(cm of sense wire), respectively. Note that the COT inner layers will accumulate roughly 0.1 Coul/(cm of sense wire) at an integrated luminosity of 2 fb^{-1}. No where in the chamber did we observe Malter-effect currents, visible cathode etching, visible cathode or anode growths, or significant gain loss. In particular, the resistance of the cathode changed by less than 10% (the uniformity of the unirradiated material), the gain loss averaged over all sense wires was (0.7 +/- 0.8)%/Coul/(cm of sense wire), and the measured rate of gain loss for wires irradiated at Run II intensities implies a gain loss of less than 10% for the COT inner layers at 2 fb^{-1}. The ageing tests will continue with this gas mixture, the mixture with 5% CF_4, and other candidates.

The major drawback to CF_4 is cost. To keep this at a tolerable level, it may be necessary to re-cycle the gas. Of course, besides the impact on the chamber design, re-cycling requires a pumping and cleaning system. The Fermilab Physics Department will assist CDF in the design of the re-cycling system.

4.6 Readout Electronics and Trigger

The COT has 30,240 channels: 16,128 axial and 14,112 stereo. The breakdown by superlayer is shown in Table 4.5. The electronics and trigger systems of the COT are largely based upon the designs utilized for the CTC. Data acquisition is based upon standardized modules used elsewhere in the Run II CDF design.

The overall layout of the COT readout electronics chain is shown in Figure 4.6. Pulse amplification, shaping and discrimination is carried out on the chamber face using an Amplifier/Shaper/Discriminator (ASD) chip developed at the University of Pennsylvania. The differential discriminated signal is carried off the chamber face to TDC boards mounted in VME crates on the endwalls by a two-piece cable consisting of 4 meters of 0.023″ coaxial cable followed by 6 meters of a standard 50 mil spacing ribbon cable. Time-to-digital conversion is performed with TDCs designed at the University of Michigan for the Run II upgraded muon system. The TDC boards contain Level 1 and Level 2 trigger event buffering. TDC auxiliary cards latch hits for the eXtremely Fast Tracker (XFT) track trig-

Layer	Number of Cells	Sense Wires	ASD Boards
1	168	2016	84
2	192	2304	96
3	240	2880	120
4	288	3456	144
5	336	4032	168
6	384	4608	192
7	432	5184	216
8	480	5760	240
axial total (2,4,6,8)		16,128	672
stereo total (1,3,5,7)		14,112	588
total		30,240	1260

Table 4.5: Numbers of cells and sense wires per superlayer. Twelve sense wires per cell.

ger processor. (See Section 12.3 for details of the XFT.) Latched hit data are multiplexed and sent up to the first floor counting room via Ansley cables (we plan to reuse existing Ansley cables). Trigger segment finding and linking is done in 6 VME crates in the first floor counting room. Digitized timing information for the COT is readout via serial link to first floor VME readout buffers (VRBs) in a fashion similar to the readout of the SVX II.

This design offers the advantage of having all of the electronics except the ASDs off the face of the chamber and therefore accessible. The elements on the chamber face operate continually: no timing signals need to be sent to the chamber.

The following sections will describe the major elements of the COT electronics: front end, ASD, TDC, DAQ, and chamber cooling.

4.6.1 Front End

This section describes the front end board, the ASD chip, signal cables and low voltage power distribution.

4.6.1.1 Boards and connections

A two-layer printed circuit board holds pin receptacles which attach to the pins on the wire board. This motherboard plugs into two cells, holds high voltage decoupling capacitors (1 nF,3 kV for potential wires and 470 pF, 4 kV for sense wires) and provides a portion of the gas seal. Signals are brought out on a single-inline, 36-pin, 0.1″ spacing connector.

A second multi-layer PC board plugs into the motherboard and houses three Penn ASD chips (see Section 4.6.2). The ASD board also holds a calibration receiver, HV protection, crosstalk cancellation resistors, and low voltage bypass capacitors. The board receives ±3VDC for the ASD power.

4.6.1.2 Signal Cables

The ASD provides a programmable differential current output, typically 2 mA into a characteristic cable impedance of 40 Ω to ground. The differential signals are carried off of the chamber face through the gap between the endplug and endwall calorimeters by 0.023″ coaxial cable. Limited cable space through this gap is the motivation for the thin coaxial cable. Outside the endplug-endwall gap, a transition is made to standard 50 mil spacing ribbon cable which carry the signals the remaining $\sim$ 6 meters to the TDC. The larger cable is less expensive and has better transmission properties. The total cable run is approximately 10 meters from the chamber face to the TDC cards on the endwall.

For each ASD board, there is one 50 conductor cable which carries differential signals from 24 channels ($\times$2 per channel for differential output) plus two calibration lines.

The signal cables are terminated by hand into printed circuit boards which plug into the ASD boards and the mass-terminated ribbon cable. Measurements with sample cables indicate that

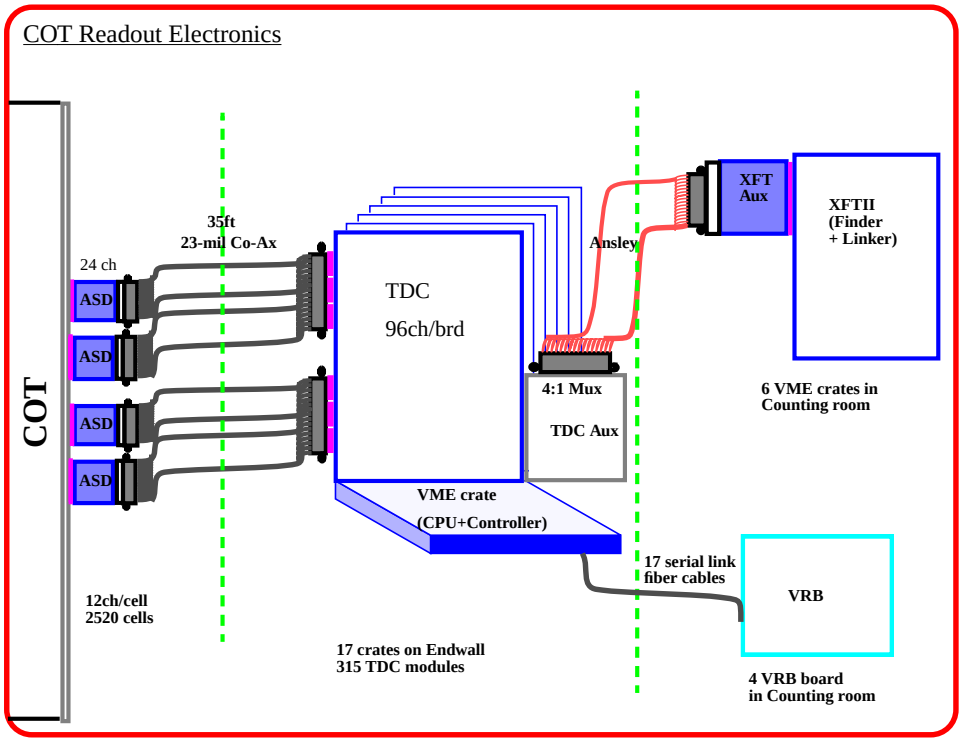

Figure 4.6: An overview of COT readout electronics.

impedance matching between the two cable types, as well as cable compensation, can be done in a straightforward manner. We are in the process of defining the optimal cable compensation circuit.

4.6.1.3 Low Voltage distribution

Two supplies per side per quadrant provide low voltage power (± 3 VDC) to the ASD cards mounted on the chamber end plate. Six cables distribute the voltage from each supply to the chamber. The number of cables is determined by current-per-cable safety requirements.

4.6.2 ASD

An Amplifier/Shaper/Discriminator (ASD) chip was developed for the SDC detector by the University of Pennsylvania group. The Penn ASD chip was optimized for straw systems in the SDC and ATLAS detectors [4]. Given that the charge collection and signal profile for hits in the COT will not be markedly different than for straws, the basic ASD design is applicable to both systems. The ASD provides all of the analog signal processing between the chamber and the TDC. The chip is fabricated by the inherently radiation hard bipolar process. Each channel of the eight-channel chip has a fast, low noise preamplifier, ion tail cancellation stage and discriminator. The shaping and discriminator stages are fully differential, the preamplifier is pseudo-differential.

In the proposed version of the ASD, a baseline restorer stage will be included before the discriminator to prevent changes in the effective threshold at high hit rates. A measurement of the charge will be encoded into the width of the discriminator output pulse in a manner similar to that employed by the CTC outer superlayers. This dE/dx measurement will cover about 16 bins of 1 ns resolution. The 24-channel ASD board, located on the chamber end plate, handles two 12-wire drift cells with three 8-channel ASDs per board.

4.6.2.1 Baseline Restoration

The multihit nature of the COT requires that the ASD not only shape the signal for optimal two-track resolution but also that high rates and/or large hits do not cause large baseline variations. Changes in baseline can distort the pulse shape and degrade the time resolution performance of a second hit. A version of the ASD with baseline restoration has been developed for the ATLAS Transition Radiation Tracker [5]. Optimization of the shaping and base-

line restoration for the COT will be done using data from the CTC and COT prototype chamber, as well as from SPICE model simulations of chamber and circuit performance.

4.6.2.2 dE/dx

The ASD will also be designed to encode the magnitude of the charge deposited in the chamber cell in the trailing edge of the discriminator output pulse. In this scheme, the leading edge of the discriminator output indicates the time of arrival of the primary ionization and the trailing edge (*e.g.* the pulse width) is logarithmically related to the total charge deposited on the sense wire.

For the CTC, superlayers 3–8 (54 layers) are instrumented with dE/dx circuitry. The resolution for the CTC is dominated by the sampling statistics and is measured to be approximately 10%. The dE/dx resolution and hence, particle identification capability of the COT will be better because all 96 layers will be instrumented with charge measurement capabilities. Also, due to the more uniform drift field of the COT near the cathode planes, a larger fraction of hits will be used to determine the dE/dx for each track.

In a fashion similar to the CTC, a tradeoff between two-hit resolution and dE/dx resolution is achieved by implementing a logarithmic relationship between the measured charge and the time over threshold ($\Delta t \sim \log(Q)$). This keeps the time for the trailing edge encoding short (approximately 10–15 ns beyond the width of the shaped pulse) while maintaining good resolution at the lower end of the dE/dx spectrum.

4.6.3 TDC

The signals from the ASD boards are sent differentially to TDC modules via a combination of coaxial cables (two per channel) and ribbon cable (section 4.6.1. A total of 315 TDC modules are located in the 17 VME crates on the endwall of the detector.

The DT96TDC[6] is a 96-channel VME module, being designed for the Run II CDF muon system by University of Michigan group. The TDC is designed to replace the existing Fastbus LeCroy 1879's and includes the necessary event buffering capability, sufficient pipeline length, and the necessary timing resolution[7].

The DT96TDC uses a custom chip, JMC96[8], which has been specifically developed for this TDC module. The JMC96 chip has 1 ns timing, multihit capabilities, and L1/L2 storage buffers. The TDC module contains a standard VME interface, receivers for 96 signals, a Xilinx based register file and a digital signal processor to perform the zero suppression of empty channels. The design of the module is flexible to allow for different readout options using a 32 bit word to encode board/channel ID, the time of the leading edge and the width. The output of the zero suppression is loaded into an on-board FIFO for the transmission via the VME Readout Controller to the 1st floor memories, the VME Readout Buffer modules.

Each TDC crate contains 18 or 19 TDC modules, a CPU crate controller and a TRACER[9]. The Motorola MVME162 is currently being considered for the CPU crate controller to download programs, diagnostics and global control from the DAQ network. The TRACER is a system interface module to provide an interface to the Trigger System Interface and the Master Clock. It also provides a path for sending the event data to the VME Readout Buffer.

4.6.4 DAQ

Data from the TDCs are read by a local processor in the crate and sent to the VME Readout Buffer (VRB)[10] through a TRACER type module. The VRB is a VME based slave module designed to be used in the calorimetry and SVX DAQ system. The VRB receives data via transition module data links, which are typically serial optical connections. The VRB can accept input data at a combined rate of up to 600 MBytes/sec on multiple channels.

The VRB crate is located in the counting room and is controlled by SRCs[11] to the trigger system. Each VRB has 10 channels input up to 50 Mbytes/sec. The output is driven at >40 Mbytes/sec using VME64 protocol.On board SARAM buffers (30 kB/channel) are programmable in terms of number of buffers and sizes. The J3 backplane is used for commands and status.

4.6.5 Trigger

The TDC signals for the axial superlayers are also tapped off of the modules and sent to the track processor (XFT) located in the 1st floor counting room.

The TDC Auxiliary card will take the 96 TDC signals, latch TDC hits in time bins, and send 3-to-1 multiplexed signals to the XFT Auxiliary card via 336 Ansley cables, two cables per TDC Auxiliary card.

The XFT Auxiliary cards reside in the first floor counting room. They demultiplex the latched TDC hits and pass them along to the XFT cards, which house segment finder and linker chips. See Section 12.3 for details of the XFT.

4.6.6 Calibration

Circuit operation can be verified and the system time and charge behavior can be calibrated by injecting charge into the front end of the ASD chip. The current design of the TRACER module will be slightly modified to include calibration capability. In calibration mode, the modified TRACER sends pulses along the VME backplane to each TDC board in the VME crate. The TDC in turn transmits the pulse down to the ASD cards through a single channel which is a part of the 50-conductor signal cable. The signal is received on the ASD board and injected into the chips via a pulse forming network.

4.6.7 Cooling

In the Run I tracking system, the total heat dissipated from the VTX is 150 W and from the CTC is 310 W, for a total of 460 W. The maximum heat load is on the axial side with 75 W (VTX) + 225 W (CTC) = 300 W. The CTC and VTX are cooled by the solenoid cryostat and chilled water lines connected to the CTC endplate at the inner diameter and outer diameter. Under the present cooling conditions, temperature probes near the CTC preamps read 2–7°C below ambient ("ambient" being the temperature when both power and cooling are turned off).

Assuming that the COT ASD dissipates 30 mW/channel, the total heat load due to the preamps is 907 W. At $4 \times 10^{32}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ we expect a positive ion current in the drift gas of approximately 0.011 Amps per superlayer for a total of 0.089 Amps. For a voltage drop of 3 kV, the heat dissipated in the chamber gas is 266 W. The total heat load becomes 1.2 kW.

To handle this heat load, cooling lines are placed on both ends of the COT at the inner and outer diameters, as well as between each superlayer. Better estimates of cooling requirements will be done in the near future, but we do not anticipate a significant engineering effort.

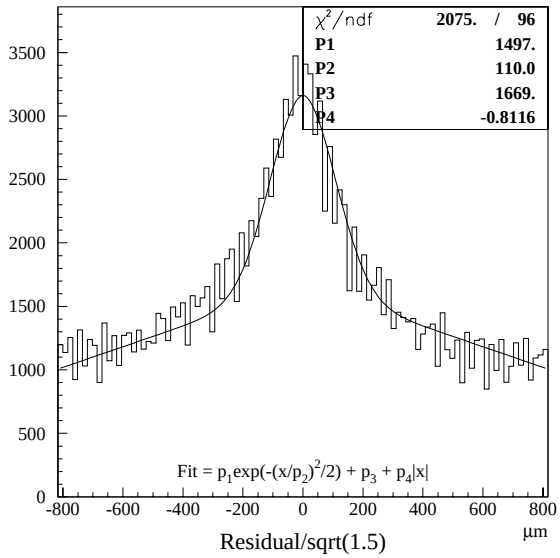

Figure 4.7: COT un-biased resolution using no pattern recognition. Scale factor on x axis corrects for combined error of three points, see text. Fit is Gaussian plus line.

4.7 Chamber Performance

The expected performance of the COT can be derived from measured performance of the CTC accounting for the COT-specific geometry and Run II operating conditions. We leave a detailed discussion of expected track reconstruction performance until Chap.7. In this section, we describe the detector-level performance issues in terms of the intrinsic position resolution and the resolution for separating two tracks. We measure the first quantity from an actual COT prototype cell and extract the second quantity from arguments based on the COT geometry and expected electronics performance. From these discussions, we can describe the expected COT performance in Run II conditions at a given luminosity based upon our measured CTC performance in Run I conditions.

4.7.1 Position Resolution

The single hit position resolution has been measured in a full-length COT prototype cell by fitting the

width of the residual distribution for hits on a track. To avoid biases due to the specifics in the pattern recognition algorithm, we use the following procedure. For each set of hits on three consecutive wires, we use the inner and outer hits to predict the location of the middle hit. We take the difference between the measured and predicted hit location. For three consecutive wires hit, there are eight combinations of possible hits since each wire in the prototype has two possible drift signs. The result is shown in Figure 4.7. All drift signs are considered: each "triplet" makes $2^3 = 8$ entries, only one of which is correct. So the size and shape of the entries contributing under the peak is as expected.

We find a hit resolution of the prototype cell of 110 μm. CTC prototypes without a magnetic field gave a resolution of ~ 120 μm, while the the CTC for $p\overline{p}$ data at 14 kG gives 180 μm. Based on this, we expect the resolution of the full COT chamber (including calibration uncertainties, wire position errors, etc.) to be 180 μm, the same as that measured by actual data in the CTC.

4.7.2 Two-track Resolution

The ability of the CTC and COT to distinguish between two closely overlapping hits is determined by the pulse shape at the discriminator input. The width of the pulse multiplied by the drift velocity gives the spatial extent of a single hit. For the purposes of this discussion (since prototype front-end electronics is currently under development), we assume that the electronic pulse shaping for the COT has a performance equal to that achieved in SL0-SL2 in the CTC (the outer CTC layers used slower electronics).

The pulse shape can be treated as the convolution of two terms.

- The response to a δ-function of charge arriving at the sense wire. The finite width comes from the avalanche response and electronic shaping.

  The contribution to the pulse width is the same for the CTC and COT ignoring improvements of the COT electronics. In terms of distance, the spatial resolution for two hits to be separated scales with drift velocity, *i.e.* the higher drift velocity of the COT would give an expected worse 2-track resolution.

- Variation in charge collection time. This is a function of track angle and electrostatics of the chamber.

  The COT is intended to operate above the v vs. E saturation point. The CTC operated just below this point which caused an additional spread in the pulse shape especially in the weak field regions between sense and potential wires. For a worst case estimate, we ignore the expected improvement in the COT, then the relative variation of the charge collection time depends on the track angle and path through a cell. In terms of 2-track spatial resolution, we find that this is better for the COT due to shorter drift length and a narrower charge collection region.

The discriminated pulse width has been measured for the CTC and can be characterized by the time over threshold. We use the pulse width for high-p_t tracks (muons in $W \rightarrow \mu\nu$ data) for the COT's response to radial tracks. To this, we add a "geometric width" set by the COT cell size and track angle as given by the angular distribution in minimum bias Monte Carlo (tuned to match CTC data). The simulation is further tuned so that the occupancy reproduces that observed in the CTC. Figure 4.8 shows the "dead space" (pulse width times drift velocity) given by the radial width, T_r, and geometric width, T_g, for typical tracks at low, medium, and high-p_t.

Figure 4.9 shows the resulting average spatial 2-track resolution for the CTC and COT as a function of superlayer. We see that, despite a $\sim 70\%$ increase in drift velocity for the COT for 132 ns operation, the overall dead space per track or 2-track resolution is lower by a factor of 0.87. For 396 ns operation, an improvement in resolution of 0.79 is predicted. The anticipated faster gas planned for 132 ns operation accounts for the difference between the two COT scenarios. The improvement relative to the CTC primarily comes from two sources:

1. We assume fast electronics (like the CTC has on SL0 – SL2) used throughout the COT. This gives a factor of 1.5 reduction in pulse width for radial tracks, partially compensating for the increase in drift velocity.

2. The cell boundaries help "hide" the radial response term (Fig. 4.8) resulting in less variation of charge collection time.

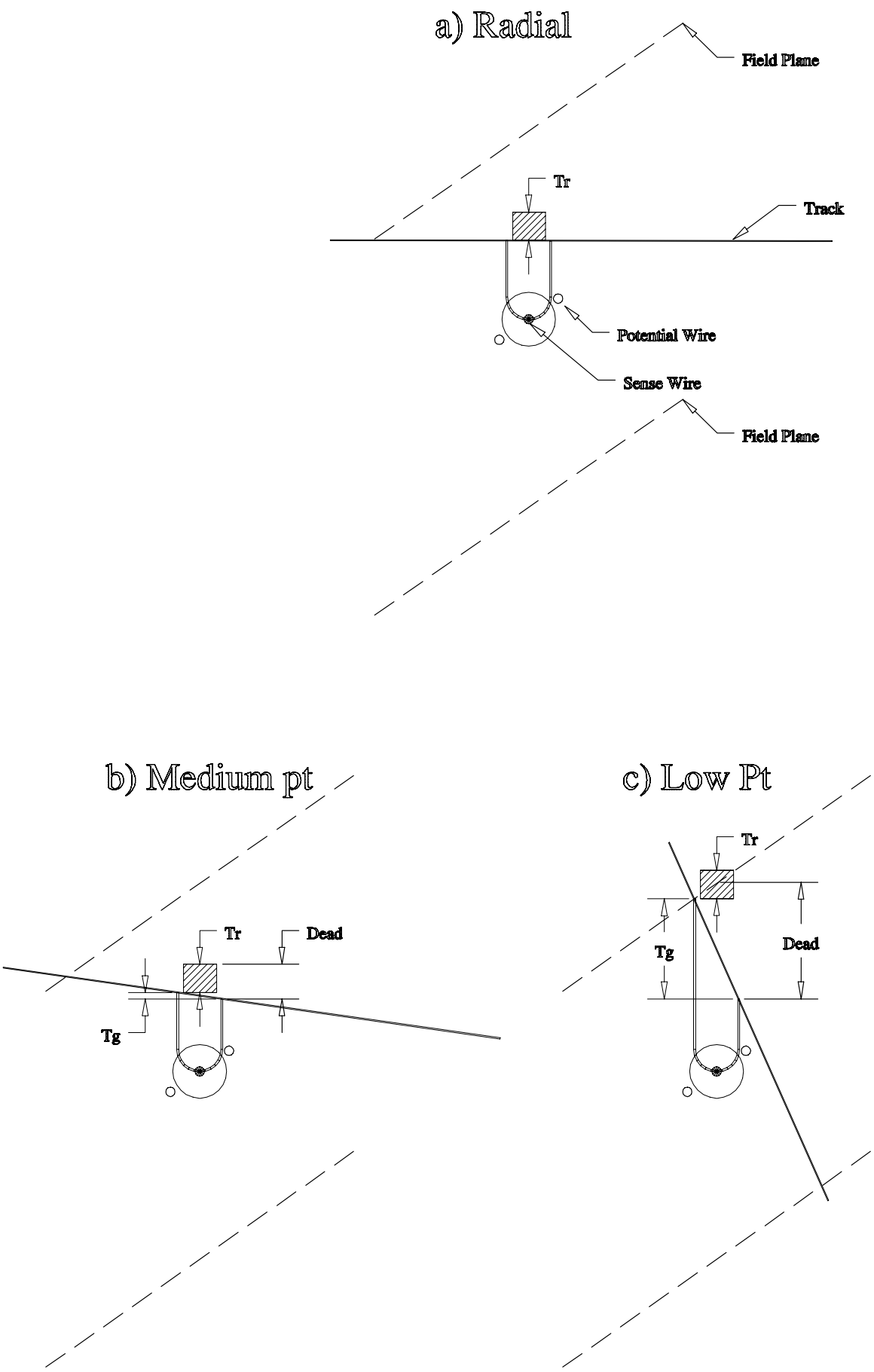

Figure 4.8: Contributions to "dead space" in COT. On the left is a track far from the cell boundaries. The case shown to the right has the effective dead space clipped by the cell boundary.

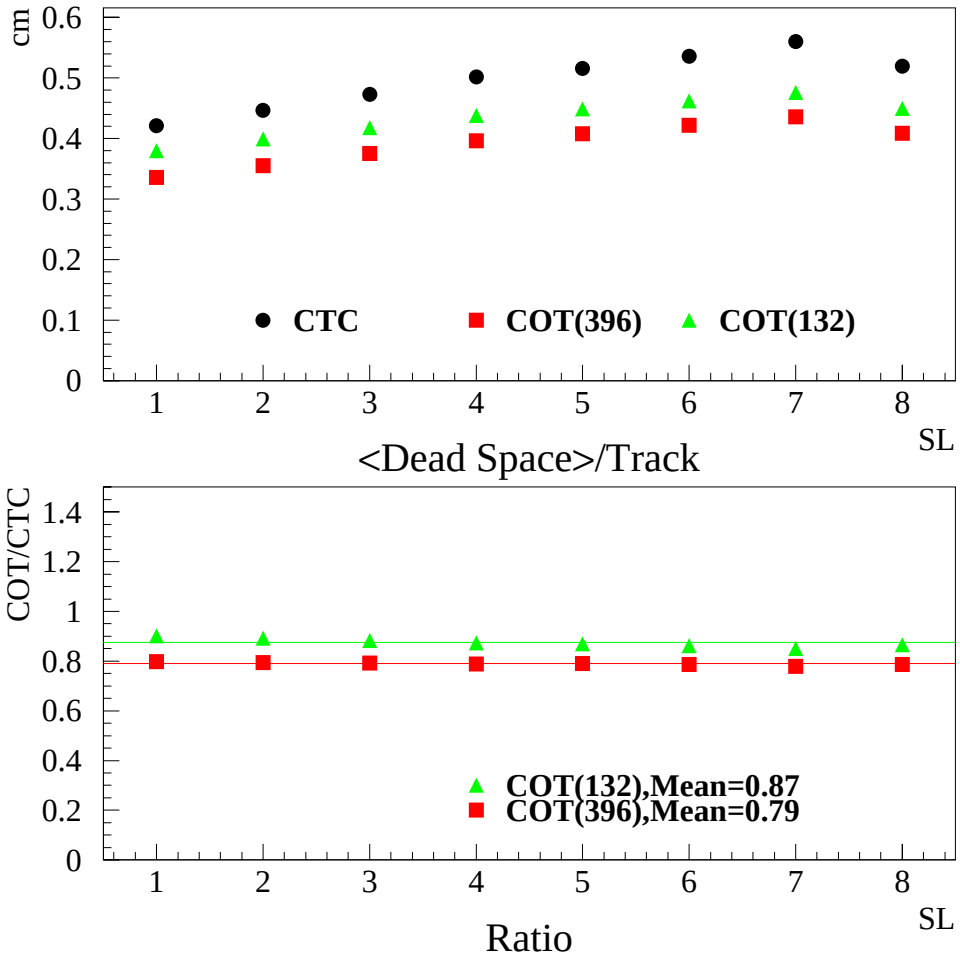

Figure 4.9: Mean pulse width in CTC and COT. Assumes no improvement in pulse shaping. Error on ratio is systematic, based on varying the radial response term 50% (CTC and COT in the same direction).

4.7.3 Luminosity Scaling

In the overview to this chapter we described a scaling rule for anticipating the performance of the COT at Run II luminosities by comparing to the CTC performance at certain Run I luminosities. In the simplest version of the argument, the luminosity scale factor is the ratio of the number of bunches. We now include an additional factor related to the relative 2-track resolution as determined in the previous section and then take a quantitative look at the prediction.

The 2-track resolution of the CTC, as measured by the average dead space per track in minimum bias simulation is approximately 0.45 cm averaged over superlayer. For the COT, we expect a 2-track resolution improvement by a factor of 0.79 for 396 ns operation and 0.87 for 132 ns operation.

The corrected scale factors between the CTC in Run I (6-bunch) and the COT in Run II are then given by the following:

- $\frac{36/6}{0.79} = 7.6$ @396 ns
- $\frac{108/6}{0.87} = 20$ @132 ns

i.e. The COT performance at $7.6 \times 10^{31}\text{cm}^{-2}\text{s}^{-1}$ in 396 ns operation and $2 \times 10^{32}\text{cm}^{-2}\text{s}^{-1}$ in 132 ns operation is expected to be comparable to the CTC performance at $1 \times 10^{31}\text{cm}^{-2}\text{s}^{-1}$ in Run I.

We note that luminosity scale factor still does not account for COT improvements in stereo reconstruction and possible improvements in the front-end electronics. Nevertheless, it gives us a data driven technique for anticipating in a rough way some details of expected COT behavior.

One very interesting benchmark is hit finding efficiency as a function of radius and luminosity. We have used conversion electrons as a control sample to study this in the CTC in Run I. Figure 4.10 shows hit usage as a function of superlayer for conversion electrons measured by the CTC; the abscissa also shows

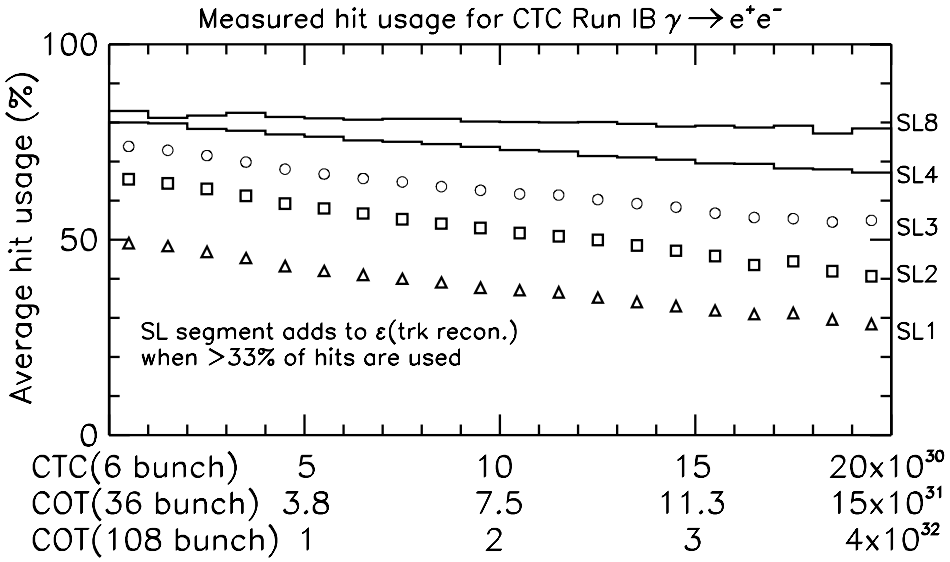

Figure 4.10: CTC conversion electron hit usage vs CTC and expected COT luminosities. The average hit usage for SL4–SL8 fall within the indicated band.

the equivalent luminosity for the COT performance. The exact shape of these curves depends on the data sample being analyzed and the nature of the track-finding and track quality requirements. In the figure, a maximum hit usage of approximately 80% is a consequence of optimizing track reconstruction by including only the best measured hits in a fit. The fraction of hits which are used on average at higher luminosities is smaller because hits are more likely obscured by those from other tracks. The density of overlapping tracks is higher at the smaller radii of the inner superlayers. Note that mid-point of Superlayer 1 for both the CTC and COT are at about the same 47 cm in radius.

A standard offline requirement for accepting a track as being "well-measured" is that the track uses at least 33% of the hits on a minimum of two superlayers. This requirement convoluted with the distribution shown in the figure shows that tracking efficiency for the COT is expected to remain high at the luminosities expected for Run II. However, we see that at luminosities in excess of $1 \times 10^{32}\text{cm}^{-2}\text{s}^{-1}$ the inner superlayers of the COT will be most efficient with 108 bunch operation, and the ability to link to a real silicon segment will be essential.

A detailed simulation study of the COT and complete integrated tracking performance is given in Chapter 7.

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