



**Fermi National Accelerator Laboratory**

**FERMILAB-Pub-96/031-E**

**CDF**

# **Thermal Analysis of the CDF SVX II Silicon Vertex Detector**

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February 1996

Submitted to *Nuclear Instruments and Methods*



Operated by Universities Research Association Inc. under Contract No. DE-AC02-76CHO3000 with the United States Department of Energy

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# Thermal analysis of the CDF SVX II silicon vertex detector

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## Abstract

A simple finite difference technique is used to model conduction and convection in silicon detector components. The solution is found using a simultaneous equation solver which solves in minutes and enables parametric studies to be performed quickly and easily. The modeling technique is compared to output from a finer mesh, solved using ANSYS. The method lends itself to the problem of thermal runaway in silicon detectors, which occurs when internal (temperature dependent) heat generation within the silicon exceeds the heat removal rate by conduction and convection, the effect of which increases with radiation dose. Comparisons between the computer simulation and some physical models is provided, as well as a comparison to analytical techniques. This modeling technique is then applied to the CDF SVX II silicon detector to determine the temperature profile of the silicon during operating conditions.

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## 1. Introduction

A second generation silicon strip vertex detector is being designed by the CDF group at Fermilab. The SVX II detector consists of 5 layers of silicon, each of which is composed of twelve 30° wedges of silicon. A ladder is defined by four crystals of silicon which is actively read out on each end. Two crystals comprise an electrical unit and are wirebonded at the ladder quarter points. A barrel is defined as the length of the ladder and is made up of twelve wedges and five layers of silicon. There are 3 barrels in the full SVX II design.

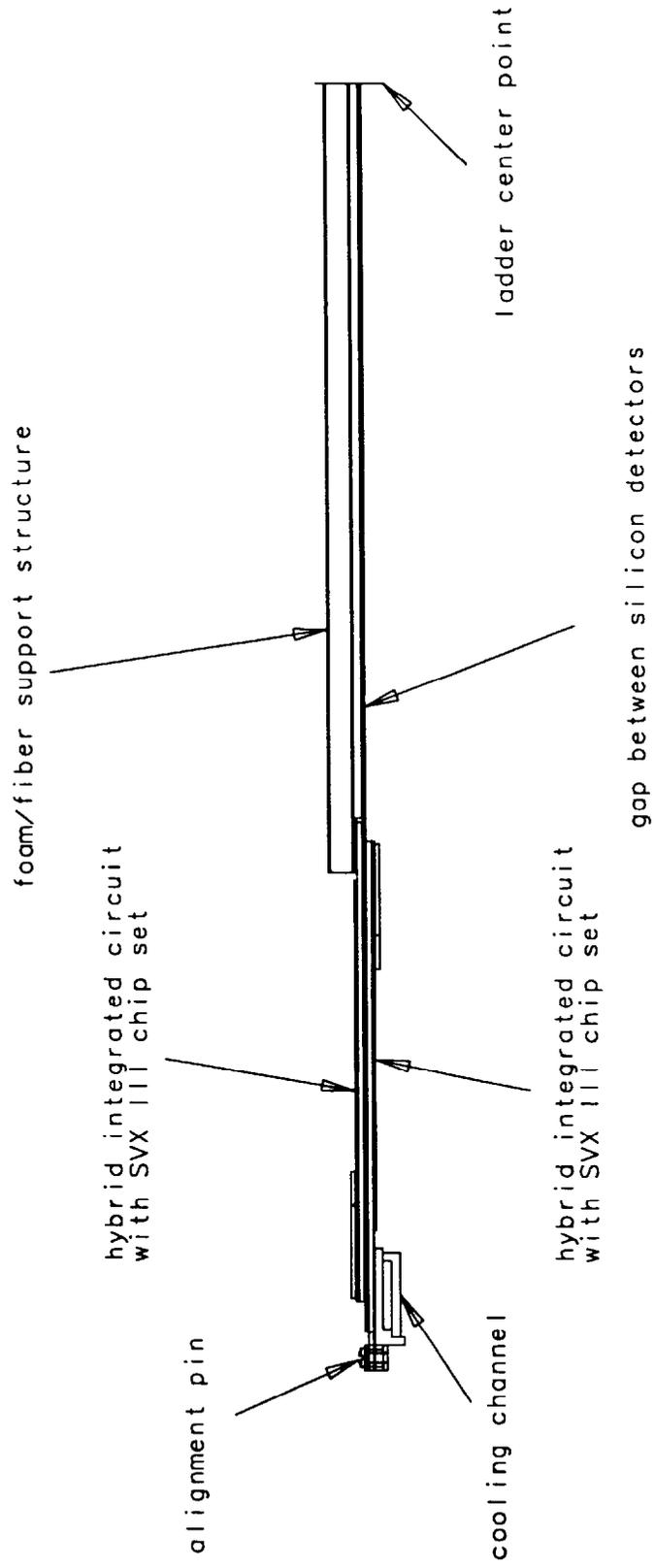
Part of the design effort is in the area of thermal management. To begin, constraints must be established in order to set design goals. The constraints imposed will ultimately dictate the coolant temperature at the inlet to the detector, flow rate of coolant, and the thickness of the substrates which conduct the thermal load from the power generating components to the bulkhead.

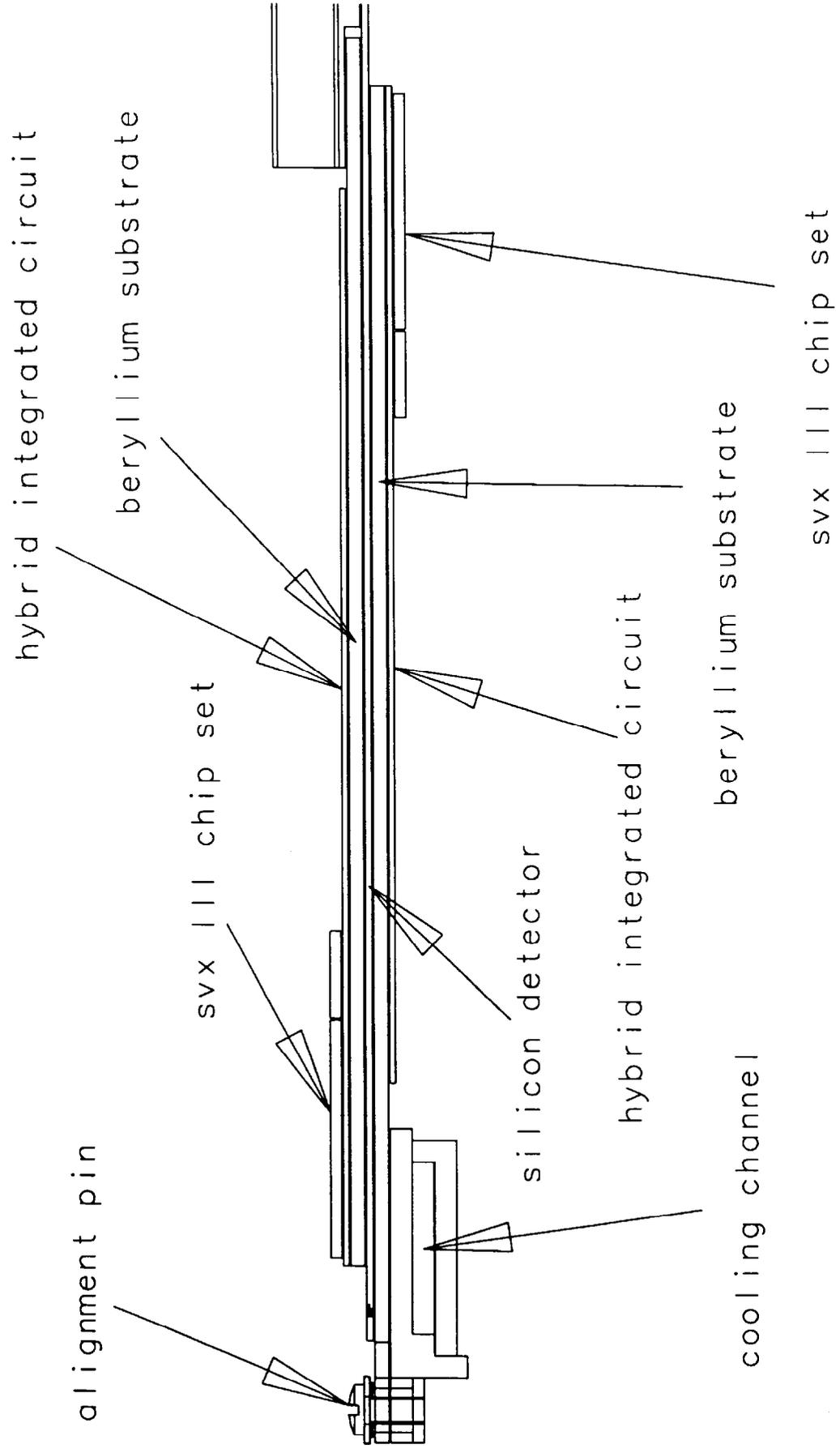
It has been decided within the CDF silicon group that the operating temperature of the silicon should not exceed 10°C at the beginning of the run. Secondly, the silicon detectors must not experience thermal runaway after 1 Mrad of exposure, expected at the end of the run at the innermost layer of silicon.

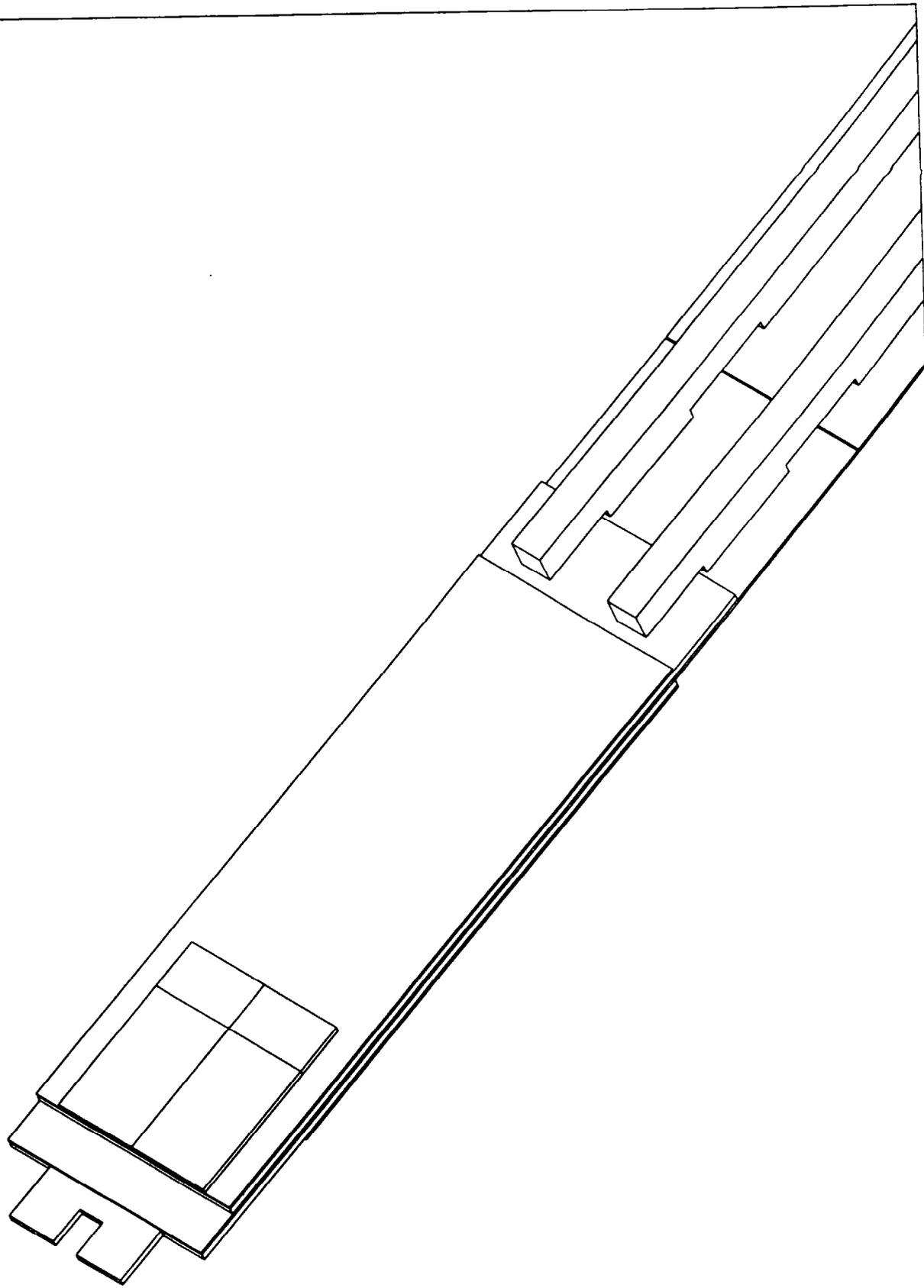
Conduction and convection are simulated in order to understand the effect of varying the thickness of the cooling substrate on the silicon temperature profile. Radiation heat transfer is disregarded in all analyses.

## 2. Design discussion and heat loads

The silicon detectors are built into ladders, which are four crystals in length. Each ladder is separated into two electrical lengths of two crystals each. Figure 1 shows a half-ladder drawing, and Figure 2 shows a close-up of the conduction portion of the ladder. Figure 3 shows a perspective view of a quarter of the ladder. The cooling channel (otherwise







known as the bulkhead) acts also as a support structure and has features machined in it which precisely locate the ladder in three-space. It also serves to convectively cool the warmer portions of the ladder, as will be discussed later.

It is expected that the average gas temperature in the detector volume will be substantially lower than the surrounding gas temperature. For this reason, an insulating barrier has been assumed to occupy the radial region between the outer silicon detector and the environment immediately outside.

The silicon has readout strips on both top and bottom, providing track information in both phi and z coordinates in a cylindrical system. Thin film copper on kapton hybrid integrated circuits are mounted on beryllium cooling substrates on both the top and bottom of the ladder. The bottom side beryllium substrate has an alignment slot in the end which is used to precisely locate the silicon to the mounting pin. The top side beryllium is extended beyond the region of the hybrid circuit, serving both as a structural component for the support piece, and as additional conduction path for the SVX III chip on the opposite side of the ladder.

SVX III chips (front end analog and back end digital) are mounted on the ends of the hybrids, and read out individual strips of the silicon detector. The SVX III chips are the primary source of heating within a ladder.

Cables extend beyond the end of the ladder, which read out the information from the hybrid to the outside world. Heat generated within the cables is modeled as a convective heat load.

The primary heat flow path for the SVX III chips is via conduction through the beryllium substrates and the silicon detector itself to the cooling channel. However, some of this energy is convected to the surrounding gas environment within the detector volume. The average gas temperature is affected by all convective heat loads. Heat is dissipated from the hybrid components, the cables, and the chips. In addition, there is heat transfer through the outer insulation to the cooler gas volume. Some of the heat load is carried away by the gas flow within the detector environment. The primary convective heat sink is to the cold support structure.

The coolant temperature, not yet specified, is assumed to be adequately low as to produce a 0°C ledge temperature to which the ladders are mounted.

### **3. Calculation Method**

Typically a problem of this nature would be simulated using ANSYS or some other pre-packaged software. However, given the nature of this problem the cooling calculations are performed using a simultaneous equation solver, EES [1], on a Macintosh computer. These problems set up as such result in a set of ~600 equations and unknowns which solve in a matter of minutes.

The temperatures within the conduction region of the ladder (in the region of beryllium) are calculated by writing a series of finite difference equations and solving them as a DC electrical circuit. An energy balance is performed on each node of the mesh based on the calculated thermal resistance between the current node and the neighboring nodes. Heat input to the node is added with an additional term in the energy balance. Convection can be added if the node has a convective boundary, using standard convection equations and an assumed film coefficient, as determined by Ratzmann [6]. The node may also have

internal power generation, such as from the chips or from leakage current within the silicon detector.

In the convection region of the ladder (beyond the beryllium cooling substrates), conduction between elements is considered along the silicon, but the effect of convection is much more substantial.

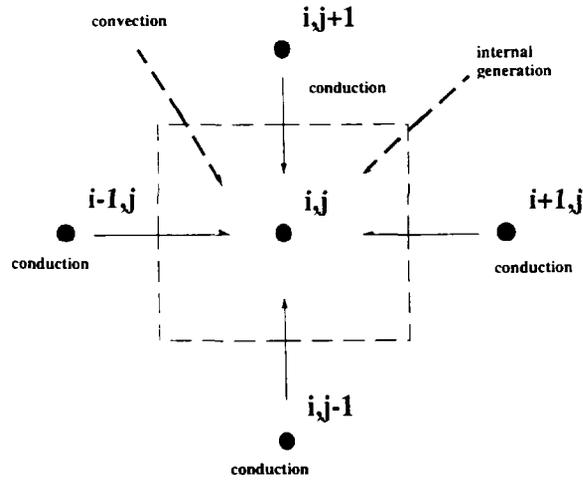


Figure 4

By writing all of the energy balance terms in a simultaneous solver, the average inner temperature of the gas can be directly calculated. The convection equations are written based on an unknown average temperature and the average temperature of the gas is then calculated by summing all the convection terms and setting to zero, the point achieved when thermal equilibrium is reached. Additional convective loads may be directly added, if known, as non-temperature dependent values. Following is a schematic with all the convective inputs:

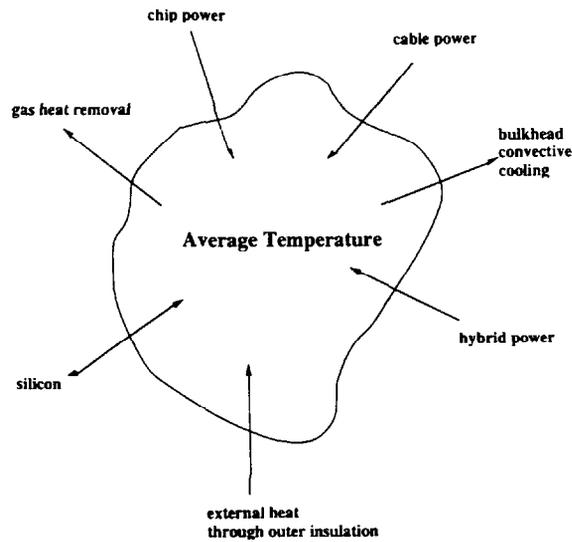
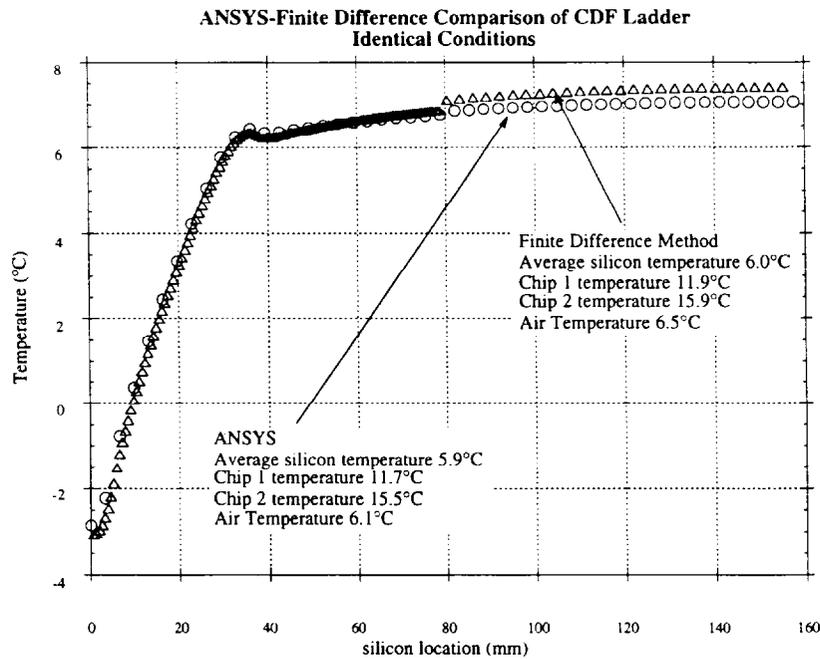


Figure 5

#### 4. Model verification

EES [1] has limitations to the number of equations which can be solved simultaneously. This limits the size of the element for a problem of this nature. To determine if the element size can be adequately small to correctly reflect the conduction portion of the problem, a test problem was solved using this method and comparing the output that was obtained using ANSYS, using much smaller elements.

The temperature distribution within the silicon was calculated assuming a geometry similar to the current ladder design. Without going into details of this model, the two methods predicted a nearly identical temperature distribution in the silicon. They also predict very similar chip and air temperatures as shown on the plot. The difference between the two was in the region of convection and was not related to element size, rather the conditions of convection.



**Figure 6**

#### 5. Radiation damage and thermal runaway

Frautschi [2] describes a method to calculate the leakage current in a silicon detector as a function of the radiation damage. Using data obtained from the first silicon detector (SVX) at CDF, a method was described extrapolating from the SVX dose to the dose of SVX II over its lifetime, 2000 pb<sup>-1</sup>. Effectively, the leakage current can be calculated with the equation:

$$I_{leak} = I_0 + \alpha \times \phi \times V_{strip} \quad \text{Equation 1}$$

where  $I_0$  is the leakage current with no radiation damage, assumed zero for these calculations.  $\alpha$  is 3E-8 nA/cm, the damage coefficient at 20°C,  $\phi$  is the dose rate

received in units of MIPs/cm<sup>2</sup>, and  $V_{strip}$  is the volume of a strip in the silicon detector for 2 crystals.

The dose rate,  $\phi$ , is 3.5E-4 Mrad/pb<sup>-1</sup>. This number is derived from CDF experience and corresponds to a radius of 2.99 cm. To correct for the different radii of SVX II Frautschi scales by  $r^{-1.7}$ . Applying this method and extrapolating out to 2000 pb<sup>-1</sup> the calculated leakage current density is 3.36E-7 A/mm<sup>2</sup> at 20°C for a detector with a pitch of 0.006 cm (60 microns). This translates, using 1 Mrad  $\equiv$  3.73E13/cm<sup>2</sup> of minimum ionizing particles in silicon [2], in a predicted fluence of 3.7E13/cm<sup>2</sup>/2000 pb<sup>-1</sup>, similar to that predicted by Matthews, et. al. [5] using the same method. Matthews, et. al. [5] determined this interpretation to be the more conservative of the two methods presented in that paper.

Frautschi [2] and others have provided an equation to correct for the temperature dependence of the leakage current:

$$I_{leak}(T_2) = I_{leak}(T_1) \left\{ \frac{T_2}{T_1} \right\}^2 \exp \left\{ \frac{E (T_2 - T_1)}{2k T_2 T_1} \right\} \quad \text{Equation 2}$$

$E = 1.2$  eV and  $k$  is the Boltzmann factor 8.617E-5 eV/K. The predicted leakage current density using the above method is 5.11E-8 A/mm<sup>2</sup> at 0°C for the inner layer of the SVX II.

This equation is well approximated if large deviations from 0°C do not occur, using equation 3 below provided by Miller [8], and others. In this equation  $q_0$  is the heat flux at a reference temperature,  $\alpha$  is a constant chosen to best fit with Equation 2 over the desired range of temperatures, and  $T$  is in °C.

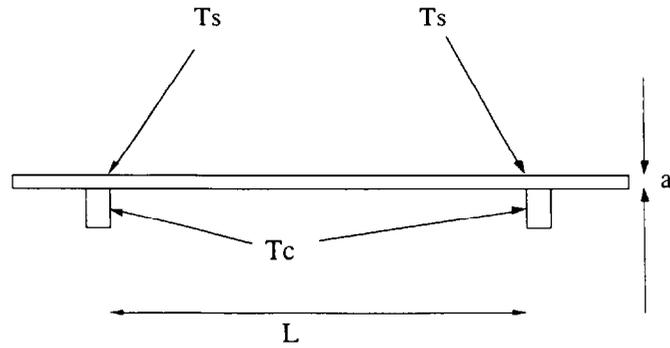
$$q = q_0 * \exp(\alpha * T) \quad \text{Equation 3}$$

Thermal runaway is modeled assuming the worst case scenario for power generation in the detector. 150 V bias will be assumed for all thermal runaway models. Matthews, et. al. [5], predict ~150 V bias as the upper limit operating voltage after 2000 pb<sup>-1</sup> for the SVX II inner layer, using the more conservative model in that note.

## 6. Comparison to Analytical Solutions

Hanlon and Ziock [3] determined a number of analytical expressions which can be applied to the problem of radiation damage induced leakage current in a silicon detector. They describe a variety of scenarios in which analytical methods are used to determine the point at which thermal runaway occurs in a detector. Two of their solutions are modeled here as a means of cross-checking the modeling technique with the expected analytical results.

The first solution compares to the Special Case: Silicon Temperature  $T_s = 0$ , no convection, as described in [3] in pages 4-6. The detector module which is modeled is of the following configuration:

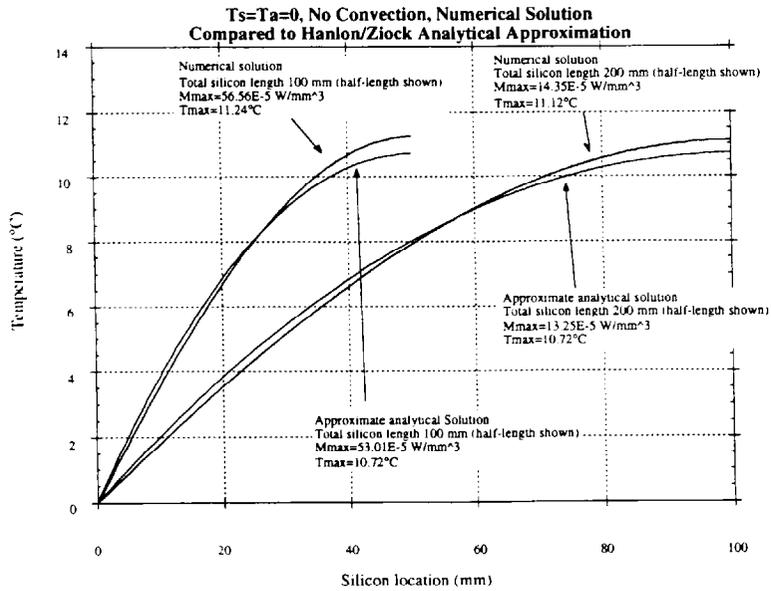


**Figure 7**

The silicon is mounted on cooling channels which have a temperature  $T_c$ . The silicon at that point, due to gradients in adhesives, silicon, etc... is  $T_s$ . The distance between cooling tubes is  $L$ . The silicon thickness is  $a$ , and the width of the silicon, not shown, is  $b$ .

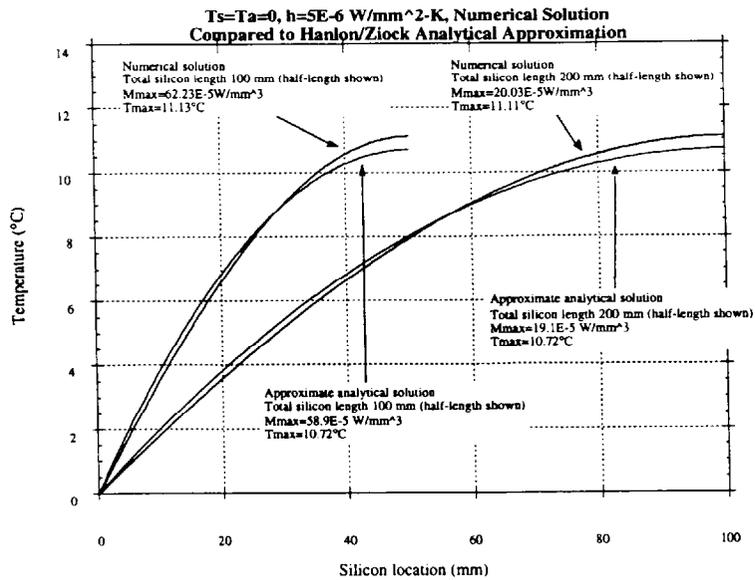
Using the same assumptions as described in the paper, the value  $M_{max}$  was obtained numerically and plotted for ladder lengths of 100 and 200 mm (plotted are half-length ladders). Equation 3 above is used in the simulation, with  $\alpha$  as 1/9.532, the same as was used in [3]. Program variables are input for the conditions as described, and the temperature distribution in the silicon is calculated for equilibrium conditions. The power generated in the silicon is calculated per node and is temperature dependent.

In Figure 8, for the 100 mm ladder, the value of  $M_{max}$  above which caused thermal runaway was 56.56E-5 W/mm<sup>3</sup>. This compares to 53.01E-5 W/mm<sup>3</sup> as determined for this set of conditions and geometry by the analytical model. Varying the element size to other than the 0.25 mm used did not substantially affect the predicted  $M_{max}$  value at which thermal runaway occurred. Similar results, as shown in the plot, are seen for the 200 mm silicon length.



**Figure 8**

The second solution compares to the Special Case: Silicon Temperature  $T_s = 0$ , with convection, as described in [3] in pages 9-10. The detector module which is modeled the same as shown in Figure 9.



**Figure 9**

The numerical method results are quite close to the analytical, differing by ~5%. The difference in the two sets of results may be attributed to the fact that the analytical solution is an approximation to the true solution, as seen in the overlaid parabola of the analytical approximation.

The numerical method employed in this section will be used later in order to simulate the more complex conditions in the CDF ladder designs.

## 7. KEK Silicon Measurements and Modeling

The CDF/ATLAS Silicon group in Japan observed thermal runaway in a silicon detector by uniformly irradiating a detector with  $4.2E13$  protons/cm<sup>2</sup> [4]. The measurements were performed by clamping the detector on the end. It was cooled by running a tube along the clamped region and running a coolant fluid through it. The exposed region of silicon was 66.8 mm in length. Thermocouples were mounted on the surface in the regions shown. The setup was placed in an oven and taken down to a vacuum of ~2-3 torr, thus the ambient temperature was controlled as well. The bias voltage on the silicon was varied incrementally under a variety of coolant and environmental temperatures. The temperatures were recorded, as well as the total leakage current through the bulk silicon.

In the measurements simulated, the coolant temperature was maintained to be 10°C cooler than the ambient temperatures, although measurements were performed.

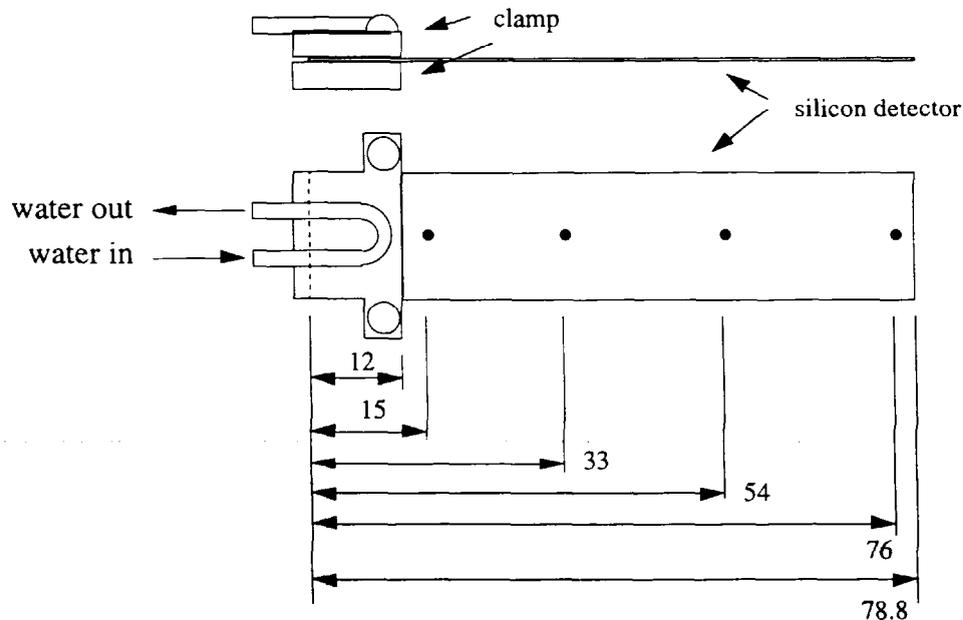
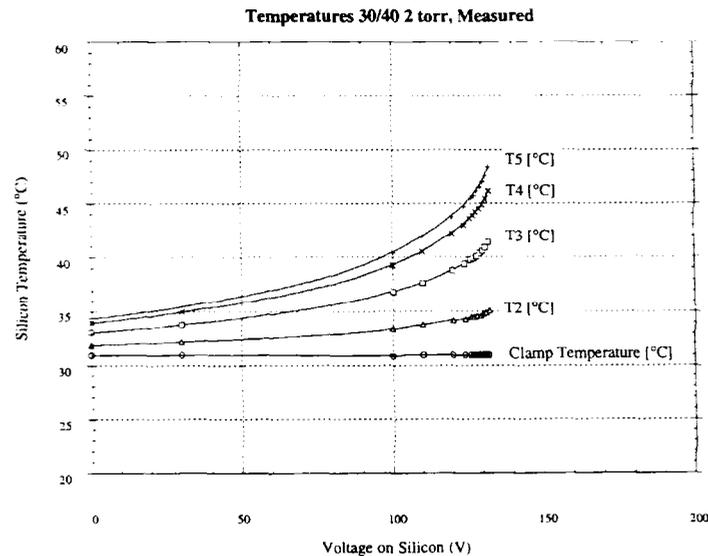


Figure 10

The test setup was simulated using the finite difference method described above. As reported by Kohriki, et. al. [4] there are three parameters which must be derived in order to simulate the test setup:

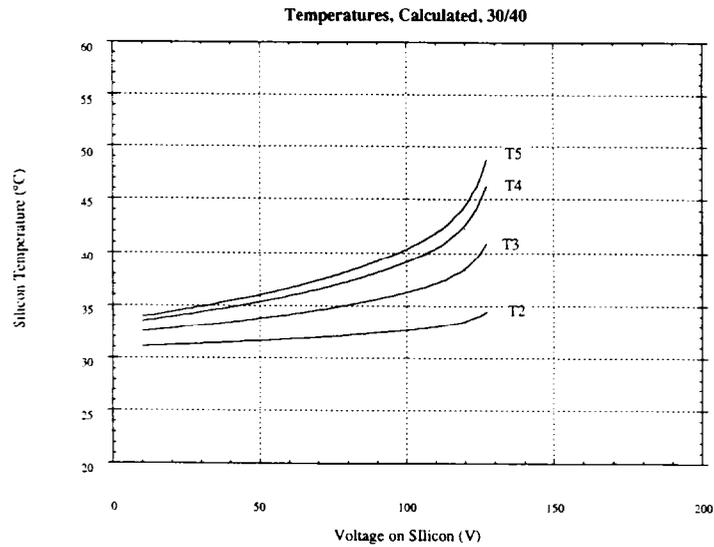
1. thermal resistance between the silicon detector and the coolant
2. convective film coefficient over the silicon
3. leakage current density at 0°C

These parameters were varied in order to reproduce the temperature profiles above. The thermal resistance between the silicon detector and the coolant was determined by comparing temperature profiles for the 30/40°C 3 torr case:



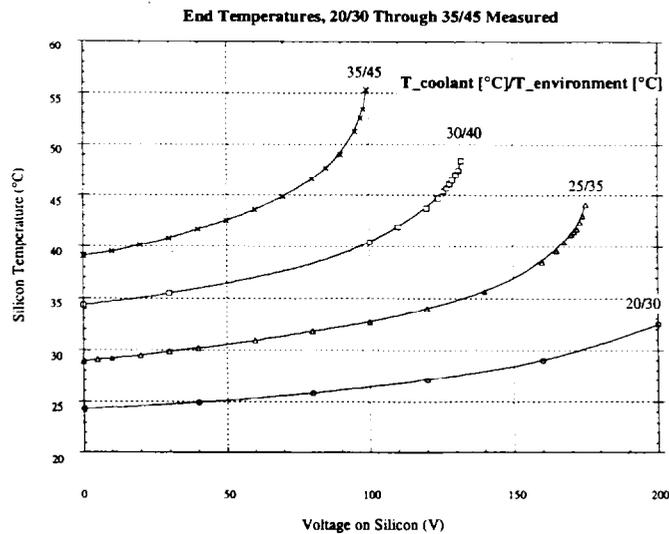
**Figure 11**

A 1 mm width section of clamped silicon was simulated. The thermal resistance between the silicon and the cooling channel was determined iteratively by successive solutions to be 190°C/W. Convection is used to model both convective and radiative heat transfer for the test model. The film coefficient was also varied in order to best match the data in this set of measurements. It was found to be 4.0 W/m<sup>2</sup>-k, in good agreement with that found in [4].

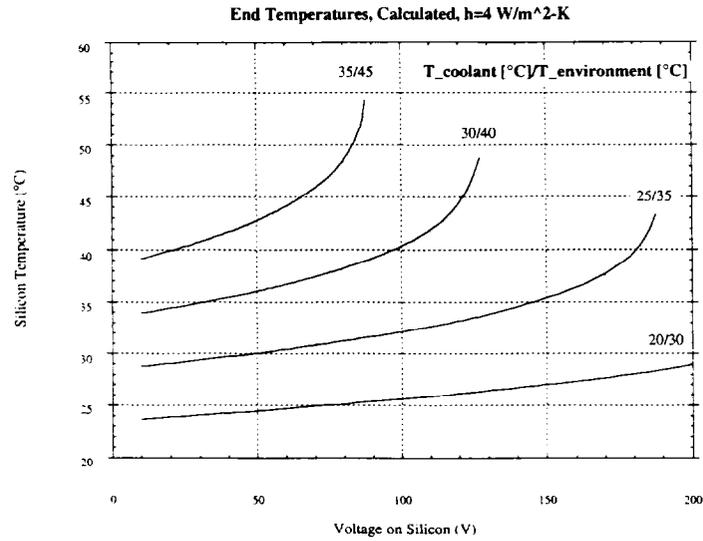


**Figure 12**

With the simulation parameters set, the model was run for the other measured cases of 20/30 through 35/45 °C coolant/ambient temperatures. The measured temperatures at the end of the silicon, plotted below in Figures 13 and 14, compare well with the temperatures predicted in the simulation.

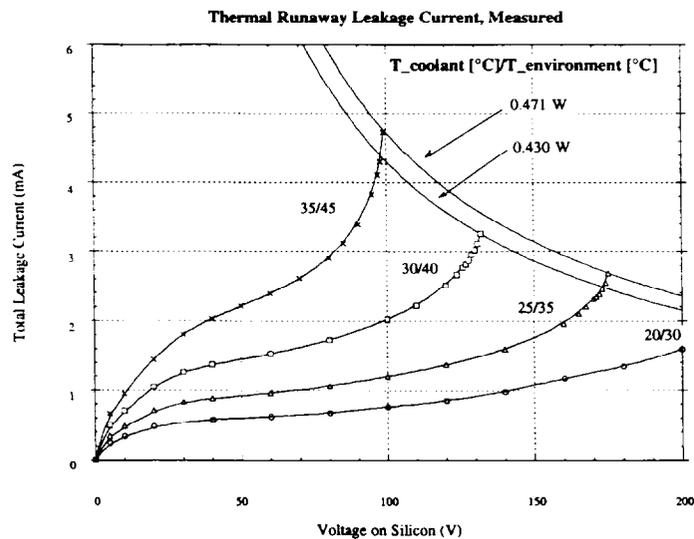


**Figure 13**



**Figure 14**

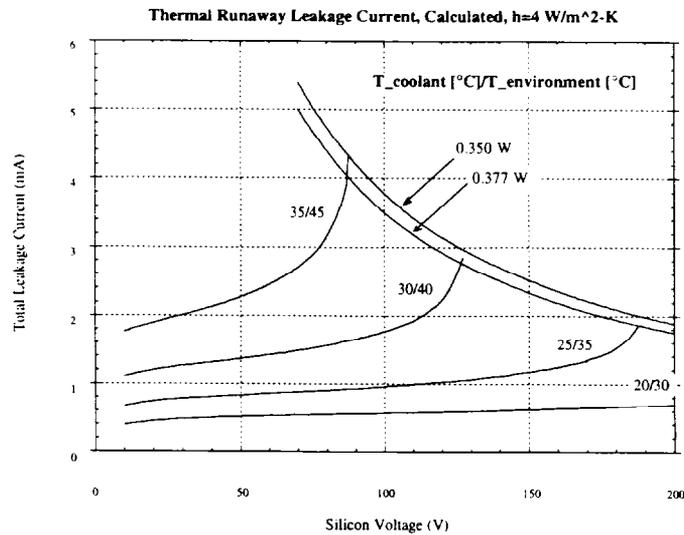
The leakage current of the detector was measured in the test piece and shown in Figure 15. It is calculated in the simulation by summing the currents within all the finite difference elements.



**Figure 15**

The measured leakage currents are compared to those calculated in the simulation, Figure 16. An interesting parameter is the power generated in the silicon at the runaway point. Within the bounds shown, the power generated in the silicon remained a constant for the measurements performed. If the ambient temperature is kept at a constant 10°C warmer

than the coolant, then the power curves would effectively predict other points of runaway for differing bias voltages.



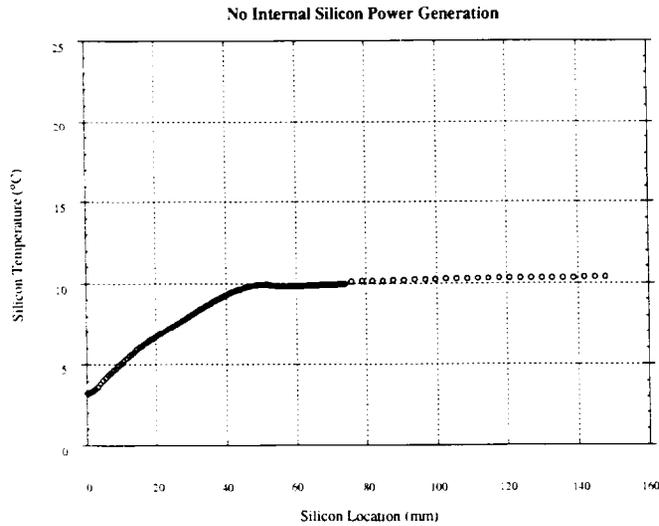
**Figure 16**

The simulation well predicts the runaway leakage current and the temperature at runaway, although the power dissipation in the silicon and the bias voltage varied somewhat from those values measured.

## 8. CDF Silicon Detector Results

The CDF silicon detector thermal analysis is carried out using the method described above. To begin, the baseline solution is determined for the situation where there is no significant leakage current in the silicon. This corresponds to the beginning of the run and satisfies the first of the two design goals described at the beginning; the silicon should not exceed 10°C at the beginning of the run, prior to any radiation damage.

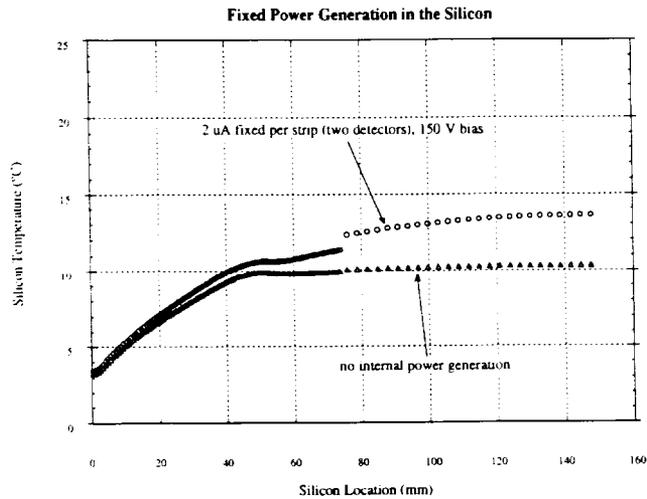
Convective loads, SVX III chip power, hybrid component power, and other assumptions are based on the best understanding of these values [6] and [7]. The hybrid substrate (sometimes known as a "heat spreader") thicknesses are chosen in order to reduce the gradient between the cold end and the end of the beryllium substrates, reducing the end of the conduction region to an acceptable temperature. The resultant gas temperature determines the temperature of the silicon in the convection region.



**Figure 17**

Next, radiation damage induced leakage currents must be considered. In order to determine the point at which thermal runaway occurs, the simulation is split into two parts; conduction and convection. The temperature profile in the conduction region of the ladder, ~0-55 mm, remains largely unchanged for widely varying leakage currents in the silicon. 2 uA and 150 V applied bias represent an upper limit on what sort of power generation can be expected at the end of the run with ~1 Mrad radiation exposure [2] and [5].

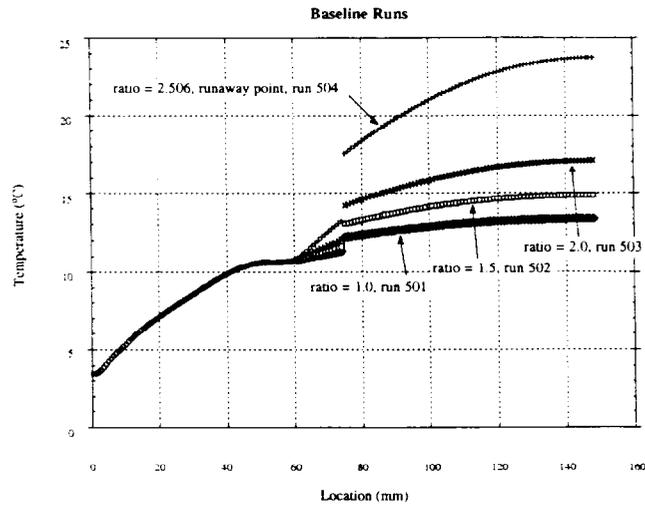
The majority of the complexity of the thermal modeling occurs in the conduction region of the ladder. For this reason the two are decoupled by assuming, for the sake of the thermal runaway analysis, that the temperature profile within the conduction region remains unchanged for all subsequent analyses. This reduces the convection modeling to a much simpler solution by enabling all the convective heat sources to be at constant heat temperatures.



**Figure 18**

With the temperature profile in the conduction region now assumed constant, the temperature dependence of the leakage current is considered by adding the necessary complexity to the convection region of the program. A separate, simpler program is written which models the convection region only. Being simpler, the node size can be reduced and the more accurate Equation 2 can be used to accurately portray the radiation damage effect. Exposed surface temperatures of the bulkhead and ladder are assumed constant for the convection portion of this solution, using the temperatures obtained for the fixed 2uA/150 V bias solution.

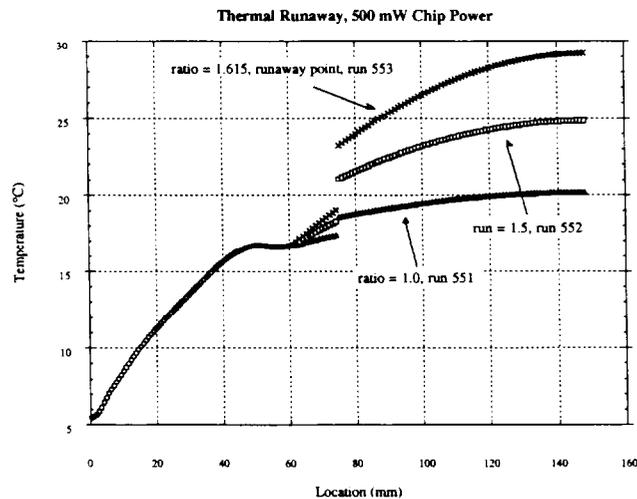
The baseline solution occurs at "ratio = 1.0". This solution represents all of the nominal inputs regarding radiation damage and the temperature profile is well matched to the constant power assumption as seen in Figure 18 above. The damage coefficient, integrated luminosity, and applied bias voltage are all directly proportional to the value ratio, enabling simple extrapolation to other conditions. Reporting the value ratio as such in some ways represents the level of safety that the ladders see against thermal runaway. A value of 2.506 suggests that the damage coefficient, for instance, could be substantially higher and thermal runaway would not occur.



**Figure 19**

One of the more important parameters to assume is the SVX III chip power. Nominally assumed to be 300 mW per die, errors on the level of one or two hundred mW would substantially increase the temperature profile of the silicon during operation. This would increase the silicon temperature at the beginning of the run, and would require a much colder fluid at the tube inlets to cool the silicon to the design temperature of 10°C.

Assuming the support ledge temperature to be 0°C as in Figure 19, the simulations were run to determine the temperature profile of the silicon and the exposed temperatures with a chip power of 0.500 W. Next, the convection portion of the ladder was simulated assuming the conduction portion to be fixed. As before, the second design requirement; the silicon detectors must not experience thermal runaway after 1 Mrad of exposure, is satisfied and a level of safety is seen in the value of ratio = 1.615.



## Figure 20

### 9. Conclusions

Application of a finite difference technique to the solution of conduction and convection heat transfer is not a new idea. However, finite difference equations are easily written into a simultaneous equation solver, enabling the direct calculation of the average gas temperature. The equation solver is especially good at solving heat transfer problems such as these where the power dissipation is temperature dependent.

Results are compared to ANSYS finite element modeling and to analytical solutions. This modeling technique is used to reproduce thermal runaway measurements based on tests performed at KEK, and results are compared to analytical solutions.

The CDF ladder is modeled in order to meet the design goals set by the CDF Silicon Detector Design group; the silicon is kept to 10°C maximum at the beginning of the run and thermal runaway does not occur in the ladders during the expected lifetime of the detector.

\*\*Include Thanks to the KEK group and acknowledgement to the DOE.\*\*

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- [2] Frautschi, M. A., Radiation Damage Issues for the SVX II Detector, 27 January 1994, CDF note 2368.
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- [6] Ratzmann, P., Ladder Thermal Analysis for CDF with SVX III Chips, June 5, 1995, CDF Note Number 3507.
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