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The CDF Silicon Vertex Detector SVX and Its Upgrades

Sally Seidel

Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510

New Mexico Center for Particle Physics
University of New Mexico
Albuquerque, New Mexico 87131

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Sally Seidel
The New Mexico Center for Particle Physics
The University of New Mexico
Albuquerque, New Mexico, USA 87131

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Abstract

The three generations of CDF silicon vertex detectors, SVX, SVX′, and SVX II, are described. SVX, which operated during Tevatron run Ia, achieved 10.6 μm resolution in $r-\phi$. SVX′ is a radiation-hard device for run Ib with a similar but improved mechanical design and improved signal/noise. SVX II, which will be installed for run II, will track in three dimensions with radiation tolerance and electronics appropriate to a Main Injector environment.

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1 INTRODUCTION

The CDF Collaboration's [1] physics goals for the 1990's mandate the addition of a vertex detector capable both of excellent tracking and of separating secondary from primary vertices with high precision. The first such detector, the SVX (for Silicon VerteX detector) [2] was installed in 1992 and operated during Tevatron run Ia. It was replaced in 1993 by the SVX′, a similar device able to withstand significantly more radiation. Planned upgrades to the collider bunch structure, as well as to the luminosity, necessitate replacing the SVX′ with a third detector, the SVX II, at the beginning of run II. These three silicon vertex detectors are described below.

2 SVX

Figure 1 shows the SVX. The SVX consisted of two 12-sided, electrically independent barrels and had an active length of 51 centimeters. The barrels were inserted into CDF symmetrically about the interaction point and coaxially with the beams. Each barrel was made of 4 layers of single-sided DC-coupled silicon microstrip sensors, their strips oriented parallel to the barrel axis. The 8.5 cm sensors were supported in groups of three and wirebonded end to end to form the primary mechanical and electrical units of the device, known as "ladders." A layer had 12 ladders, each of which subtended 30° in azimuth. The SVX had 46080 channels and was constructed from 0.7 m^2 of silicon. Its approximately 8 cm outer radius allowed it to fit snugly inside the CDF vertex time projection chamber, or VTX. SVX had a geometrical acceptance of approximately 60%.

Figure 2 is a diagram of an SVX ladder. Three aligned microstrip sensors were supported by a Rohacell and carbon fiber structure for a total active length of 25.5 cm per channel. Their strip pitches were 60 μm (for the inner three layers) or 55 μm (for the outermost layer). The sensor nearest to the detector end was wirebonded to an off-board custom thick-film hybrid known as an "ear." [3] The ear carried 2, 3, 4, or 6 SVX-D chips (innermost to outermost layer, respectively) and had a reference hole for use during alignment. A copper-Kapton cable known as a "pigtail" connected the ear to the rest of the data acquisition system. An inactive, or "dummy" ear,

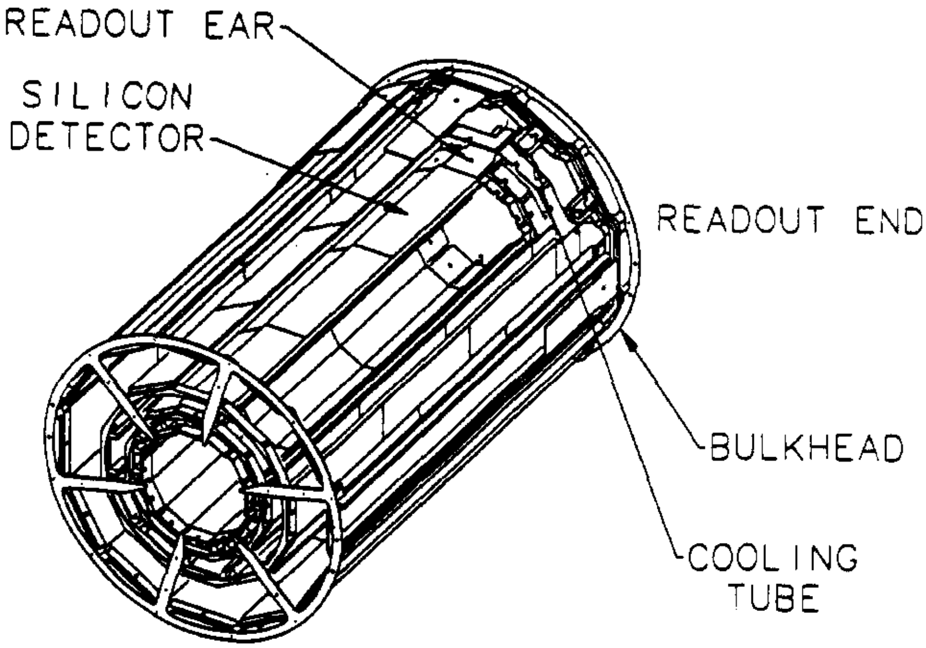

Figure 1: Isometric view of one barrel of the SVX detector.

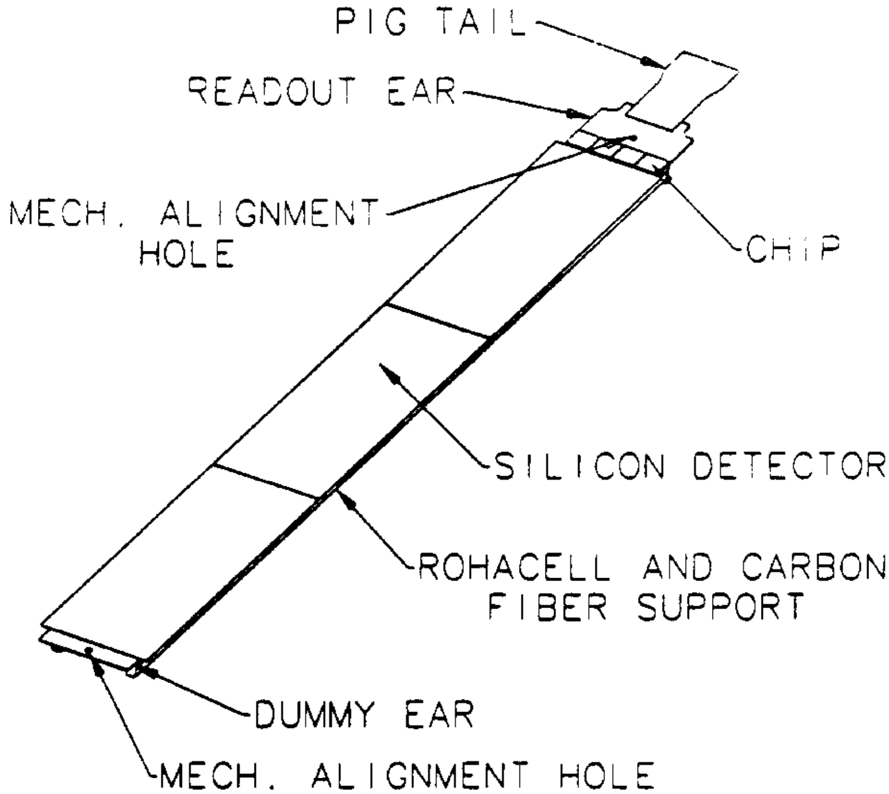

Figure 2: SVX Layer 2 ladder.

bearing only an alignment hole. adjoined the sensor at the opposite end of the ladder.

The radii of the 4 layers were 20.05 mm, 42.56 mm, 56.87 mm, and 78.66 mm. The inner layer was positioned as close as possible to the beampipe (which has an outer diameter of 1.5″) for the best possible impact parameter measurement. The outer layer was positioned as close as possible to the outer tracking for good matching between systems. The middle two layers provided redundancy as protection against inefficiency of a channel in this high track density, high radiation environment. Each ladder was rotated about its longest axis to an angle 3° from the perpendicular to the radius in order to improve overlap between adjacent ladders. The SVX did not operate as a stand-alone tracker, but used tracks pointing toward it from the main outer tracker, the Central Tracking Chamber or CTC.

The single-sided, DC-coupled microstrip sensors were produced by Micron Semiconductor, Ltd. Their typical leakage current per channel was less than 2 nA, and fewer than 1% of the channels in the SVX had leakage currents above 75 nA. Layers 0, 1, 2, and 3 had (2, 3, 4, and 6)$\times$128 channels, respectively. The measured depletion voltage for these sensors was 30 ± 15 V. The capacitance per channel seen by the preamplifers was approximately 30 pF.

The sequence of read-out operations began with the SVX integrating the signal from its hit channels. If a Level 1 trigger was subsequently received, a second, off beam, integration was performed to set the thresholds. The two integrated values were then compared for each channel, and a latch was set if Integration 2 produced a value over threshold. A priority encoding circuit read out the analog pulse height and digital address of the latched channels (and, optionally, their nearest neighbors) and presented that information to a 7-bit bus.

The primary data acquisition unit of the SVX was a "wedge," which consisted of 4 ladders, one from each of the layers, at a common azimuthal angle with respect to the beam axis. The four ears in each wedge were daisy-chained to a unit known as the "portcard," which was connected serially to a "digitizer." Groups of six digitizers were connected to a "sequencer." There were four sequencers for SVX. The tasks of these units are described in detail below.

The ear boards were fabricated from aluminum nitride for good thermal conductivity and a coefficient of expansion that is well-matched to the silicon. The ear distributed power, ground, and control signals to its chips, set the current in the chip integrator, and filtered the bias line.

The SVX chips [4] are custom CMOS devices fabricated by Hewlett-Packard with 3 μm feature size. Each provides charge integration, sample and hold, voltage amplification, and comparator/latch functions for 128 channels. They have 15 mV/fC gain, dynamic range from -25 fC to 60 fC, a 1 μs integration time, and a 1.7 μs reset time (to be compared with the 3.5 μs time between beam crossings during run I). The equivalent noise charge per channel is 2100 electrons in quadruple sampling mode for about 30 pf input capacitance. They dissipate 1.3 mW per channel.

The portcard was a thick-film hybrid mounted to the bulkhead to provide power distribution, regulation, and filtering to the ears. Portcards also inject charge for calibration and threshold setting and buffer and drive signals to the external data acquisition system.

The digitizer formatted the chip identification code and digitized the analog data. In addition to controlling the chips, the sequencer, a FASTBUS unit, generated the read-out clock and provided synchronization to the Tevatron.

This read-out configuration produced fewer than 6kB per SVX event. As only two threshold values could be stored per portcard (i.e., per wedge), the chips on each hybrid were selected for similar DC analog levels while the sensors on their ladder were matched in depletion voltage.

The mechanical design was optimized for low power dissipation, low noise, and low mass. A track at normal incidence encountered 3% of a radiation length. The SVX was cooled by under-pressured water at its ends and by chilled gas which entered at the detector's center and cooled along its entire length. This system permitted the front end electronics to operate at 40°C and the silicon, in the range 25°C–28°C. The ladders were pinned into slots in the bulkhead and rested on shelves into which the slots were cut. The sensors were aligned to 4 μm via Cordax equipment during assembly. At installation, the SVX was aligned to within 50 μm of the CTC by survey. The final alignment was accomplished with tracks. The detector maintained position stability of 10 μm during operation. It was supported externally.

SVX integrated a dose from 30 pb^{-1} of collisions; data were written from 21 pb^{-1}. The detector achieved a spatial resolution of 10.6 μm. Figure 3 shows the residuals between fitted and measured tracks. Figure 4 shows its impact parameter resolution as a function of track p_t including the effect of the finite beam spot size. The impressive contribution of SVX to heavy flavor physics at CDF has been documented elsewhere. [5]

Throughout the run, SVX maintained 98.5% good channels and showed an overall occupancy of 6%, 2% from physics events. Tracking efficiency was 93% for 3- or 4-layer tracks and 98% for 2-layer tracks, including correction for dead regions. Pedestals were stable for weeks, much longer than the time between calibrations, and gains were uniform to within 5%. Because of the radiation-soft design, the signal-to-noise ratio at the innermost layer degraded from 9 to 6 during the course of the run, necessitating the installation of SVX′.

3 SVX′

The performance of the SVX exceeded expectations. Nevertheless, the radiation-softness of its sensors and electronics mandated that the design of its replacement be different. While SVX′ has a mechanical design very similar to that of SVX, progress in sensor technology permitted SVX′ to be assembled from AC-coupled single-sided silicon microstrip sensors. A FOXFET structure is used for biasing. AC-coupling eliminates the need for quadruple sampling since the leakage current does not appear at the preamplifer input. The consequent reduction in equivalent noise charge produced a signal-to-noise ratio of 16 at installation. The ears are slightly modified for use with the FOXFET, and the higher-gain, radiation-hard SVX-H chip is used. Layer 1 ears have alumina substrates. An additional design modification permitted elimination of a gap at 0° in the tracking with a consequent 5% increase in the acceptance.

At the time of this writing, SVX′ has been installed into CDF and is operating but has not yet taken collision data. SVX′ is designed to survive the radiation associated with a few hundred pb^{-1} of data at the Tevatron.

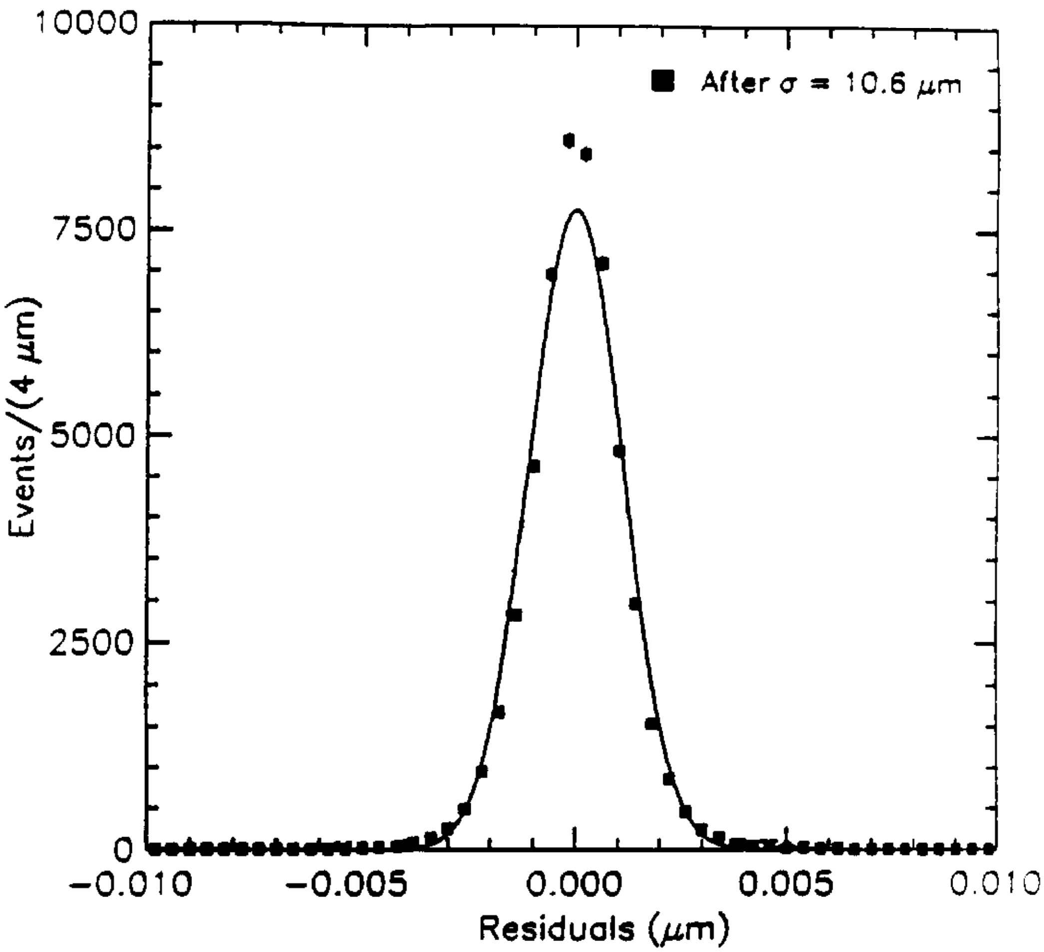

Figure 3: Residuals between fitted tracks and measured hits after full internal alignment corrections. Each track contributes four entries to the histogram, one per layer. All four residuals are included in the track fit. The curve is a gaussian fit.

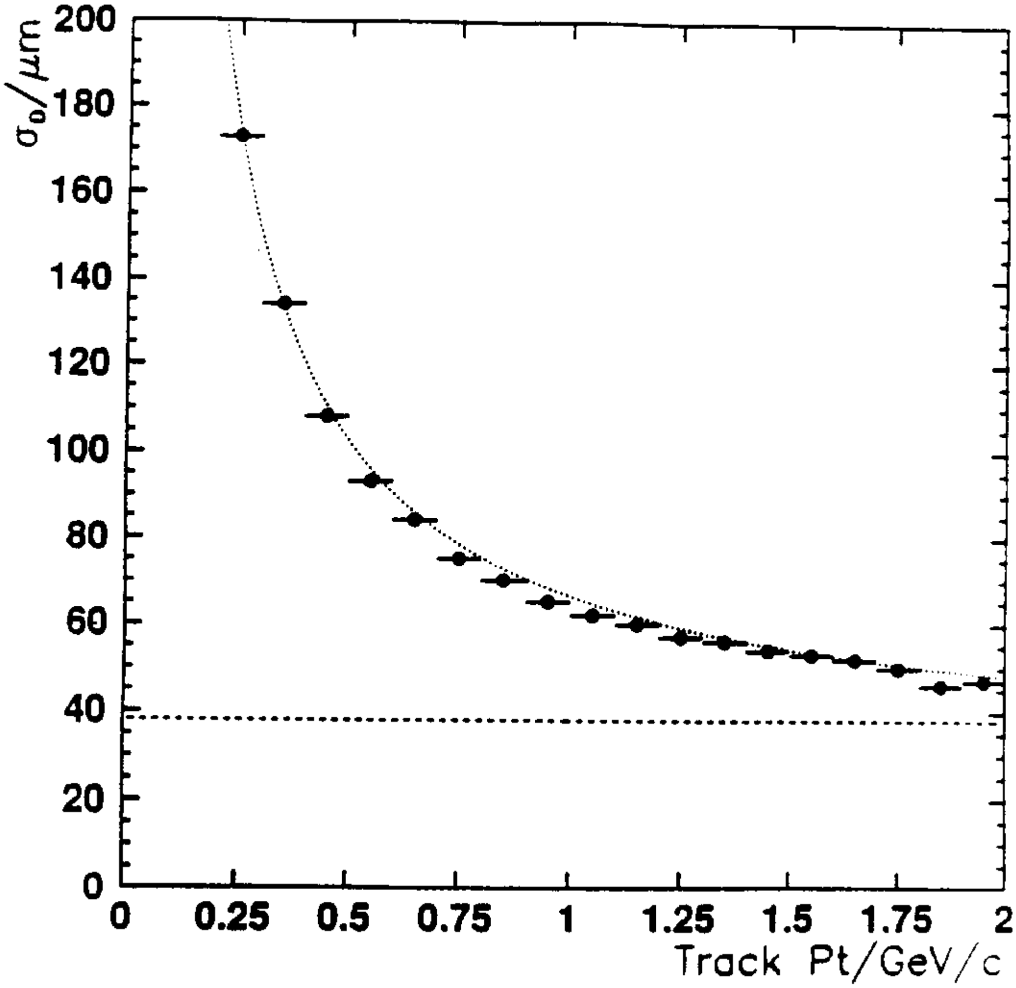

Figure 4: Measured impact parameter resolution of the SVX versus track p_t including the effect of finite beam spot size.

4 SVX II

CDF has identified the improved detection of B decays as one of its primary goals for the latter half of the decade. In addition to improving the sensitivity to top decay through bottom, that program targets rare decays. Such a plan necessitates four changes in the vertex detector design. The first change involves improving the coverage of the interaction region at the Tevatron, which will have a σ_z approximately equal to 30 cm. The 51 cm SVX and SVX′ geometries permit loss both of high-p_t events in the bunch tails and of spherical and forward events everywhere. The first type of loss impacts studies of all rare decays. The second type is especially damaging to studies involving B's. The SVX II will have a total length of 96 cm. Simulation studies [6] indicate that such coverage would improve acceptances for three-track B-tagged top (by 50%), lepton-tagged ψK_s^0 (by 50%), and single B's (by 80%). The second change is the implementation of double-sided sensors. This recent advance in technology should significantly improve the efficiency of the vertex detector for identifying displaced vertices and resolving track ambiguities in (high-multiplicity) B decays. A third change involves the installation of forward tracking in the vertex region. Decays of $b-\bar{b}$ pairs have low p_t and consequently cover a wide range of pseudo-rapidity η. Forward disks are being considered as a second-stage upgrade to SVX II. The fourth modification to the tracker is necessitated by collider upgrades. Linac upgrades, combined with the commissioning of the Main Injector, will produce a luminosity increase to at least $10^{32}\text{cm}^{-2}\text{sec}^{-1}$ and a bunch structure that reduces the time between crossings to 132 ns. The radiation hardness of all technologies in use will have to be guaranteed up to 1 MRad (at the inner layer), and the electronics will have to be completely redesigned.

Figure 5 shows the current design of the SVX II. There will be three independent barrels, each composed of 12 four-layer wedges. Figure 6 is a conceptual design of an SVX II ladder. Ladders will contain 4 microstrip sensors which will be wirebonded in pairs to produce two electrical units, one read out at each end. SVX II hybrids will be mounted directly on the silicon to reduce the dead space between barrels from 4 cm to about 1.5 cm. Rohacell ladders will be fabricated to match the sensors' coefficient of thermal expansion. The total number of channels will increase by an order of magnitude. Alternate wedges will be staggered in radius to allow room at the bulkheads for the increased number of read-out chips, and the beampipe

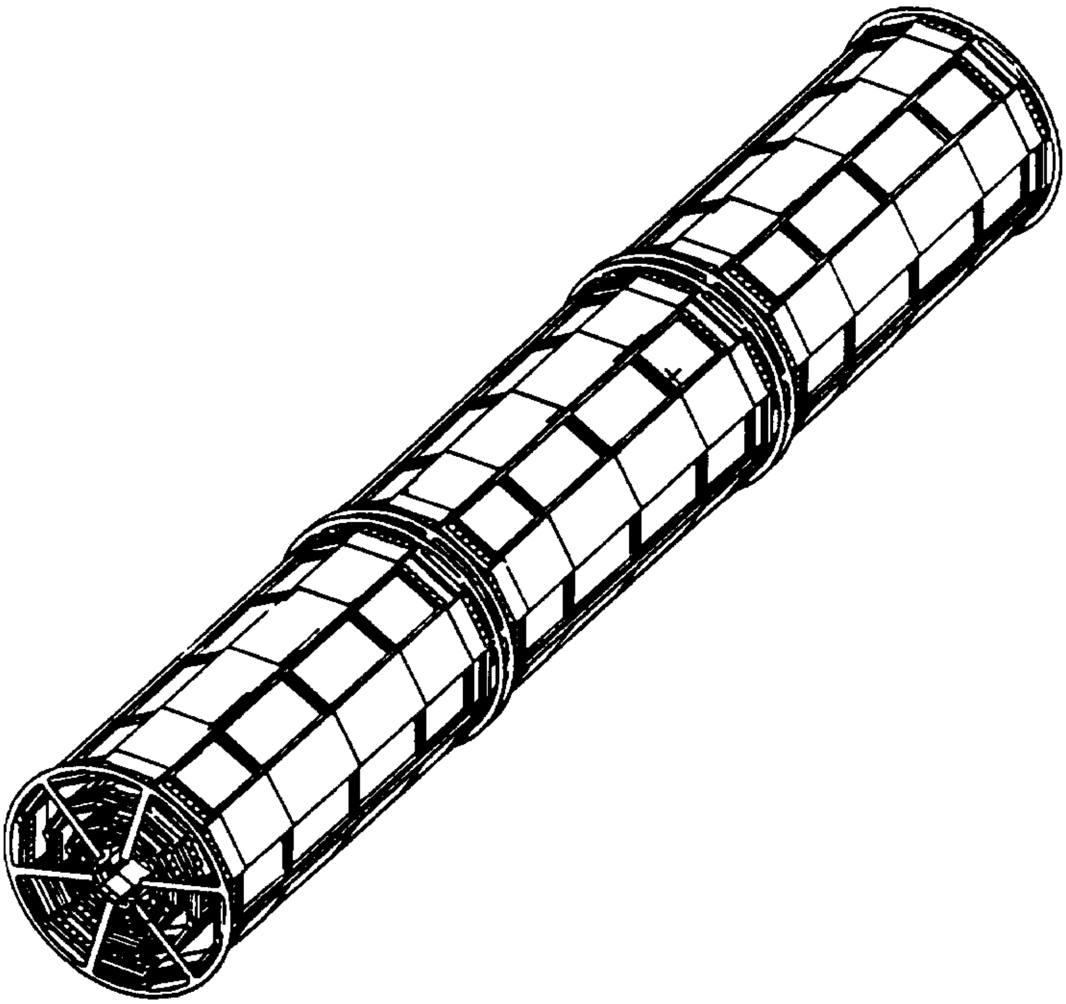

Figure 5: SVX II barrel geometry.

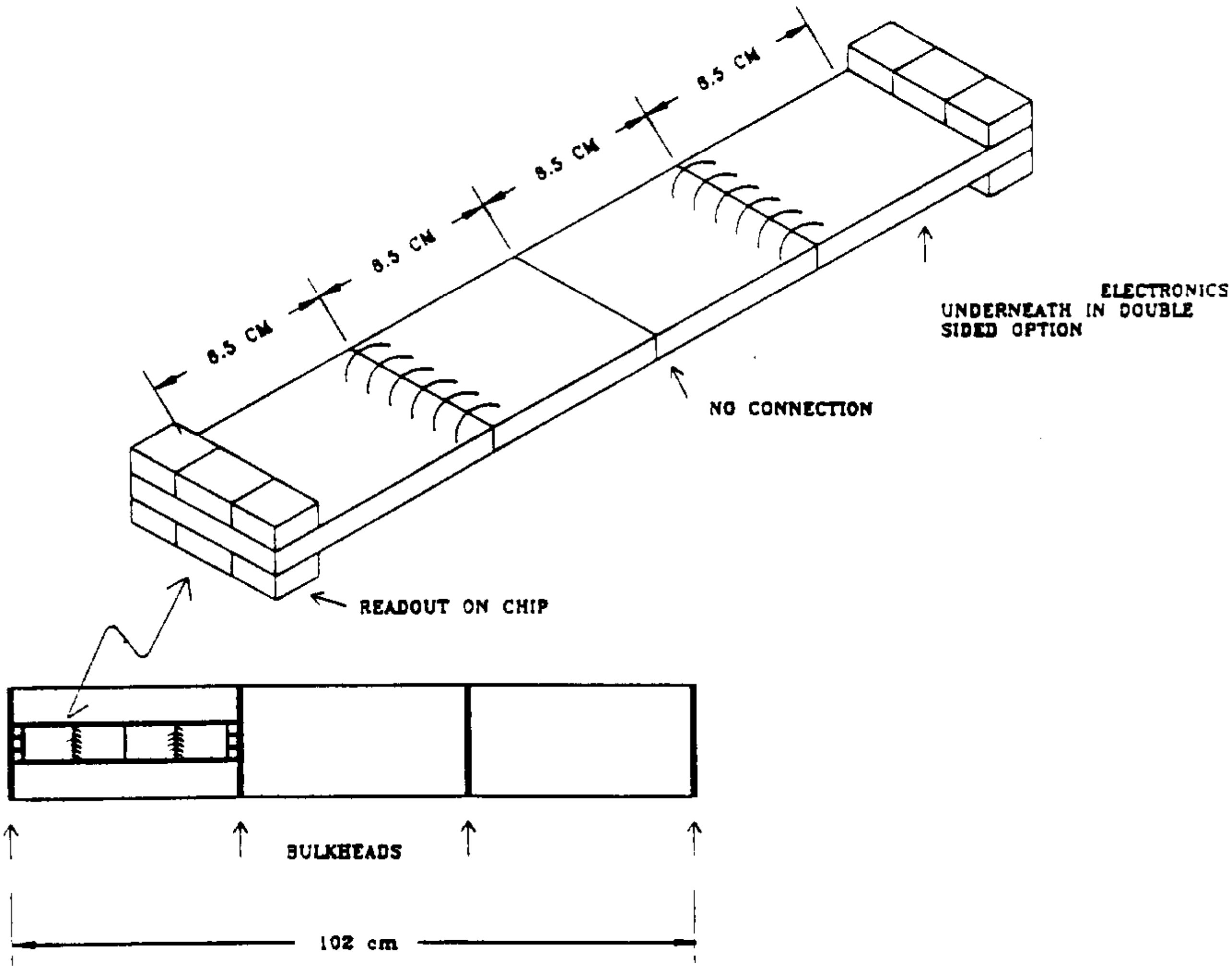

Figure 6: Conceptual design of an SVX II ladder.

outer diameter will be reduced to 1 inch. To maintain effective cooling, water channels will be integrated directly into the beryllium bulkheads.

The double-sided sensors will have p-side read-out pitch between 58 and 62 μm (depending upon layer) and n-side read-out pitch of 134 or 150 μm (also depending upon layer). The p- and n-side strips will be orthogonal to each other. At the present time, several varieties of prototypes are under evaluation in order to determine the optimal technology for re-orienting the transverse n-side strips so that they may utilize a hybrid on one of the short edges of the sensor. Both Delphi-style double-metal and Opal-style glass z-interconnects are being considered.

To guarantee radiation hardness, biasing will be done through polysilicon resistors, and p-implants will provide n-side strip isolation. So-called "intermediate strips" [7] may be used to improve resolution without increasing the number of data acquisition channels. These are implants that are interleaved with read-out channels and are identical to their implants in all ways except that they do not have their own ac-coupled aluminum strips but are instead capacitively coupled to their neighbors.

The SVX II readout [8] will utilize the deadtimeless SVX-III chips which are now in design. Digitization will occur on-chip, and signals will be bussed on copper strip lines to a new portcard. The portcard will contain a field programmable gate array for chip control and an array of "dense optical interconnect modules" which interface with optical fibers. The optical signal will travel to a custom VME module in the collision hall, the Fiber Interface Board, which will drive the signals serially (by fiber) to the counting house. There, another custom card, the Silicon Acquisition Readout, will both transmit them to the Silicon Vertex Tracker [9] and buffer them for response to higher level trigger decisions.

Acknowlegments

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References

[1] An overview of the CDF detector is provided in F. Abe *et al.*, Nucl. Instr. and Methods A271 (1988) 387.

[2] W. C. Carithers *et al.*, Nucl. Instr. and Methods A289 (1990) 388, and references therein.

[3] C. Haber *et al.*, IEEE Trans. Nucl. Sci. NS-35 (1988) 171.

[4] S. Kleinfelder *et al.*, IEEE Trans. Nucl. Sci. NS-35 (1988) 171.

[5] See, for example, S. Dell'Agnello, Proc. 7th Meeting of the Division of Particles and Fields, Batavia, IL, 1992, and N. M. Shaw, Proc. 7th Meeting of the Division of Particles and Fields, Batavia, IL, 1992.

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[8] B. T. Huffman, private communication.

[9] L. Ristori, "SVT: The Silicon Vertex Tracker," CDF Internal Note 1421, 1991.