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Double-Sided Silicon Microstrip Sensors for the CDF SVX II Detector

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ABSTRACT

The SVX II is the planned third-generation silicon vertex detector in the Collider Detector at Fermilab. Now in the prototyping phase, it is scheduled for operation in Tevatron Run II. This document describes aspects of the detector related to the design of the silicon microstrip sensors.

1. Introduction

The SVX II is the planned third-generation silicon vertex detector in the Collider Detector at Fermilab (CDF). Now in the prototyping phase, it is scheduled for operation in Tevatron Run II. Details of its mechanical design are included in Reference 1. This document explains some of the motivations behind the detector design and focuses on the design of the silicon microstrip sensors themselves.

2. Motivation for the Design

The design of the SVX II is driven by the CDF physics goals for Run II and is supported both by detailed simulation work and studies of the behavior of SVX and SVX′, the first two CDF silicon vertex detectors.

The potential of a silicon microstrip vertex detector for both reduction of combinatoric background and improvement of mass and momentum resolution has been convincingly demonstrated[2] with the SVX for events with secondary vertices. Reference 3 documents the SVX′ upgrade, which was conducted primarily but not entirely to achieve improved radiation hardness. The program to upgrade a second time, to SVX II, proposes to achieve three goals:

1. The new vertex detector must be able to operate in the Main Injector environment, in which the beam crossing time will be reduced from the present 3.5 μs to 132 ns or 395 ns and the luminosity will be increased to $10^{32}\text{cm}^{-2}\text{s}^{-1}$. (Reference 4 discusses the impact of the proposed accelerator changes upon the SVX II electronics.)

2. The vertex detector should have improved acceptance for b and top events.

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3. The detector should have the capability for three-dimensional tracking and secondary vertex location in both the $r - \phi$ and $r - z$ projections, and it should provide readout capable of supporting a Level 2 vertex trigger processor.

The interaction region is expected to have a σ_z of about 30 cm during Run II. At 96 cm length, the SVX II will have nearly double the z coverage of SVX and SVX′, which are both 51 cm in length. Figure 1 shows the anticipated improvement of SVX II over SVX in geometrical acceptance for single tracks. This increased length is important both for accepting high p_t events produced in the tails of the bunch and for increasing acceptance of $B\overline{B}$ events, in which many tracks have high rapidity and there is little correlation between the rapidity of the B and that of the $\overline{B}$. Simulation studies[5] predict that the 96 cm length of the SVX II will increase acceptance of three-track B-tagged top, single B's, and lepton-tagged $J/\psi K_s^0$ by 50%, 80%, and 50%, respectively.

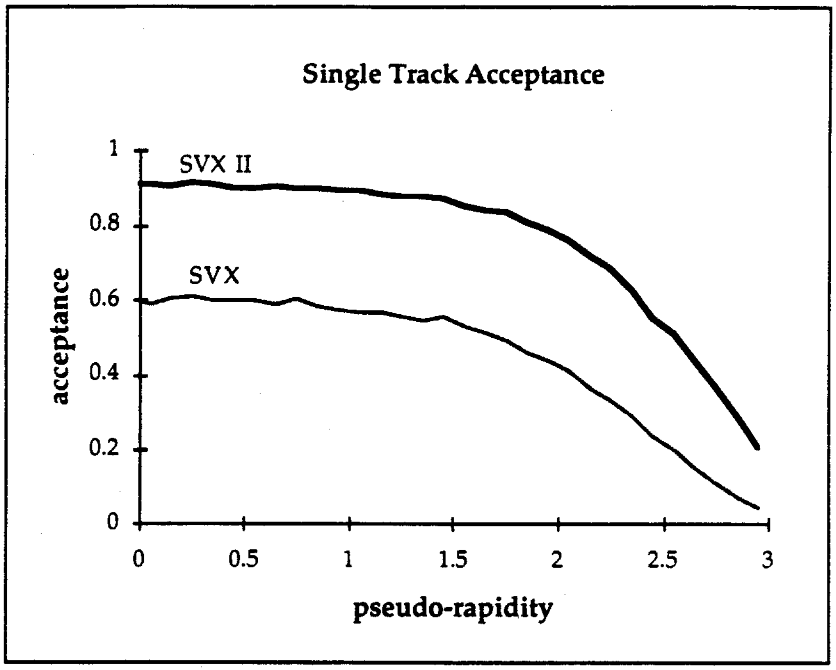

Fig. 1. Single track acceptance for SVX and SVX II for interaction region $\sigma_z = 30$ cm.

The ability to track and vertex in three dimensions is expected to improve the resolution on mass measurements of secondary particles as well as to reduce the number of ambiguous track assignments in high-multiplicity decays. A study[5] was conducted in which $B\overline{B}$ events were simulated with both B's decaying to $J/\psi K_s^0$. The B mass was reconstructed for several possible SVX II geometries. The value of σ_{m_B} was predicted to decrease with the SVX II geometry by 29% over that obtained with SVX. Use of double-sided silicon microstrip sensors is also expected to improve rejection of W+jets background to top events by more than a factor of 40 and to increase the acceptance for lepton-tagged $J/\psi K_s^0$ with an impact parameter significance cut of 3 by 60%.[5]

3. The Silicon Microstrip Sensors

The SVX II will utilize microstrip sensors which are double-sided and as long as possible, their length being subject to the constraints that

1. their capacitive load on the pre-amplifiers should be consistent with a signal-to-noise ratio of at least 12 throughout their operational life.[6]

2. the channel occupancy must be no more than a few percent.[7]

3. efficient use of the silicon wafer must be maintained as much as possible.

The SVX II electrical unit has been chosen to be two sensors, of length approximately 8.0 cm each, wirebonded end-to-end so that their (longitudinal) p-side strips measure $r-\phi$ and their (transverse) n-side strips measure $r-z$. Pairs of these two-sensor units are assembled into mechanical units called "ladders" which are then arranged to form three 12-sided, four-layer barrels.

The specifications for the SVX II sensors include the following:

- n-type bulk silicon
- AC-coupled readout
- orthogonal p- and n-side strips
- polysilicon biasing on both sides
- common p-blocking implant for n-side isolation
- 60 ± 15 V depletion voltage before irradiation
- < 250 nA/cm^2 active area leakage current at $V = V_{depl} + 10V$, which corresponds to about 20 nA/channel.

Table 1 shows the p- and n-side readout pitches and numbers of channels for the four layers in the baseline design. Layer 0 is the innermost layer.

Table 1. SVX II readout pitches and numbers of channels.

	Layer 0	Layer 1	Layer 2	Layer 3
$r-\phi$ readout pitch (μm)	60	58	60	62
$\#r-\phi$ channels	2×128	3×128	5×128	6×128
$r-z$ readout pitch (μm)	150	134	134	150
$\#r-z$ channels	2×128	3×128	3×128	4×128

To minimize the amount of mass in the active area of the detector, and to simplify assembly, the n-side strips will be read out at one of the sensor's short edges so that signals can be routed directly out the end of the barrel. The baseline design calls for use of sensors with a double-metal[8] structure in which the first and second metals are separated by 5 microns of insulator. Because of concern that the double-metal structure may produce unacceptably high capacitance at the pre-amplifiers, a fall-back option of (Opal-style) metallized glass[9] is also being considered for the n-side. Both double-metal and metallized glass involve multiplexing signals on the n-side; however, with the present design, no ghost tracks involving more than 2 hits can be produced.

4. Issues Influencing the Design

4.1. *Radiation Damage*

The SVX II will operate in the Main Injector era at Fermilab with an inner radius of 2.5 cm. Consequently, its innermost sensors will receive an integrated particle flux of approximately $2 \times 10^{13}/\mathrm{cm}^2$ in 1 fb^{-1}. Surface damage due to radiation can increase leakage current and capacitance at the input of the preamplifiers, both of which effects decrease the signal-to-noise ratio. Bulk damage creates trap sites which cause the bulk to invert from n to p type at $1-2\times10^{13}/\mathrm{cm}^2$ and which may require increased voltage to minimize changes in strip capacitance or fully bias the sensor. The polysilicon resistor technology was selected for its radiation hardness. The coupling capacitors utilize a compound dielectric of silicon dioxide and silicon nitride, which reduces the occurrence of pinholes, permitting use of thin capacitors which can withstand voltages well in excess of 100V. It is nonetheless expected that the inner layer of the SVX II will have to be replaced during the lifetime of the detector. References 10 and 11 discuss radiation damage issues relevant to the SVX II design.

4.2. *Microdischarge-induced Noise*

Recent studies by Ohsugi, et al.[12] indicate that AC-coupled silicon microstrip sensors in which the readout strip aluminization is narrower than its implant have significantly lower noise amplitude at all bias voltages than do similar sensors with the ratio (readout strip width/implant width) ≥ 1. The observed noise increase for relatively wider readout strips is believed to be caused by microdischarges produced by the high electric field in the bulk silicon. To minimize noise due to this effect, SVX II sensors will have implants that are 6μm wider than their aluminum strips everywhere, including in the bonding pad region and (if double-metal readout is used) beneath vias.

4.3. *"Intermediate" Strips*

"Intermediate strips" is a term used by the SVX II designers to designate implants which are biased and in every way identical to all other implants on their side of the sensor, but which are not read out directly.[13] Intermediate strips capacitively couple their charge to neighbors which are read out, thereby improving the sensor's resolution and shaping its internal electric field without increasing the readout channel count. The SVX II baseline design retains an option for use of intermediate strips. The option will be exercised if prototypes indicate that intermediate strips improve sensor resolution without significantly increasing capacitance or degrading radiation hardness.

5. Status and Plans

Prototype sensors have been ordered from SINTEF/SI, Micron Semiconductor Incorporated, and Hamamatsu Corporation with a variety of designs, including sensors with and without intermediate strips, sensors with various n-side pitches, sensors with double-metal, and sensors ready for application of glass. In the very near future, specifications will be finalized for a design which optimizes signal-to-noise ratio, resolution, and radiation hardness. The impact on CDF tracking of additional sensors with small-angle stereo strips is also being studied.[7] An order for production sensors will be placed in 1995.

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