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Abstract:

Future colliding beam runs at Fermi National Accelerator Laboratory will involve bunch spacings of protons and antiprotons at 132 ns intervals. Due to finite processing time, a pipelined architecture is needed to store events until a trigger decision can reach the detector. A single ported pipeline design has been implemented in a 1.2 micron rad soft CMOS technology and partially tested. Results are presented of the performance of that design. The chip supports a level 1 accept rate of 5 kHz. Because high statistics B physics experiments will require level 1 accept rates of 50 kHz, a new dual ported pipeline device has been proposed which would make the readout virtually deadtimeless for trigger rates approaching 50 kHz. The operation of the proposed deadtimeless device is explained.

1. Introduction

In this paper progress in the development of a readout chip for the SVX-II detector at CDF is described. Initially a readout chip designed to run with a beam crossing time as short as 132 ns, a level one latency time of 4.1 microseconds, and a level one accept rate of less than 5 kHz was envisioned. A chip (SVX-II) with a single ported pipeline consisting of 32 cells to accommodate the 4.1 μ s level one trigger formation time has been designed and test chips implemented in a 1.2 micron radiation soft CMOS technology were received in February, 1994. The operation of this chip is described.

Because of delays in the Fermilab Main Injector program and the rapid development of the B physics program within the CDF collaboration, it has been proposed to expand the scope of the SVX II project by designing the readout system to operate at level one accept rates of approximately 50 kHz with virtually no deadtime. To achieve this goal the collaboration is proposing to continue the development of the present readout chip toward one with a dual ported pipeline capable of simultaneous analog and digital operation and the addition of analog cells to act as data buffers during digitization and readout. Such buffering has been proposed before for use in LHC project where the expected trigger rates are also anticipated to be high.[1,2] A preliminary look at a two chip architecture (SVX-III) proposed for this readout is discussed.

2. SVX-II/III Architecture and Operation

To understand the operation and design of the SVX chips one must know something about the operating parameters of the Tevatron beam as it is proposed in future runs. For the near future the spacing between beam crossings will be 396 ns with 132 ns spacing possible into the next century. Figure 1 shows a picture of what 132ns bunch spacing would look like in the Tevatron. Each filled-in circle represents a group of 7 rf buckets one of which contains protons and antiprotons. The rf frequency of the Tevatron is 53 MHz so each group of filled circles represents a potential collision every 132 ns. Collisions come in three groups of 33 crossings separated by 2 μ s gaps called abort gaps. At a luminosity of $10^{32} \text{cm}^{-2} \text{s}^{-1}$, the average number of collisions per crossing is one.

Figure 2 shows the block diagram of the sections on the SVX-II chip.[3] A charge sensitive amplifier is employed as the first stage of amplification. The SVX-III device is similar but has skip logic to control the dual ported pipeline. The full 132ns between crossings is used for integration time, and resetting and switching in the next cell of the pipeline. Since there is not enough time between beam crossings to reset the front end amplifier, it has been designed with a 380 fC dynamic range and a gain of 5 mV/fC. The front end preamp is reset only during the abort gaps. This amplifier also has a bandwidth control which is set during initialization. This is needed in order to optimize the amplifier performance for 396 ns bunch spacings as well as 132 ns. It is possible to randomly excite each of the 128 channels in a chip by downloading a mask during initialization. This allows one to pulse any given channel through the calibration input.

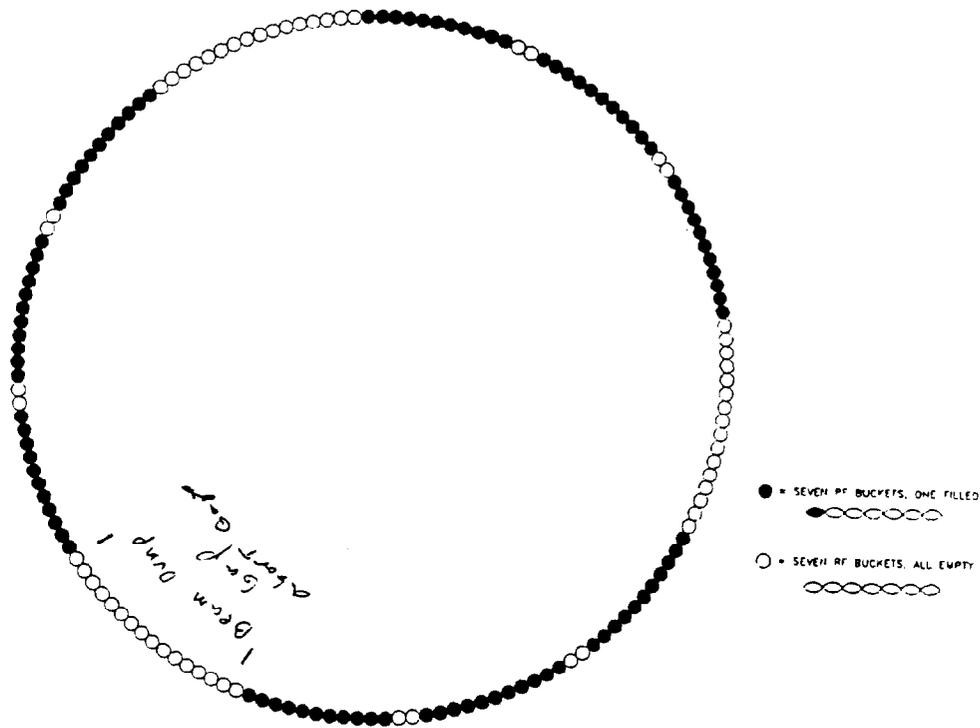


Figure 1 This diagram shows the structure of the Tevatron beam for bunch spacings of 132ns. Each filled circle represents seven rf buckets with one bucket containing protons and antiprotons. The $2.1\ \mu\text{s}$ gaps are to allow for safe aborting of the beam. The rf frequency of the Tevatron is 53MHz.

During a given beam crossing, only one of the pipeline capacitors in the second amplification stage is switched into the amplifier's feedback loop. A double correlated sample is taken, so only the difference in charge between the last and the present beam crossing is placed on the pipeline capacitor. Before each beam crossing the cell to be written is reset and that capacitor placed in the feedback loop. The pipeline has to be long enough to allow for the trigger processing time and the cable delays to the chip. It has been determined that for 132 ns bunch spacing a 32 cell pipeline is long enough, allowing for $4.1\ \mu\text{s}$ of total delay. The depth of the pipeline is set during initialization.

When an event is read out, advancement of the pipeline ceases and the same amplifier that wrote to the cell is now used to send the charge to a comparator. A Wilkinson-type ADC performs the digitization by switching a comparator when a constant ramp current deposits more charge on the comparator reference than the charge on the pipeline cell. When the comparator fires, the value of a Gray code counter is latched into an asynchronous FIFO. When the maximum count is reached, the FIFO is engaged and all the channels above a user-defined threshold collapse in order of channel number and are in the FIFO ready for readout. The Gray code counter has a maximum count of 8bits. An external resistor will control the ramp current allowing some flexibility in choosing the digitizer's dynamic range. CDF intends to digitize to 7 bits and up to 6 MIPS with a counter frequency of 53 MHz. The counter counts on both the rising and falling edges of the clock.

Note that readout and data taking never occur at the same time. Therefore, the readout lines are switched into control areas of the chip during acquisition and digitization and act as

SVXII Block Diagram

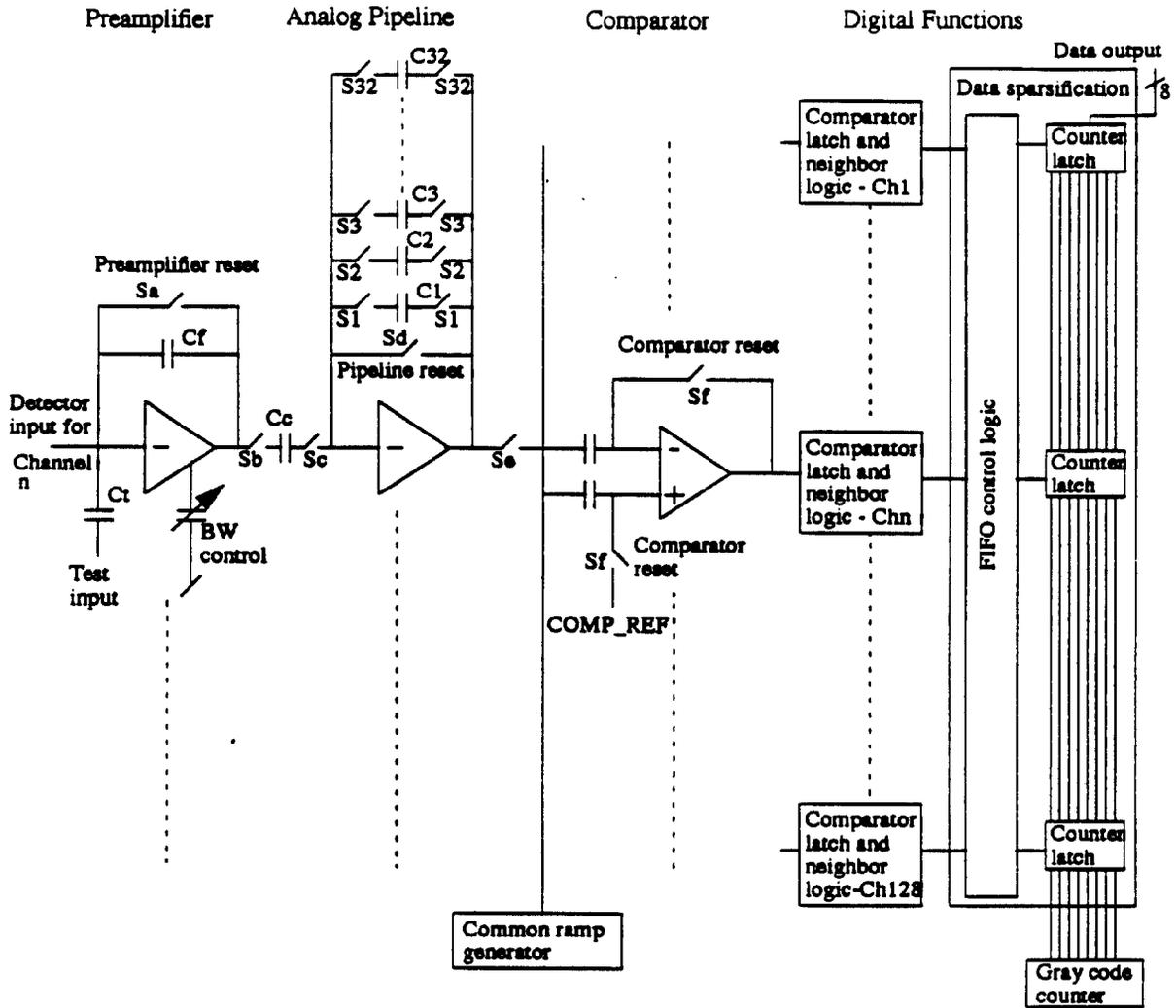


Figure 2 A block diagram of a single channel of the SVX-II chip. The sections split into the analog amplifier, the single-port pipeline, and the digitization and readout sections.

control lines. The output arrives on an 8 bit bus with channel number and then the channel data appearing on the bus on the high and low cycles of a 26.5MHz clock respectively. To read data from a chip, a Priority IN pin is sent high, telling the chip to put the digitized data on the readout

bus. When that chip is finished with readout it will send a Priority OUT pin high on the next clock allowing the next chip in the chain to take control of the readout bus and output its data. In this way, multiple chips can be daisy chained and use the same output data lines.

2.1 Chip Features and Test Results

The first submission of a full SVX-II chip was received in late February of this year. Apart from some operational problems in the digital section of the chip which can be corrected, the analog portions performed to specification.

There are many features of this chip that make it an extremely flexible device. The flexibility is required not only because of the fact that the bunch spacing is expected to change, but also because the device is used by both the CDF and D0 experiments at Fermilab. The detectors from these two experiments have different input capacitances, and it is important to be able to optimize the amplifier performance for the two cases.

Below is a list of features of the SVX-II chip:

- All 128 channels can be independently pulsed for calibration purposes.
- Can be set to receive either positive or negative input signals.
- On-chip digitization and sparsification.
- Preamplifier bandwidth is adjustable to allow optimization for a range of input capacitances and beam crossing times.
- Adjustable pipeline depth (up to 32 cells).
- Control and data functions are on the same lines, reducing the number of I/O pins on the chip.

The following is a list of the test results from the first rad-soft submission of the SVX-II chip. The chip noise is a function of both the input capacitance and the integration time of the amplifier. This noise performance is shown graphically in Figure 3 from measurements made on the SVX-II chip.

Table 1: Measured Test results

	Test Result	Specification
Preamp Dynamic Range	340 fC	380 fC
Pipeline Dynamic Range	>18 MIPS	18 MIPS
Preamp Gain	5.9 mV/fC	5.0 mV/fC
Pipeline Gain	3.0 mV/fC	3.0 mV/fC
Noise for 20pf input capacitance and 200ns integration time.	1350 e-	As small as possible
Pipeline crosstalk	0.2%	<1%
Nonlinearity	<.1%	<1%
Power during Acquisition	200mW	Total average power less than 500mW per chip.
Power during Readout	840mW	

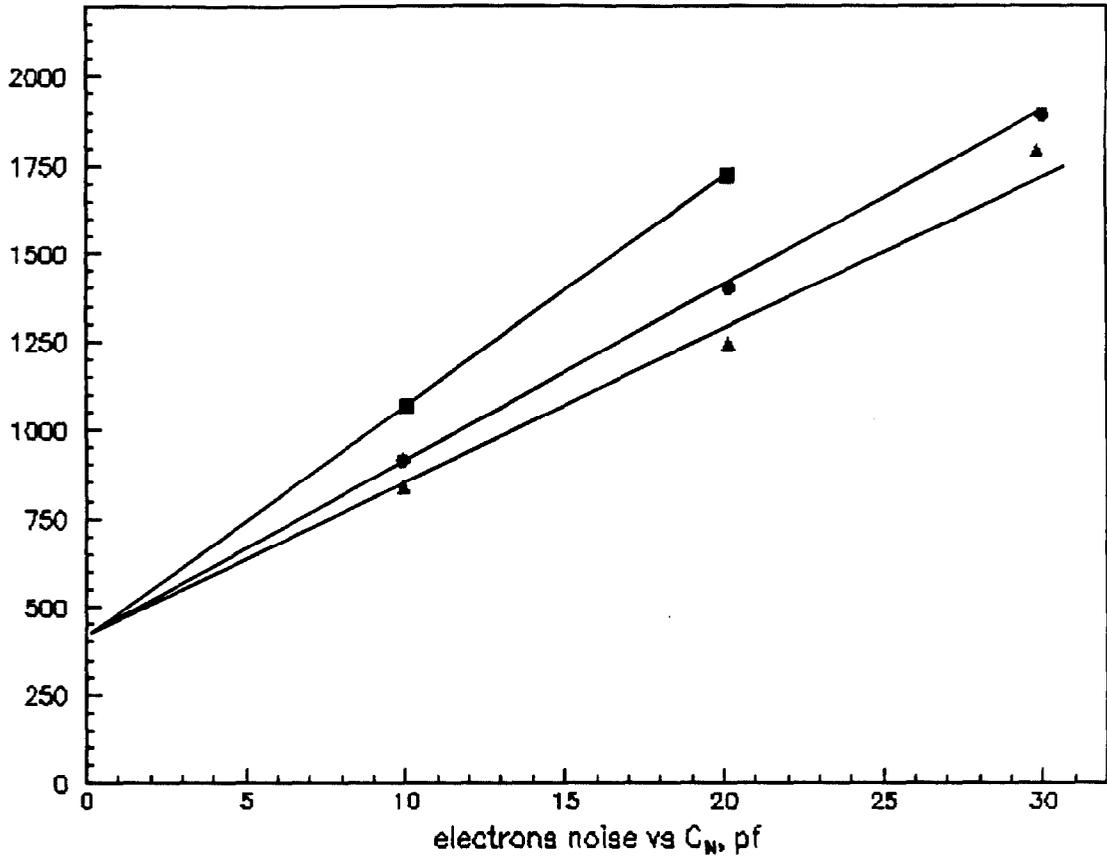


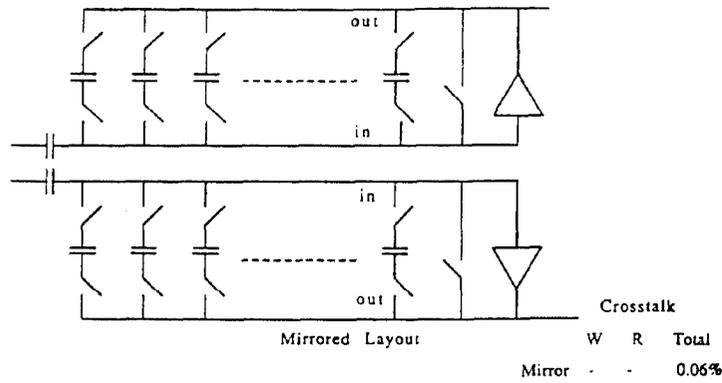
Figure 3 Shown here is the measured noise performance of the SVX-II chip as a function of input capacitance for three different bandwidth settings.[4] The bandwidth settings correspond to 1-99% rise-times of 150ns, 200ns, and 400ns.

The small channel to channel crosstalk is achieved by making each successive pipeline the mirror image of its neighbors in the layout. In this way the input lines and output lines are always next to each other so the output of one amplifier will not easily couple to the input of its nearest neighbors.

3. The Proposed SVX-III readout Chip Set

The SVX-II chip has some deadtime for two reasons. First, the pipeline is stopped and all chip functions come to a halt during digitization and readout. Consequently, events will be lost while those operations are in progress. Secondly, there are potentially good events waiting in the pipeline which occurred during the trigger formation time of the event being processed. However, the pipeline is lost after a readout cycle and the entire event taking process begins anew. One loses an amount of time equal to the level 1 trigger formation time which is 4.1 μ s. These are quite large effects when the trigger rate is 50kHz. For such a trigger rate the estimated dead time (assuming a 10% hit occupancy) would be about 40%.

SVXII Pipeline



Dual Port Pipeline Extension of SVXII Pipeline

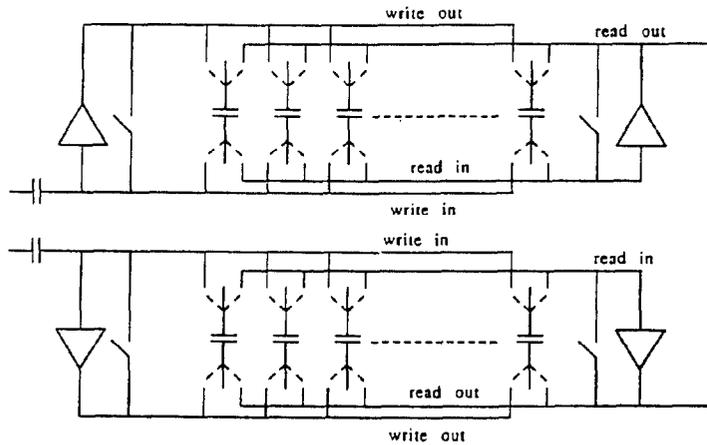


Figure 4 Drawings contrasting the current single-port pipeline with the proposed SVX-III dual ported pipeline. The mirror image design of successive channels helps reduce cross-talk between cells.

The way around this problem is twofold. First, the pipeline must be dual ported so that any cell can be read from or written to independently. This requires the addition of another pipeline amplifier. Whereas the SVX-II pipeline amplifier can be either reading from or writing to the pipeline depending on how it is controlled, the SVX-III chip will have dedicated read and write amplifiers for the pipeline.

Secondly, a daisy chain of 10 SVX-II chips requires about $4.1 \mu\text{s}$ to complete digitization and readout for a 10% hit occupancy. The SVX-III chip will have 4 extra cells in the pipeline. These cells will allow the chip to pull a cell out of the pipeline while it is being read out and still maintain a $4.1 \mu\text{s}$ delay. This has the same effect as adding 4 memory buffers where the data is stored until readout is complete.

Figure 5 shows why at least 4 cells are needed for deadtimeless operation at a 50kHz trigger rate. λ symbolizes the trigger rate and μ represents the service rate; in this case the service rate is synonymous with the time required for digitization and readout. Two cases are shown here, one with a Poisson distributed service time and the other with a fixed service time. In both cases it is assumed the trigger rate is Poisson distributed. The actual service time will have a probability distribution somewhere between these two extremes.

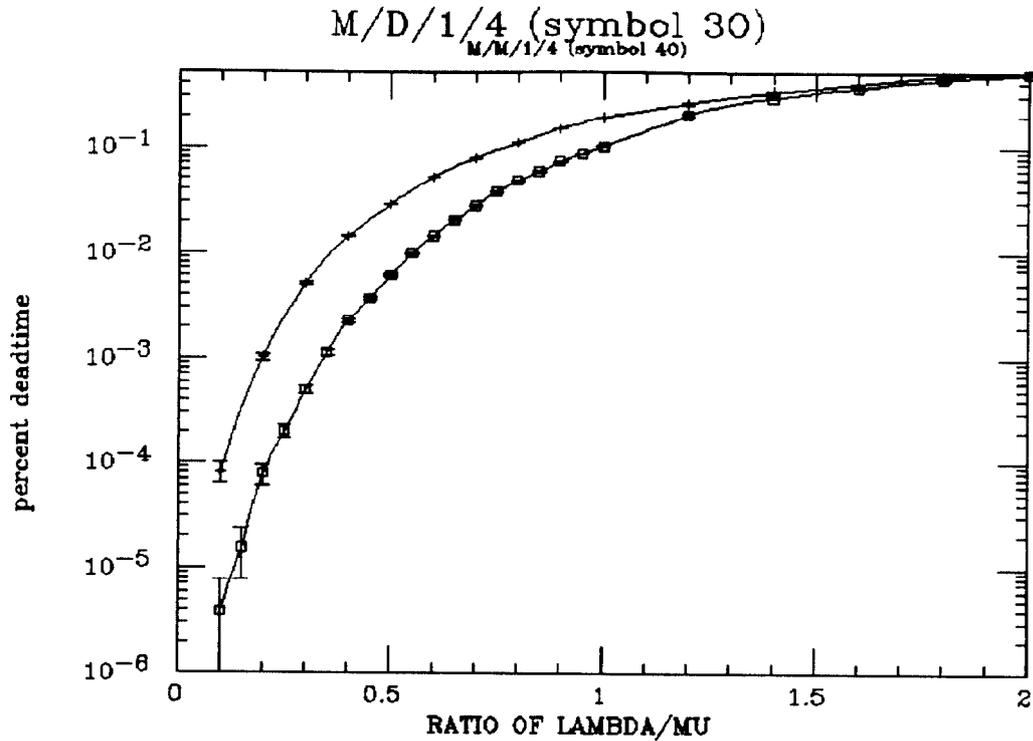


Figure 5 The percentage of deadtime as a function of the ratio of the trigger rate over the service rate given that there are 4 holding buffers: Λ =trigger rate and μ =service rate. The diamond points assume the service time is fixed while the square points assume a Poisson distributed service time. The input distribution is assumed to be Poisson distributed in both cases. The plot was generated using a Monte Carlo simulation.[5] Percent deadtime is defined as the percentage of time all four buffers are full.

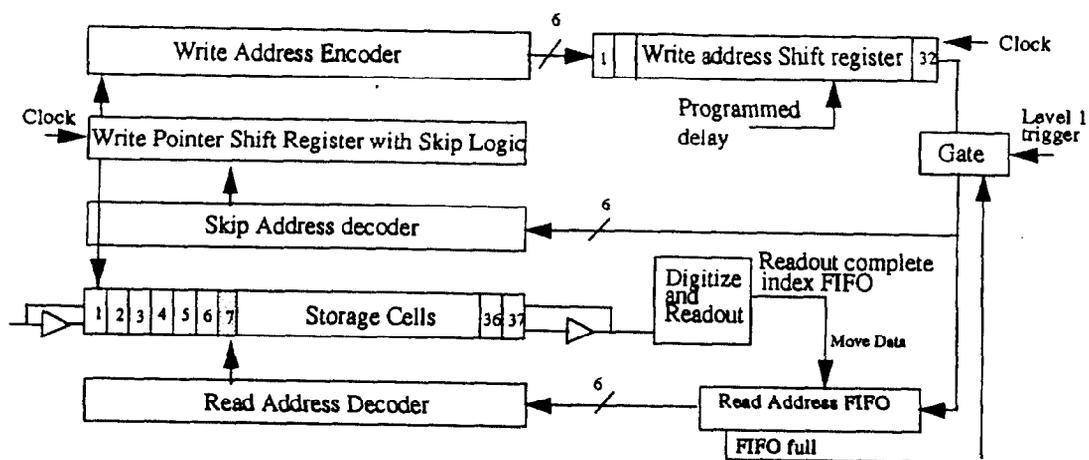
As long as $\Lambda/\mu < 0.5$, the percentage of deadtime remains less than 2%. To achieve the same deadtime with only 3 additional cells requires $\Lambda/\mu < 0.3$. The deadtime quickly rises above 10% as $(\Lambda/\mu) > 0.5$ placing a limit on the trigger rate permitted.

3.1 Operation of the SVX-III deadtimeless Pipeline

Figure 6 shows a block diagram of how the proposed SVX-III deadtimeless pipeline will operate. At each beam crossing data is being placed on the storage cells in the pipeline. Shown in the figure is a cell (#7) that is currently in the readout cycle. This cell is remembered by the skip address decoder and will be skipped by the write pointer when it reaches that cell.

As the write pointer shifts from cell to cell, the 6 bit address of that cell is encoded and loaded into a 6 bit parallel shift register which is as long as the pipeline depth the user sets. Shown in Figure 6 is a pipeline depth of 32 cells.

At each beam crossing, the address of the cell is shifted down the register until it falls out the back and encounters the gate simultaneously with the trigger for that cell. If there is no trigger, nothing happens. If a trigger is present, then the cell address is stored in the skip address decoder effectively marking that cell as one to be skipped. The address is also sent to a 4 deep asynchronous FIFO where it will await its turn for digitization and readout. When that cell's address is at



Skip Logic Architecture

Figure 6 Block diagram detailing the operation of the dual ported pipeline with skip logic to allow cells to act as buffers.

the front of the FIFO, the Read Address Decoder will engage the proper cell and begin a readout cycle. When the readout cycle is done, a readout complete signal is sent to the FIFO to move the next address forward and is also used as a clear for the skip logic (not shown). There is also a gate inhibitor that prevents triggers from initiating readout if the FIFO is full.

3.2 Other differences

Simultaneous read and write capability is a serious technical challenge because readout occurs during data taking cycles. For this reason, it has been decided to go with a 2 chip set. One chip will contain the analog operations and the pipeline with its skip logic, while the other will contain the digitization, sparsification, and readout functions. This has been decided in order to eliminate possible couplings from the digital to analog sections from a common substrate.

Again because of simultaneous read/write capability, one must supply separate control and output lines. It is also planned that many of the control signals and all of the output lines be differential in order to further minimize interference.

4. Conclusions

The first radiation soft submission of the SVX-II chip for use with silicon strip detectors in a high rate environment has been received. Most of the chip parameters are within specifications and a new submission is being prepared for the fall of 1994. Work is proceeding on the dual ported SVX-III readout chip set. This device will have most of the same features as the SVX-II chip, but it also will have both a dual ported pipeline and additional pipeline cells which act as buffers for the data. This will enable the SVX-III chip to remain virtually "deadtimeless" for trigger rates up to 50kHz. The preamplifier, and much of the digitization and readout electronics for this device already exist in the current chip. A layout has been completed of the skip logic and work is pro-

ceeding on the redesign of the pipeline.

5. References:

- 1 K. Borer, *et al.* RD-2 collaboration, *IEEE Trans. Nucl. Sci.* **41(4)**, pg. 877, (1994).
- 2 Joel DeWitt, *IEEE Trans. Nucl. Sci.* **41(4)**, pg. 749, (1994).
- 3 The following discussion is more completely detailed in: "A Beginners Guide to SVX-II", Ray Yarema, *et al.*, F.N.A.L., Batavia, IL 60510.
- 4 Tom Zimmerman, Private Communications, F.N.A.L., Batavia, IL, May, 1994.
- 5 Stephan Van den Brink, Private Communications, University of Pittsburgh, March, 1994.