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Trigger and Electronics Issues for Scintillating Fiber Tracking

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Trigger and Electronics Issues for Scintillating Fiber Tracking

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ABSTRACT

Scintillating Fiber technology has made great advances and has demonstrated great promise for high speed charged particle tracking and triggering¹. The small detector sizes and fast scintillation fluors available, make them very promising for use at high luminosity experiments at today's and tomorrow's colliding and fixed target experiments where high rate capability is essential. This paper will discuss some of the system aspects which should be considered by anyone attempting to design a scintillating fiber tracking system and high speed tracking trigger. As the reader will see, seemingly simple decisions can have far reaching effects on overall system performance.

1. General Comments

1.1. System and Sub-system integration

A variety of important parameters must be considered when constructing a scintillating fiber tracker to be used as part of a high speed trigger. These parameters effect the physics performance (off-line event reconstruction and track finding algorithms) of the detector, the cost to design, the cost to construct, and trigger performance of the detector as a system.

In order to build a functioning tracking system, all subsystems must be considered before the design is finalized. It is possible to design a system which does a superb job of off-line track reconstruction, but which is incapable of making a trigger and may cost an astronomical amount to instrument.

1.2. Important Considerations

It is vital that the system designers consider the following requirements and how they effect the design decisions. These requirements include (But are not limited to):

- 1) Functionality (How well does the system provide performance for both off-line reconstruction and for high speed real time triggering?)
- 2) Designability (Does the proposed solution pose insurmountable problems for any subsystem, electronics or mechanical problems)
- 3) Maintainability (Can the proposed systems be reliably maintained with a minimum effort, this affects access requirements, repair vs. replace, and diagnostics costs.),

and 4) Affordability (Can the proposed system be designed and built within reasonable cost constraints? Does any one part of the overall system force any other subsystem into a situation where its only recourse is to be overly expensive or impossible?). It is imperative that all parts of the system design be considered as to their effects on the overall system cost and performance.

2. Design Strategy

It is useful to think of the design problem as one existing in a multi-dimensional space, where the dimensions are: off-line track reconstruction performance, trigger performance, power consumption, cost to construct mechanically, cost to construct electronics, cost to maintain system, and delivery schedules. The design team will want to maximize the performance and minimize the cost of the system. We will discuss what design parameters can be varied to achieve some of these goals, SDC specific designs will also be discussed. Only designs for colliding beam experiments will be discussed, although many of these discussions lend themselves to fixed-target experiments as well.

2.1. Electronics Design and Sub-system Support

The design strategy for the electronics has been to provide: 1) high-rate performance and to avoid introduction of dead time into the system, and 2) hermetic trigger coverage. It is undesirable to have seams or holes where the trigger efficiency would be low.

2.2. Electronics Architecture

Architecturally, the electronics for the Scintillating Fiber Tracker and Trigger can be viewed as a multi-layered structure.

(1) The first layer of the structure provides the interface and support for the Visual Light Photon Counters (VLPCs) which are our choice for the transducers for the light from the scintillating fibers. This includes the VLPC readout, the supply of VLPC bias voltages and temperature monitoring, and power for the Amplifier Shaper Discriminator (ASD) circuits within the VLPC cassettes (VLPCs are cryogenic devices and reside within cassettes which install in cryostats operating at 6°K).

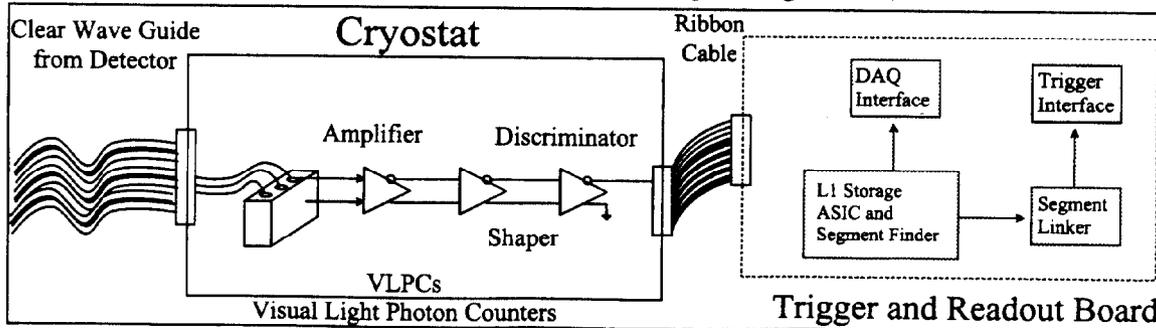


Figure 1. Schematic for Scintillating Fiber Front-end Electronics

(2) The second layer provides a trigger decision delay storage for both level 1 and level 2 trigger logic.

(3) The third layer provides high speed pipelined track information which is reported to the trigger system for linking track information with the calorimeter and muon detectors sub-systems.

(4) The final layer provides the readout path to the Data Acquisition System (DAQ) and also provides for low-rate diagnostic monitoring of proper system functionality and operating parameters.

The electronics is implemented in crates which reside in racks outside the tracking volume but close to the VLPC cryostats. Figure 1 shows a schematic of the front-end electronics system.

Functions 2, 3, and 4 above are implemented on the readout boards using Application Specific Integrated Circuit (ASIC) technology. The system is currently designed using two ASICs. The first of these, the segment-finder ASIC, shown schematically in figure 2, provides all Level 1 and Level 2 pipelined data storage as well as providing track segment finding (i.e. clustering of fiber hits) within a superlayer, and the DAQ interface for 64 fibers.

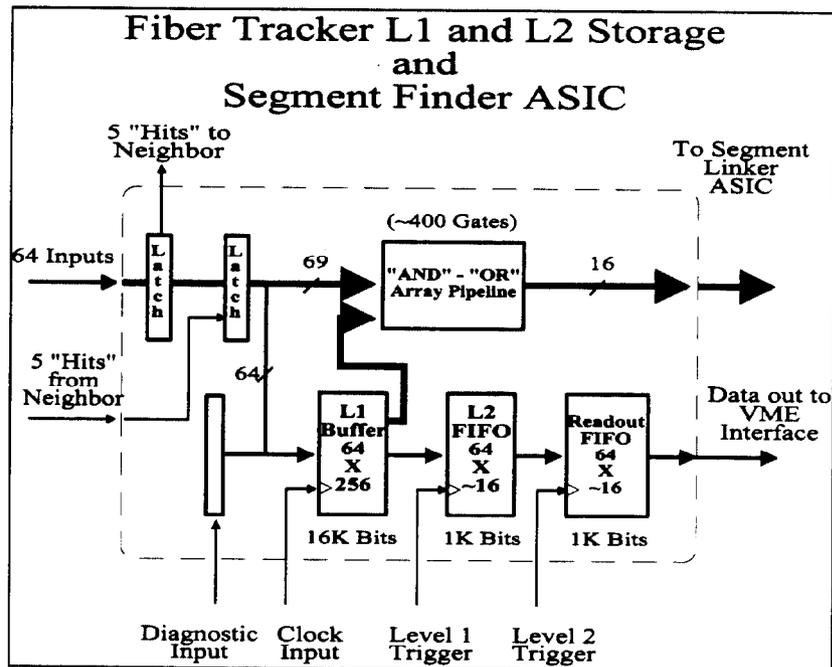


Figure 2. Level 1 and 2 Trigger storage and track segment finding ASIC.

2.3. VLPC Support

Each readout card provides support to the VLPC cassette with which it communicates. The support includes temperature monitoring for the cassette, a pressure monitor from the cryostat, up to 96 individual bias voltages for the VLPCs arrays, and power for the ASDs for each channel. These services are provided via a single 128 conductor ribbon cable which connects one readout card to its corresponding cassette.

3. Trigger Methodology

3.1. Superlayer Structure

The basic tracking structure chosen for the scintillating fiber tracker is one in which several superlayers are used. A superlayer is made up of multiple layers of scintillating fibers typically made from several layers of fiber doublets. Each fiber doublet layer is made by joining two single fiber ribbons together. A sample superlayer is shown in figure 3.

The superlayers are arranged in a barrel fashion^{2,3} at various radii from the interaction point. The choice of these radii affects many of the system performance parameters. Examples of superlayer spacing are shown in figure 4. Each superlayer has several fiber ribbon doublets, some measure the R-Phi coordinates and others measure the U and V coordinates of tracks passing through the superlayers. This superlayer scheme allows for minimum complexity in mechanical design and provides off-line reconstruction of several space points for each track. Each superlayer which participates in the trigger has two separated doublets that measure R-Phi.

3.2. High P_T Track Triggering

A high speed (level-1) trigger scheme has been developed based on recognizing high P_T tracks in a scintillating fiber barrel tracker. Only the R-Phi coordinate is used in the trigger, this is the only component required to measure the transverse momentum, P_T . The reader will see from later discussions that to get Z coordinate trigger information from the stereo layers of fibers, U and V layers, is very difficult. Alternate methods of getting Z information into the trigger will be discussed.

The trigger system is designed to find high P_T tracks very quickly and report them to a global trigger system for linking with other subsystem trigger information. The basic method used for the trigger is one in which track "segments" or stubs are found with in each superlayer. These "segments" are then linked to form tracks. These two

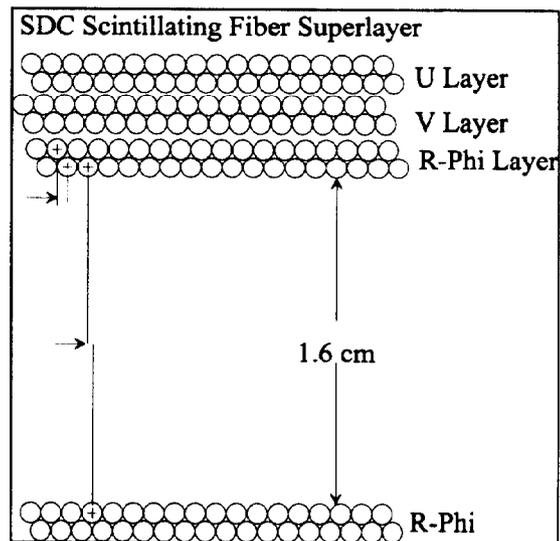


Figure 3. Superlayer structure used for SDC. Each superlayer has 4 doublets 2 R-Phi and a single U and V.

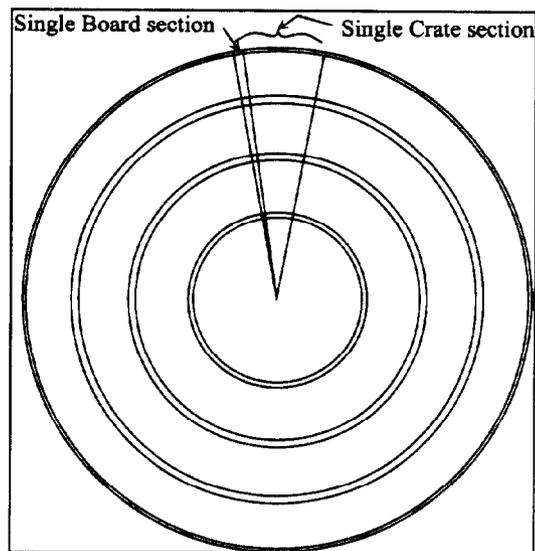


Figure 4. Axial view of scintillating fiber tracker showing superlayers at various radii.

processes, segment finding and segment linking, are carried out across the entire detector in parallel so that the delay from the arrival of the hit information from the interaction to the reporting of a found track to the trigger system can be as little as 100ns.

At the speeds required for a level 1 tracking trigger, there is little or no time for unraveling the placement or positions of the fibers. This information must be "hard wired" into the system from the very beginning. Thus, the design and construction of the tracker must make provisions for the electronics requirements from the start.

3.3. Tracker Segmentation

Figure 5, which shows a typical superlayer structure, also shows how the tracker must be segmented to allow for the formation of a trigger in a very short time span. Segmenting the tracker into Phi slices, where each slice is identical to all other slices, and where each Phi slice is handled by a single readout board, allows for all of the information needed to form a track trigger to be resident on each board. Only a small number of adjacent channel hits need be transmitted between adjacent boards in order to create a "seamless" trigger. Figure 3 shows the Phi slice (not to scale) for a single readout board and particle trajectories which cross the inter-board boundary and must have their hits "shared" across this boundary. If, in the design process, this type of symmetry is not included, each Phi slice will be different and each readout board will be unique. This would lead to a very expensive system and a difficult system to maintain.

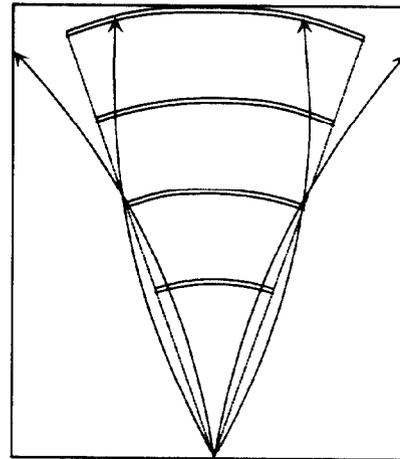


Figure 5. R-Phi slice of a 4 superlayer tracker showing charged particle trajectories which cross Board/Crate boundaries

3.4. Track Segment Finding.

The algorithm for track segment finding uses a fixed pattern of combinatorial "AND/OR" logic to find high P_T hits in a given quartet layer with a resolution of one fiber diameter. If the correct symmetry is maintained, the segment finding for each single fiber position would require four 4-input AND gates and one 4-input OR gate.⁴ Figure 6 shows the two R-Phi doublets of a single superlayer, the reader can see that the number of logic terms needed to detect a track which lies within a 10 GeV/c cone is small. In the SDC implementation, each track segment finding ASIC has 16-fiber bins to cover so that it requires 64, 4-input AND gates and 16, 4-input OR gates. If one were to allow for fiber inefficiencies and develop logic based on "2-fiber" segments, the number of terms would increase by a factor of 3, but this is still a small number of AND and OR terms.

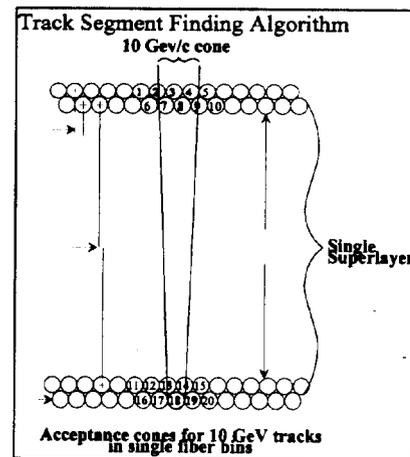


Figure 6. Segment finding.

ASICs of this size and complexity are common and if one does not need the 63 MHz performance that SSCL required, these ASICs could be replaced with Field Programmable Gate Arrays (FPGAs).

The number of fibers which must be shared across ASIC/CARD/CRATE boundaries is 5 in and 5 out per 64 element section. This allows for the system to find all track segments without any gaps or dead spots in the trigger coverage. However, if the symmetry described is not maintained, the number of fibers shared across boundaries would grow very large and the number of AND and OR terms in each ASIC would have to grow to accommodate the variations from Phi slice to Phi slice. The designer is urged to not let this happen as the cost of the electronics will grow rapidly.

3.5. Track Segment Linking

The task of linking the individual track segments into tracks can be accomplished by a scheme similar to that used for segment finding. Provided that the superlayer design maintains a Phi slice symmetry, each linker ASIC has the same task as all other linkers and the number of AND and OR terms needed is small.⁵ Thus by using a relatively small amount of combinatorial logic we can examine the entire set of hit positions for tracks which satisfy the stiffness or P_T requirement. Requiring segments from three superlayers serves to reject false tracks. It is also possible to make a range of P_T triggers by requiring that the tracks are less inclined than the minimum P_T track. This allows the system to report a P_T code including a sign bit and some number of bits of P_T information, based upon the slope of the track within the trigger layers. Figure 7 shows a typical segment linker Phi slice for SDC, note the minimum P_T threshold for SDC was 10 GeV/c. The trigger tracks are then reported to the trigger system for linking to the calorimeter and/or muon systems. Because this "processing" is done in parallel across the entire tracker, the time needed can be very short, typically less than 100 ns.

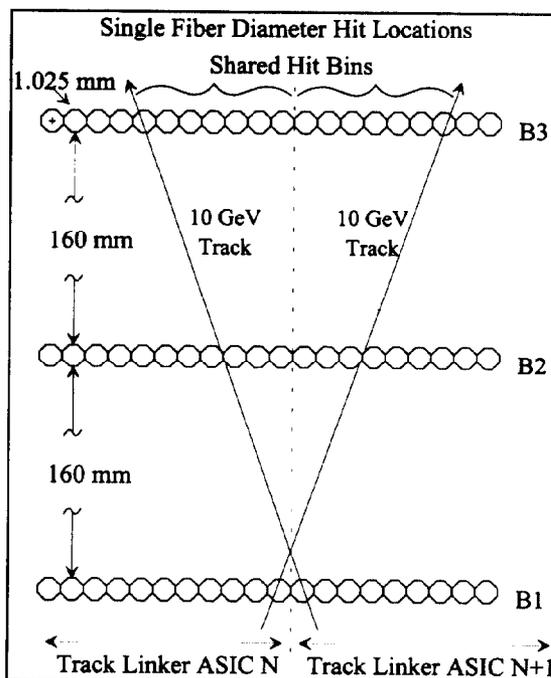


Figure 7. Triplet of superlayers used for SDC Trigger.

The combinatorial AND-OR logic of the segment linker can be designed to be remotely programmable within certain limits. Hence as luminosity increases or the demands on the trigger change, trigger thresholds can be changed dynamically to

increase the effective P_T threshold. As with the segment finder, the complexity and cost of the segment linker grow rapidly as the symmetry of the tracker is broken.

4. Tracking System Geometries

Detector geometries can have very strong effects on the performance and cost of the tracking system. Once geometries are fixed, many of the parameters of the electronics are constrained. For this reason, these geometries must be investigated as to their impact on other parts of the system before they are frozen. Once frozen, these geometries are "hard wired" into the system. The layer separation and fiber spacing both contribute to this "hard wired" information. They also affect the designability of the electronics systems. Figure 8 shows three possible barrel tracker trigger superlayer configurations. Each of these has different performance capabilities. Each of these will be discussed briefly.

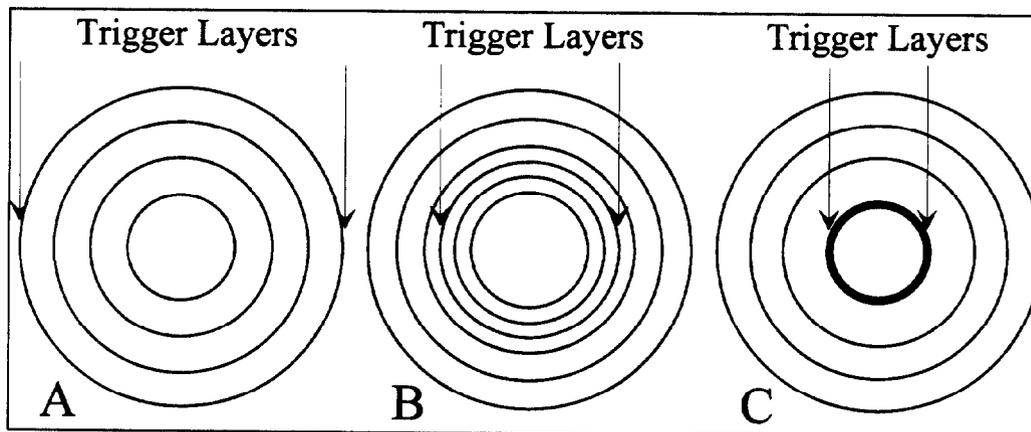


Figure 8. Various options for trigger superlayer in a barrel tracker.

4.1. Trigger Requirements

Option A has the greatest span in trigger layer spacing and so has the sharpest trigger threshold. This larger trigger lever arm also implies that the number of interconnections which cross Φ boundaries is greater. Since more fibers participate in each Φ section, this configuration is also more susceptible to fake tracks. The "search paths" over which the electronics must look for tracks are wider and thus random hits are more likely to satisfy the track conditions for a trigger.

Option C has the smallest trigger lever arm and its trigger threshold would be fairly "soft". However, since the layers are very closely spaced, it has the smallest search paths for the trigger and so the number of fake tracks would be reduced and the number of interconnections is the smallest of the three options.

Option B is a compromise between A and C. This option most closely matches that chosen for SDC. The trigger layers are as closely spaced as can be and yet provide

the required trigger threshold sharpness. As the reader can see, there are many parameters which interact to determine the overall system performance.

4.2. Electronics requirements

In order to avoid cracks or areas where the trigger is inefficient, all of the layers must communicate correctly with each other. In a system such as that designed for SDC, which has ~600,000 active fibers, the system must reside in a reasonable number of circuit boards ~1000. In order to design a system of this size which has hermetic trigger coverage, we must have a scheme which allows for the interface between each circuit board's area of coverage to be correctly handled for the trigger. To be affordable and maintainable, there must not be 1000 unique circuit boards, but rather a single species of board duplicated 1000 times. This requirement implies that a symmetry be created and maintained in the system so that each board provides a region of coverage that is the same for all boards, and that all circuit board boundaries are the same. Since the trigger is only using R-Phi, it is logical to create and maintain a symmetry in the Phi coordinate. Thus, each circuit board will cover a Phi slice of the detector as shown in figure 4.

These requirements provide some constraints on the detector configuration. If each circuit board is to cover a Phi slice of the detector, all Phi slices must be the same. This implies that superlayer spacing and fiber spacing or diameter must be adjusted to create and maintain an X-fold symmetry, where X is the number of trigger circuit boards in the system. In this way, all trigger boards are the same and a given board's position within the system is not important. This means that any board can be plugged into any slot and that maintenance is relatively easy, since a spare board is a spare for any slot. If this method can not be followed, then each slot is unique and the user is faced with a system which has X different boards and where X different spare boards are needed. This would create a system which is neither affordable nor maintainable. Indeed, for the SDC solution, we not only maintained this symmetry to the board level, but to the ASIC level as well.

4.3. Connector Issues

Once the symmetry is created in the detector as described above, it then falls to the interconnect system to bring the required signals into each of the trigger boards in the same way for all trigger boards. This can most easily be accomplished in the clear wave guide fibers which bring the light signals from the scintillating fibers to the VLPC cassettes. If one creates a Phi symmetry as shown in figure 9, where each layer's contribution to the Phi section is a multiple of N fibers, then the task of signal routing is greatly simplified.

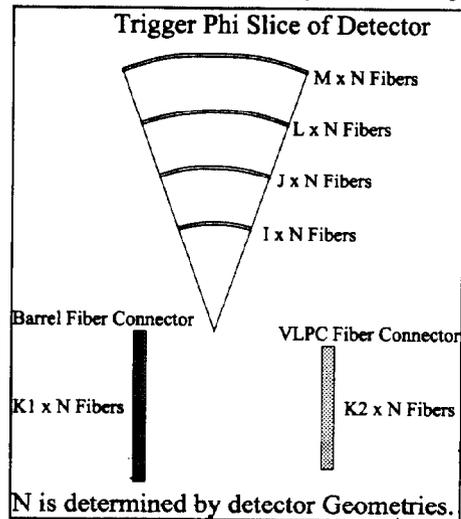


Figure 9. Phi symmetry and connector possibilities

It is possible to make larger than N connectors for both the fiber ribbons on the detector and for the VLPC cassette connections. The only requirement is that these be again in multiples of N. This scheme has many advantages in that all of the clear wave guide fiber bundles are the same. This leads to ease in manufacture and makes availability and replacement of spares very easy.

The alternative to creating and maintaining this symmetry is a system where $N=1$ and every fiber must be placed into the correct VLPC slot by hand. This system would not be affordable or maintainable.

4.4. U and V Stereo Layers

As can be seen from the preceding arguments, the number of interconnects can grow very rapidly into a system which cannot be built. This is the situation if one tries to make a trigger using the stereo layers. Each U fiber crosses a great many V fibers and the number of interconnections needed to make a trigger would be larger than the number of fibers. For this reason, the stereo fibers are not used in the trigger.

The U and V layers for the Scintillating Fiber Tracker do not participate in the trigger for Level 1. However, these fibers must still be readout as part of any event. This is accomplished in a very straight forward way using the same PC boards as are used for triggering. Up to 1024 fibers from the U and V layers are input into a card, as are the axial fibers. The Level 1 storage ASICs are used to provide the trigger delay storage and DAQ interface for these fibers. The only difference is that the segment linking ASICs are not installed on this board and no trigger system fiber-optic link is provided. These fibers are then treated identically with the trigger fibers as far as Level 1, Level 2, and DAQ buffering are concerned. By simply not loading the trigger specific ASICs we can use the same board design and eliminate extra design stages.

4.5. Z Coordinate Trigger

However, as was mentioned earlier, it is possible to get Z information for the trigger from the axial fibers. This can be done in either of two ways. The first method would be to use timing information on the arrival of the light signals at the VLPC cassette, this would give the Z coordinate by measuring the "time of flight" of the light from the particle crossing the scintillating fiber. Many experiments use this technique for other types of detectors and commercial electronics are available with sub-nanosecond timing resolutions.

The second approach to getting Z information is less precise but may be substantially cheaper. This method would use several light level thresholds to determine, from the amount of light generated and transmitted, the approximate Z coordinate. The closer to the near end of the fiber, the greater the light and the farther away the less light there would be. This approach is by its very nature less accurate than the time of flight approach.

These two methods differ in their cost and precision, and it is up to the user to decide which method provides the required trigger precision. These are only needed if

the user requires a high speed trigger which requires the Z coordinate as part of the trigger.

5. Test Beam Electronics

As a proof of principle exercise, a 128 channel fiber trigger and readout board was designed. A block diagram of this board is shown in figure 10. This 128 channel digital readout board incorporates Level 1 storage for 2048 beam crossings and track segment finding algorithms. The results of the track segment finder is stored in a pipeline on the board so that off-line analysis can be used to "fine tune" the tracking algorithms. These algorithms are implemented in electrically erasable PALs which will allow the study of track finding efficiency and the percentage of false tracks. This is accomplished by reading out the raw track hits and the results of the track finder which are also stored on board. The track finder section of this board also has "trigger" outputs so that it may be used as part of a test beam trigger.

This board was successfully used in a scintillating fiber test beam effort at Brookhaven National Laboratory.

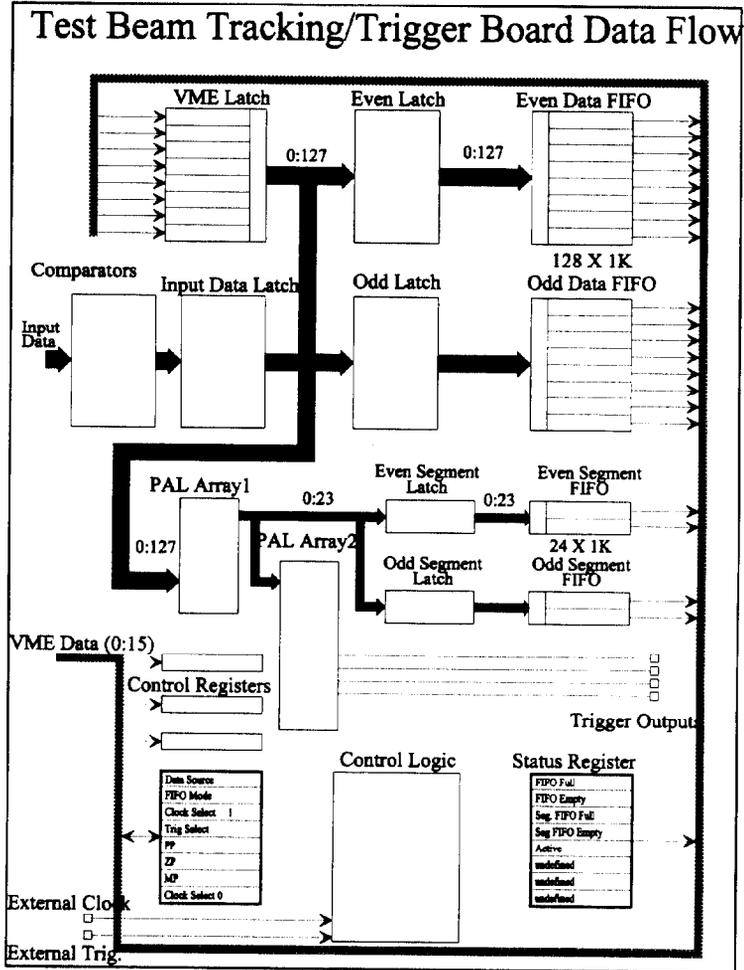


Figure 10. Block diagram of prototype readout and trigger card used in BNL test beam experiment.

6. Conclusions

It is hoped that the reader will now have a better understanding as to the ways in which different systems interact to make or break a working system. All subsystem providers to a larger system must cooperate to create an architecture which satisfies all system requirements without putting too great a burden on any one subsystem.

7. Acknowledgments

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