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FASTBUS Readout System for the CDF DAQ Upgrade

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Abstract

The Data Acquisition System (DAQ) at the Collider Detector at Fermilab is currently being upgraded to handle a minimum of 100 events/sec for an aggregate bandwidth that is at least 25 Mbytes/sec. The DAQ System is based on a commercial switching network that has interfaces to VME bus. The modules that readout the front end crates (FASTBUS and RABBIT) have to deliver the data to the VME bus based host adapters of the switch. This paper describes a readout system that has the required bandwidth while keeping the experiment dead time due to the readout to a minimum.

I. INTRODUCTION

For the next run, the Data Acquisition System at the Collider Detector at Fermilab will have at least 100 events/sec going to the Level 3[1] processor farm. The processor farm consists of a number of Silicon Graphics computers that will 'build' events from the many data fragments that are sent to them through a commercial switching network. The switch is manufactured by UltraNet Inc. and can interface to the VMEbus through 'host adapter' modules that are VMEbus sequential transfer masters. This works well at the Level 3 end of the DAQ System, since Silicon Graphics computers have high performance VMEbus slave interfaces. On the front-end FASTBUS and RABBIT crate side, however, the data has to be gathered and made available to the switch's host adapters.

The FASTBUS readout is accomplished by a set of 5 modules and two interconnect schemes. The modules are A) a FASTBUS Readout Controller[2] (FRC), B) an FRC Auxiliary Card (FRCAC), C) a VME/VSB bus CPU (Scanner), D) a dual ported VME/VSB memory card and E) a Scanner Auxiliary Card (SCAC). The interconnect schemes are A) VSB bus that connects the Scanner and the SCAC and B) Scanner bus that connects multiple FRCACs to the SCAC. Figure 1, which is a partial block diagram of the readout system, illustrates the scheme. The rest of the paper describes these components in detail.

II. COMPONENTS

A. FASTBUS Readout Controller (FRC)

The FRC reads out data from modules in its crate on demand. The demand comes from the Trigger Supervisor as a FASTBUS message or as a signal through the trigger interface card. An FRC consists of a 40 MHz 32-bit RISC

CPU, 1 to 4 MBytes of triple ported video RAM, full IEEE Std. 960-1986 ANSI/IEEE FASTBUS interface, a Scanner bus (described later in this paper) interface, diagnostic/boot PROMs, two RS-232 ports, a real time clock with static RAM, an ethernet interface with 32 (or 128) KBytes of dual ported static RAM, a dot matrix display and a trigger interface.

The memory design of the FRC is optimized for block data transfers on the FASTBUS and Scanner bus. The triple ported video RAM allows data to flow from the FASTBUS to the memory, while data is simultaneously readout by the Scanner bus. In addition, the CPU has complete access to the data read from the modules in the crate. The FRC contains DMA controllers for both FASTBUS and Scanner bus ports.

Programs can be downloaded into the FRC's memory through Scanner bus, FASTBUS or ethernet. The FRC contains enough resources to implement a real time operating system.

B. FRC Auxiliary Card (FRCAC)

The FRCAC is the FRC's interface to the Scanner bus. The data prepared by the FRC is readout by the Scanner through the FRCAC. The FRCAC plugs in the back of the FASTBUS crate at the slot occupied by the FRC. The FRCAC contains two communication registers called Scanner Command Register and FRC Status Register for diagnostic purposes and a Broadcast Register and a Transfer Count Register for normal operations.

C. VME/VSB CPU (Scanner)

The Scanner initiates data transfers on the Scanner bus but does not participate in the actual transfers. It interfaces to the VME Host Adapter of the UltraNet switch. Its function is to make the data (from all the FRCs attached to it) available to the Host Adapter. The requirements on the Scanner are that it should be a VME bus master and slave (32-bit data transfers). No block transfer capabilities are needed. It should be a VSB bus master (32-bit data transfers). No, VSB block transfer or slave capabilities are required. It should, however, be an interrupt handler on both busses. The most important requirement is that it has an UltraNet driver. In our system, this is a commercial product.

D. VME/VSB Dual Ported Memory

The Dual ported Memory is the storage for the data read from the FRCs. The requirements on this module are that it is a fast block transfer (32-bit data) slave on both the VME and VSB busses. In our system, this is a commercial product.

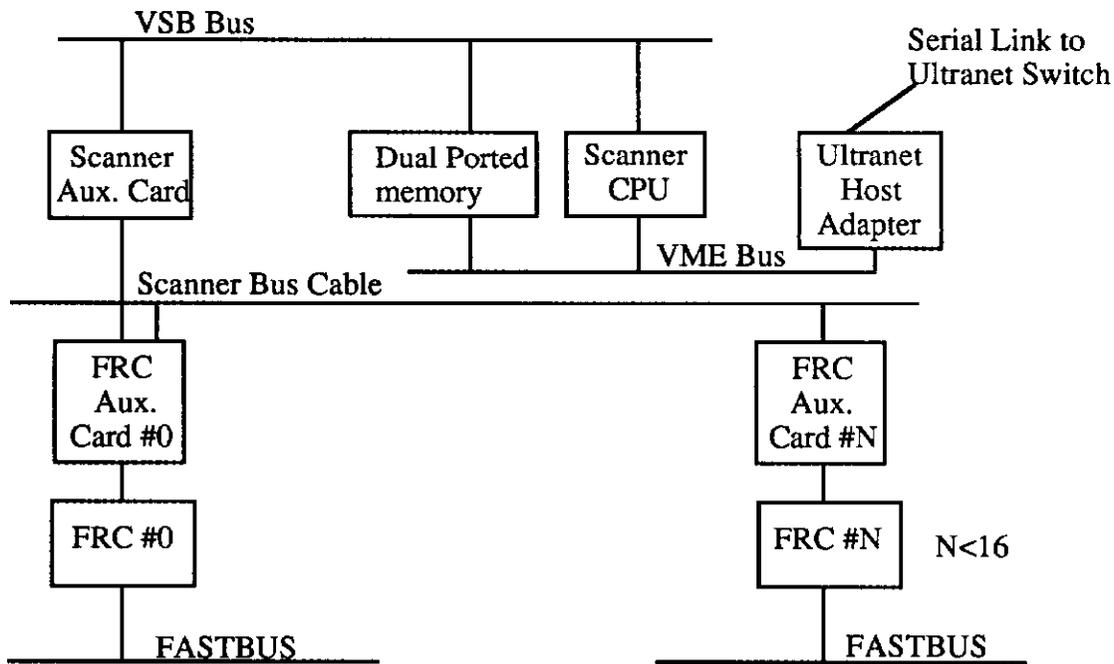


Fig. 1 Partial Block Diagram of the FASTBUS Readout System

E. Scanner Auxiliary Card (SCAC)

The SCAC reads data from the FRCs attached to it and writes that data into the VME/VSB dual ported Memory. The SCAC is a VSB bus single and block transfer slave and VSB bus block transfer master.

The SCAC contains a VSB Address Register, a Status Register and an address FIFO. The VSB Address Register contains the address at which the SCAC stores data read from the FRCs. The Status Register contains the status of the VSB and Scanner bus transactions. The address FIFO holds addresses of up to 16 FRCs to be readout. This eliminates the need for the Scanner to initiate data transfers for each FRC individually. The SCAC contains data FIFOs to hold data sent by the FRCAC. These FIFOs can be used by the Scanner for diagnostics.

III. INTERCONNECTS

A. VSB Bus

The VSB bus connects the Scanner, the SCAC and the VME/VSB dual ported memory. This is a commercial bus.

B. Scanner Bus

The Scanner Bus connects up to 16 FRCs (through the FRCACs) to one Scanner (through SCAC). The Scanner Bus implements differential RS-485 protocol and is optimized for block transfers of data. Scanner bus transfers begin with the Scanner addressing an FRC and receiving an address

acknowledge from the selected slave. Data transfers begin with the Scanner sending either data strobes during writes or a read signal during reads. During read cycles the FRCAC sends data and data strobes to the SCAC. The Scanner bus also implements broadcalls (explained in section IV). The Scanner Bus allows the Scanner to reset and reboot any of the CPUs on the FRCs attached to it.

IV. OPERATION

Readout begins when the Trigger Supervisor broadcasts a FASTBUS message or the Trigger Interface card receives a signal. The FRC reads data from the modules in its crate and stores the data in its memory along with a header. In addition, the FRC sets up the memory address where this data is stored and writes the word count in the Transfer Count Register of the FRCAC. The act of writing to the Transfer Count Register causes an interrupt to be set on the Scanner bus. This interrupt is translated into a VSB bus interrupt by the SCAC. The Scanner bus interrupt line is a single line used by all the FRCACs. The Scanner does a broadcast operation on the Scanner bus to find out the sources of interrupt. In response to the broadcast operation, a participating FRCAC places a logic one on the Scanner bus data line that corresponds to its Scanner bus address. Thus, the Scanner can know in one bus cycle how many FRCs to read. The Scanner prepares and writes the addresses of the FRCACs Address FIFO of the SCAC. The Scanner also writes the target VSB address into the SCAC's VSB Address Register and instructs the SCAC to do Scanner bus data transfer cycles. The SCAC assumes the mastership of both Scanner bus and the VSB bus. The SCAC gives up VSB mastership at the completion of data transfers from every FRC and pops the address FIFO. It then reassumes VSB mastership for the next FRC reads. These operations

continue until the Address FIFO is emptied, at which time the SCAC interrupts the Scanner. The Scanner and the FRC are involved only in the beginning of the data transfers and do not participate in the data transfers.

The Status Register of the SCAC is capable of latching a number of error conditions. These are: a) VSB slave time-out, indicating no response from the VME/VSB dual port memory (when addressed by the SCAC), b) VSB Error (including time-outs), c) Scanner bus Address Broadcast time-out, d) Scanner bus data transfer time-out, e) Scanner attempt write to a full address/data FIFO of the SCAC and f) Scanner attempt to read an empty address/data FIFO of the SCAC. On any error condition, a VSB bus interrupt is generated.

V. CONCLUSIONS

The FASTBUS Readout System is a modular design that uses commercial equipment and industry standards wherever possible. The design effort is limited to that which is not commercially available. The design implements a number of diagnostics features for use in system debugging. Special attention is paid to streamline the data transfer operations for maximum throughput. The intelligent modules in the system are relieved of data transfer functions in order that they may be better used for other important tasks.

VI. ACKNOWLEDGMENTS

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VII. REFERENCES

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