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**E. Hartouni, D. Jensen, B. Klima, M. Kreisler, S. Lee,
K. Markianos, M. Nordberg, M. Rabin, J. Uribe and D. Wesson**

*Department of Physics and Astronomy, University of Massachusetts,
Amherst, Massachusetts 01003*

**M. Church, A. Gara, E. Gottschalk, R. Hylton,
B. Knapp, W. Sippach, B. Stern and L. Wiencke**

Columbia University, Nevis Laboratories, Irvington-on-Hudson, New York 10533

D. Christian, M. Etchegoyen, G. Gutierrez, S. Holmes, J. Strait and A. Wehmann

Fermi National Accelerator Laboratory, Batavia, Illinois 60510

C. Avilez, W. Correa, J. Felix, H. Flores, G. Moreno, M. Romero and M. Sosa

Instituto de Fisica, Universidad de Guanajuato, Leon, Gto., Mexico

M. Forbush, F. Huson, J. White and J. Wightman

Department of Physics, Texas A&M University, College Station, Texas 77843

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Photomultiplier Signals*

E.P. Hartouni, D.A. Jensen^(a), B. Klima^(a), M.N. Kreisler, S. Lee, K. Markianos,
M. Nordberg^(b), M.S.Z. Rabin, J. Uribe, and D. Wesson

Department of Physics and Astronomy, University of Massachusetts,
Amherst, Massachusetts 01003 USA

M. Church^(a), A. Gara, E. Gottschalk, R. Hylton^(c), B.C. Knapp, W. Sippach,
B. Stern^(d), and L. Wiencke

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C. Avilez^(e), W. Correa, J. Felix, H. Flores, G. Moreno, M. Romero, and M. Sosa

Instituto de Fisica, Universidad de Guanajuato, Leon, Gto., Mexico

M. Forbush^(f), F.R. Huson, J. T. White, and J.A. Wightman

Department of Physics, Texas A&M University, College Station, Texas 77843 USA

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and the CONACyT de Mexico.

- a) Current Address: Fermilab, Batavia, Illinois 60510
- b) Current Address: North Chelmsford, MA 01863
- c) Current Address: IBM Research Laboratories, Yorktown Heights, New York 10598
- d) Current Address: AT&T Research Laboratories, Murray Hill, New Jersey 07974
- e) Deceased
- f) Current Address: DESY, Hamburg, Germany

Abstract

A modular system to provide high speed simultaneous measurements of pulse area and time-of-flight for photomultiplier signals is described. By requiring a minimum pulse size and a time-of-flight signal within a gate before recording either measurement, the system achieves several advantages over other techniques. In particular, since no time is wasted reading channels without useful information, readout speed is enhanced. The system permits accurate measurements at rates exceeding 10 MHz per channel and can be read out without excessive deadtime at rates up to approximately 100 KHz. Data storage problems are also reduced. Both pulse area and time-of-flight are measured using 128 bins (7 bits). Costs are less than \$40 US per channel. Other advantages and design features are discussed.

One of the challenges facing experiments in elementary particle physics is dealing with both very large numbers of detector elements and ever increasing interaction rates. For every interaction of interest, each element must be interrogated, its information digitized, and read out to a data storage device. This process must be rapid enough to avoid significant reductions in the live-time of the detector. In a program of experiments (BNL E766¹/FNAL E690²) studying hadron interactions at megahertz rates, we have developed a spectrometer system³ which addresses this challenge. In this paper, we present the details of one of the sub-systems of that spectrometer -- the high speed simultaneous measurement of pulse area and time-of-flight for photomultiplier signals.

The design of this pulse height and time system, the PHT system, was driven by the desire for both measurement accuracy and readout speed, was limited by the constraints of overall system cost, and guided by a philosophy to produce systems with capabilities well matched to the measurement requirements of the experimental program. Once reaching that goal, the design is not pushed, often reducing cost and complexity.

An essential feature of the resulting design is the simultaneous nature of the pulse area (ADC) and time-of-flight (TDC) measurements. For a given channel, the ADC and TDC measurements were made only if: (1) the pulse height was above a threshold and (2) there was a coincidence between the TDC signal and the gate for that channel. If either of these conditions were not satisfied, neither the ADC nor the TDC information for that channel was digitized or read out. This suppression of channels with zeroes or non-useful information is accomplished using discriminators in the photomultiplier bases rather than by discrimination in the ADC's or by pedestal subtraction after digitization. This method allows the use of very low thresholds since the discrimination is performed before the signals have been degraded by transit over long cables.

The ADC and TDC measurements in channels with useful information are digitized using shared Wilkenson ramps with modest dynamic range -- 128 bins. Only those channels are then read out. The readout proceeds through a priority sequence in which channels are read out in a predetermined order without computer control and in which each measurement is labeled for later identification. Since only channels with information are read out and since the digitized information is contained in a

ADC section and all eight inputs to its TDC section simultaneously. This is done using a separate integration capacitor and comparator for every input and 2 shared reference capacitors and Wilkenson ramps - one for the ADC section, and one for the TDC section. Power (-5.2V, +12V, and -12V), data busses, air cooling, and local controllers are provided in crates which can house up to 128 channels. The cost of the complete PHT system is rather modest, averaging less than \$40 US per channel.

The digitization process for both the ADC and TDC sections of the PHT board begins with the arrival of a gate from external trigger logic. The gate, typically a 25ns wide ECL level pulse, initiates acceptance and processing of digital time and analog pulse area signals. Signals which arrive outside the gate are not processed. This gate is driven differentially to a 10H116 for each channel.

The digital time-of-flight signals, also differentially driven ECL level pulses, are carried to the PHT board over 17-pair twist and flat cables. These signals arrive at the same 10H116 while the gate is present. Figure 3 shows the time-to-digital conversion section of the PHT board. The signal output from the 10H116 is wire AND-tied to the 10H116 gate output (low true). The combination of these signals is logic high unless both are low.

The gate-signal combination is used as the input to another buffer on the 10H116. The complementary outputs of this buffer are connected to the bases of a transistor differential pair to control integration. The current from a ~5mA current source is sent through a direct path across one transistor to ground when the input to the buffer is high (no gate or gate with signal). When the input is low (gate without signal), the current is directed across the other transistor of the pair to a 50pF integrating capacitor. The capacitor charges only when there is a gate without a signal, so the time is measured with respect to the start of the gate. Note that the gate-signal combination also excludes noise outside the gate, since a low level initiates integration. Channels without a signal integrate for the entire width of the gate yielding the maximum possible voltage on the capacitor.

After the capacitor charges, the voltage for each channel is held constant and is used as one input of a comparator. The complementary input is tied to a voltage reference, a single Wilkenson ramp. This is supplied by a similar integration circuit. However, the current source for this circuit supplies only ~0.1mA, so the integration rate is about 1/50th that of the signal. The output of the comparator is ECL low unless the voltage ramp exceeds the voltage of the integrated signal. When the two voltages are equal, the output swings high. Since channels that do not contain data integrate for the entire gate, the ramp is designed never to exceed the integrated signal of these

the read cycle, the Q3 output of the priority decoder goes low. This generates a logic signal to the system that the board is ready for the next gate.

Studies of the performance of the PHT system were made in a test stand⁶ constructed for that purpose. In that setup, the behavior of the TDC section was investigated by repeatedly adding 1ns delays to the TDC input signal. As expected, these studies showed some small non-linearity of the TDC for times near the beginning of the ramp due to the finite time response of the current switch. This posed no problem for our needs. The time-of-flight measurement range used in the experiment was selected to avoid that portion of the ramp. The linearity of the rest of the ramp was quite adequate.

These test stand studies were augmented by calibrations of the 240 channel system measured in place during the experiments. A precision computer controlled pulser was used to generate a start and stop pulse. The time between these pulses could be adjusted in 51.3 ps steps. The start pulse was used as the external trigger to generate the gate for the PHT boards. The stop signal was used to generate the ECL digital input signal to the TDC section of the PHT board, thereby simulating the signals received by the system in normal operation. All 240 channels were tested. By performing a linear fit to the data from each channel, we obtain an average slope of 0.127ns/bin. The channel to channel variations in the slopes were quite reasonable. The distribution of slopes for the 240 channels had a half width half maximum of 0.008ns/bin.

The calibration of the pulse area measurement was studied using the test stand. By attenuating an input pulse from a photomultiplier, the pulse area or charge on the integrating capacitor needed to produce a one bin change in the ADC reading could be determined. Typically, a charge of 0.31 pC produces an output change of one bin.

Since zero suppression was done using a discriminator in the phototube base, it was possible to make meaningful measurements of very small pulses. The discriminator thresholds were set low enough that good time measurements were made even for the smallest signals -- a few mV at the peak and roughly 5 ns wide. For some of the Cherenkov counter photomultiplier tubes in the spectrometer, the pulse height spectra for one photoelectron signals were not separated from the ADC pedestals. Yet, the efficiency of the measurement of such signals was ~100%.

The effects of power supply voltage variations were also studied. The PHT board requires three supplies; -5.2V, +12V, -12V. No effect on the performance or calibration of either the ADC or TDC measurements could be observed when the regulation on these supplies was kept within the following limits:

$-5.2 \pm 0.1V$, $+12 \pm 0.2V$, and $-12 \pm 0.4V$.

The PHT board can be modified for other applications easily. For example, it would be straightforward to change the current 8-bit Gray code -- 128 bins with redundancy -- to 256 bins without redundancy. Also, the Wilkenson ramp circuit can be adjusted to set the size of a single bin for the TDC section. By changing the 39 K Ω resistor from +12V to the emitter of the 3640 transistor, the current for the ramp is modified and a new bin width is set. In the same manner, changing the 100 K Ω resistor for the ADC ramp circuit sets the bin size for that section.

We typically allow ten minutes for a newly powered PHT board to reach thermal equilibrium. If large variations in the temperature of the boards are possible, studies of the effect on the calibration would be advisable.

The system was used in two experiments in which more than 6 billion events were recorded. The PHT system proved to be quite reliable. When a channel died, it was almost always due to the failure of a JFET SD306 or one of the 10116's. Once the system was operational, failures were quite infrequent.

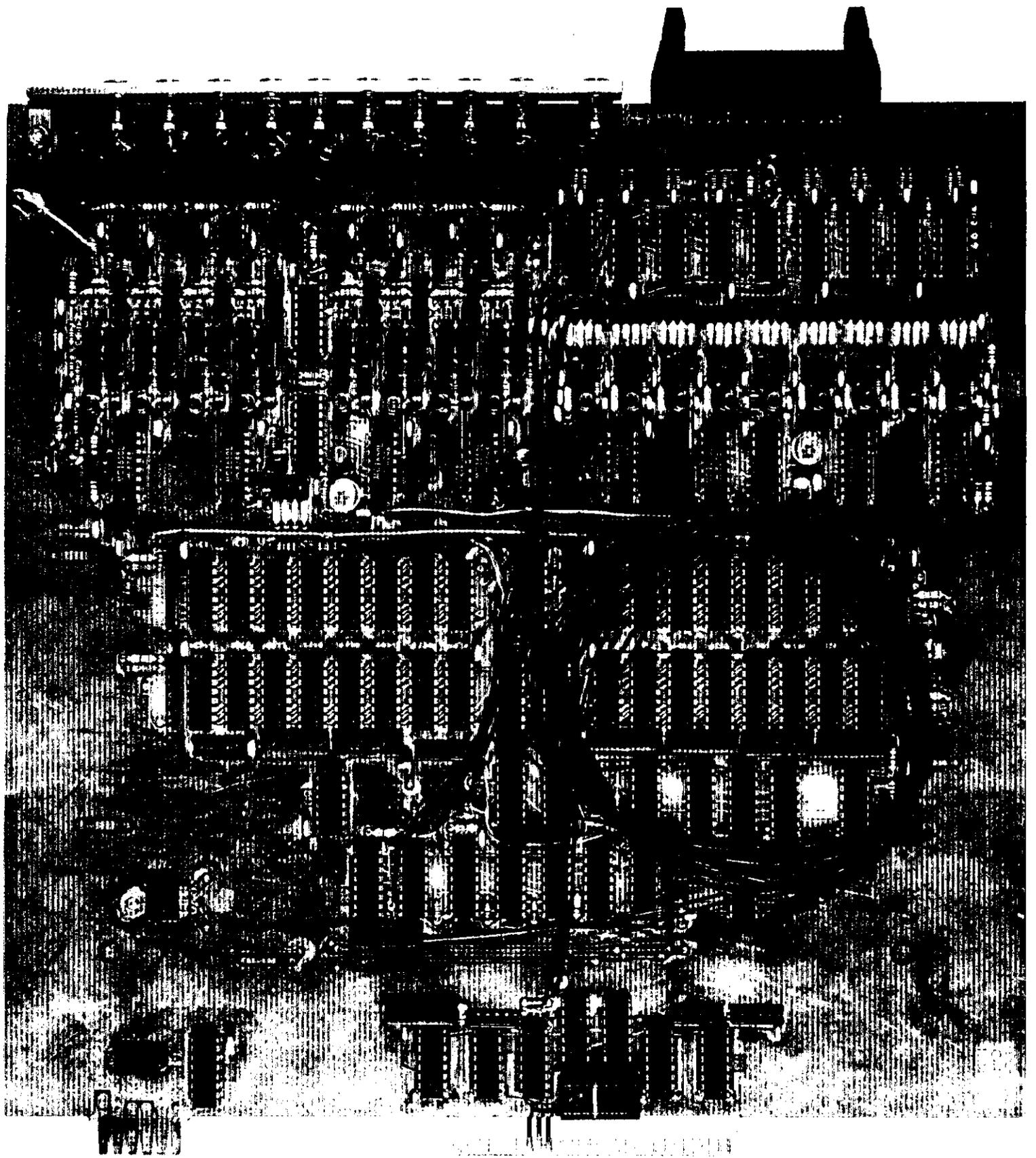
We would like to acknowledge the able assistance of the electronics technicians at the University of Massachusetts, Nevis Laboratories, and Fermilab.

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2. FNAL E690, "Study of Hadronic Production and Spectroscopy of Strange, Charm and Bottom Particles at the Tevatron", Columbia University, University of Massachusetts, Universidad de Guanajuato, and Fermilab collaboration, Fermi National Accelerator Laboratory, Batavia, IL 60510.
3. A description of the spectrometer is in preparation. See also: M. Church, " Ξ^- Production in 15-28 GeV Neutron-Proton Interactions", Columbia University Ph.D. Thesis, Nevis 260 (1986), Nevis Preprint R#1354; B Stern, "A Search for Charmed Particles in 15-28 GeV Neutron-Proton Interactions", Columbia University Ph.D. Thesis, Nevis 266 (1988), Nevis Preprint R#1386.
4. In BNL E766 and FNAL E690, both EMI 9954B and Amperex XP2262/H02 photomultipliers were used.
5. The photomultiplier system including the choice of tubes, the design and operation of the bases, the high voltage distribution system, and the latch electronics for this spectrometer will be discussed in a separate paper in preparation.
6. M.M. Nordberg, "Analysis of Time Measurement Resolution of the Brookhaven Experiment 766 PHT System", M.S. Thesis, University of Massachusetts (1988) unpublished.

Figure Captions

1. Sketch of the measurement technique.
2. Picture of the component side of an eight-channel PHT board.
3. Schematic of the TDC measurement circuit. Only one channel is shown for clarity. The PNP transistors are MPS3640 and the unmarked capacitors are 0.1 μF .
4. Comparator logic and suppression of channels with no data. As described in the text, digitization of the integrated data signal begins only when the voltage ramp equals that signal. When the channel does not contain data, that condition is not satisfied and no data is stored in the counters for that channel.
5. Schematic of the circuitry to perform the ADC measurement. Only one channel is shown for clarity. The PNP transistors are MPS3640 and the NPN transistors are MPS918. The unmarked capacitors are 0.1 μF .
6. Counter and latch circuits, including the Gray code generation logic.



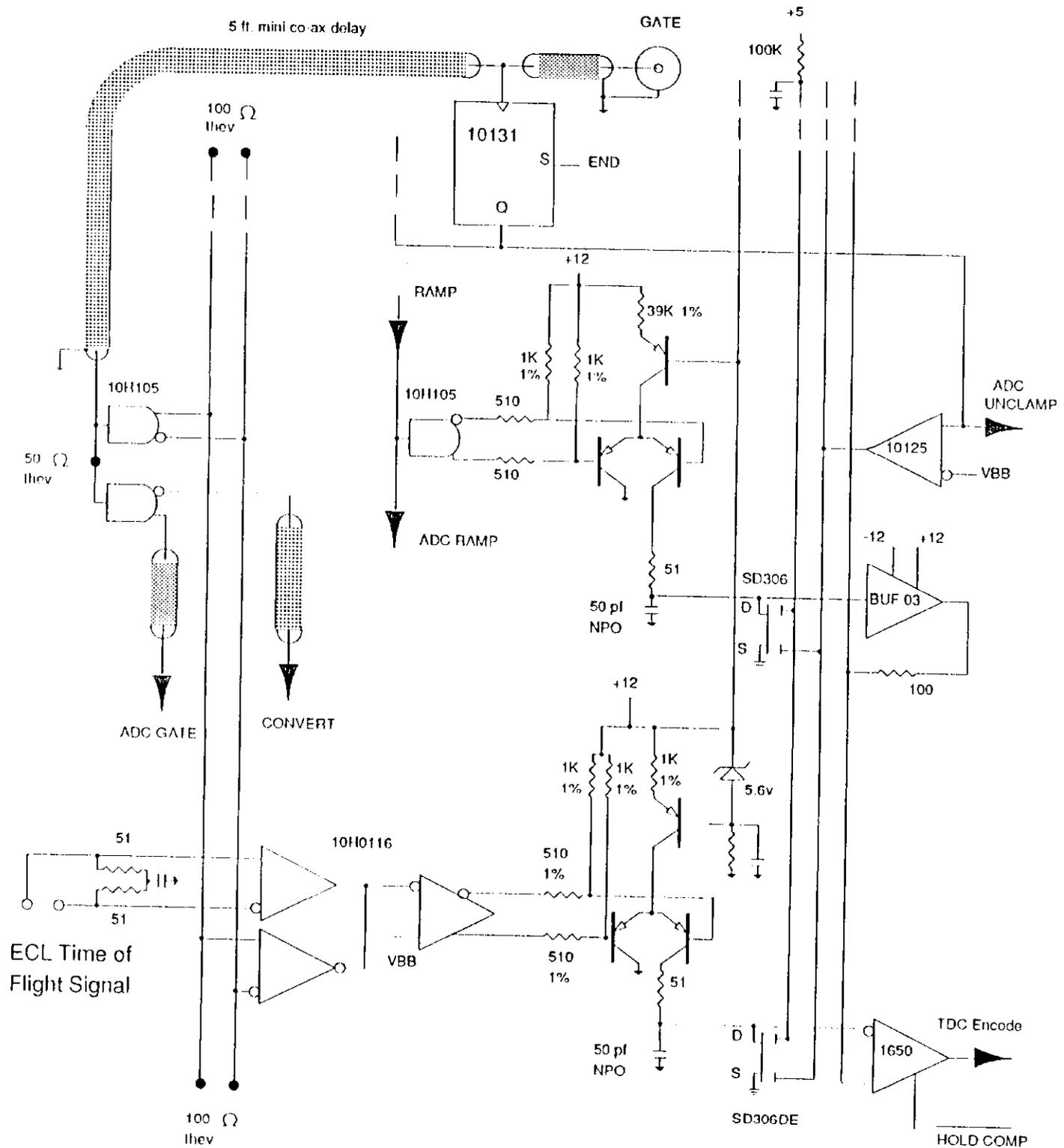


Figure 3

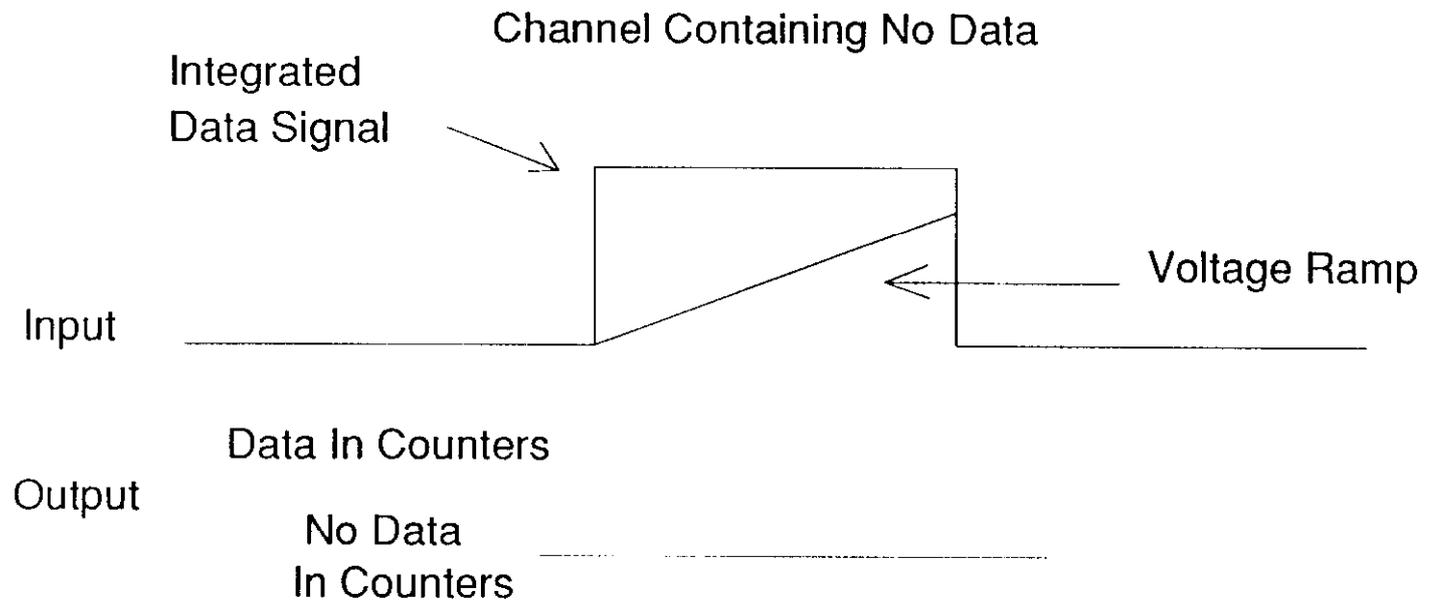
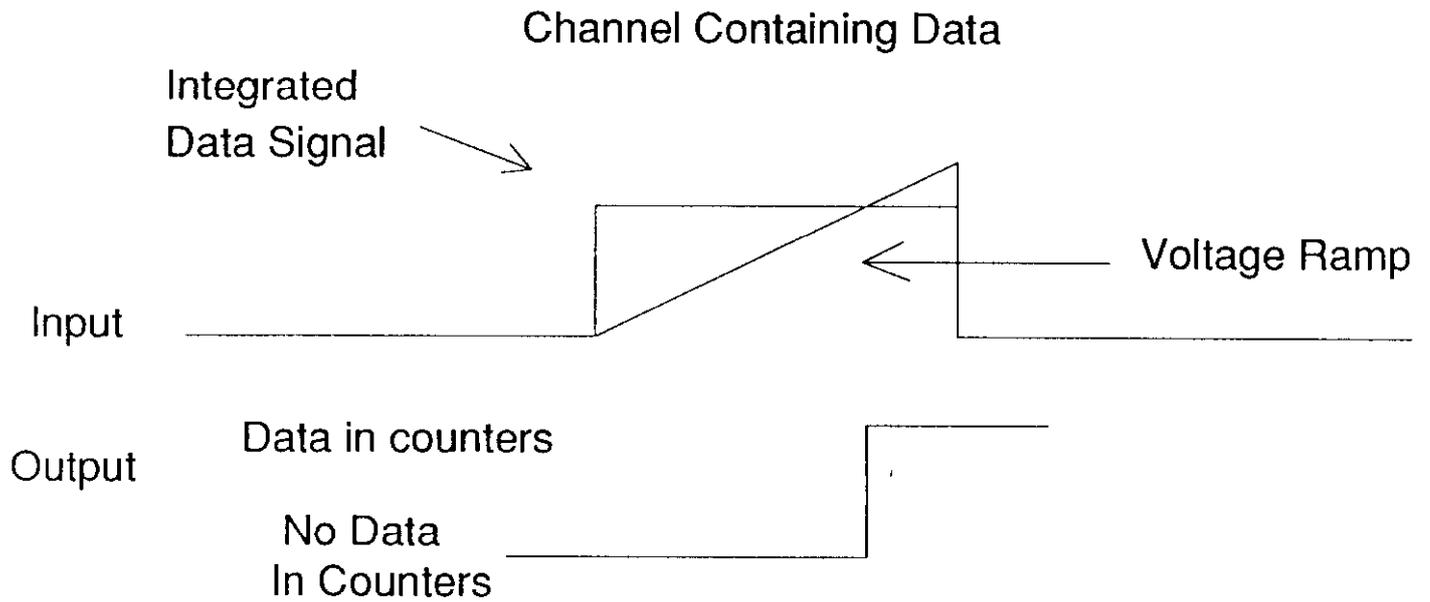


Figure 4

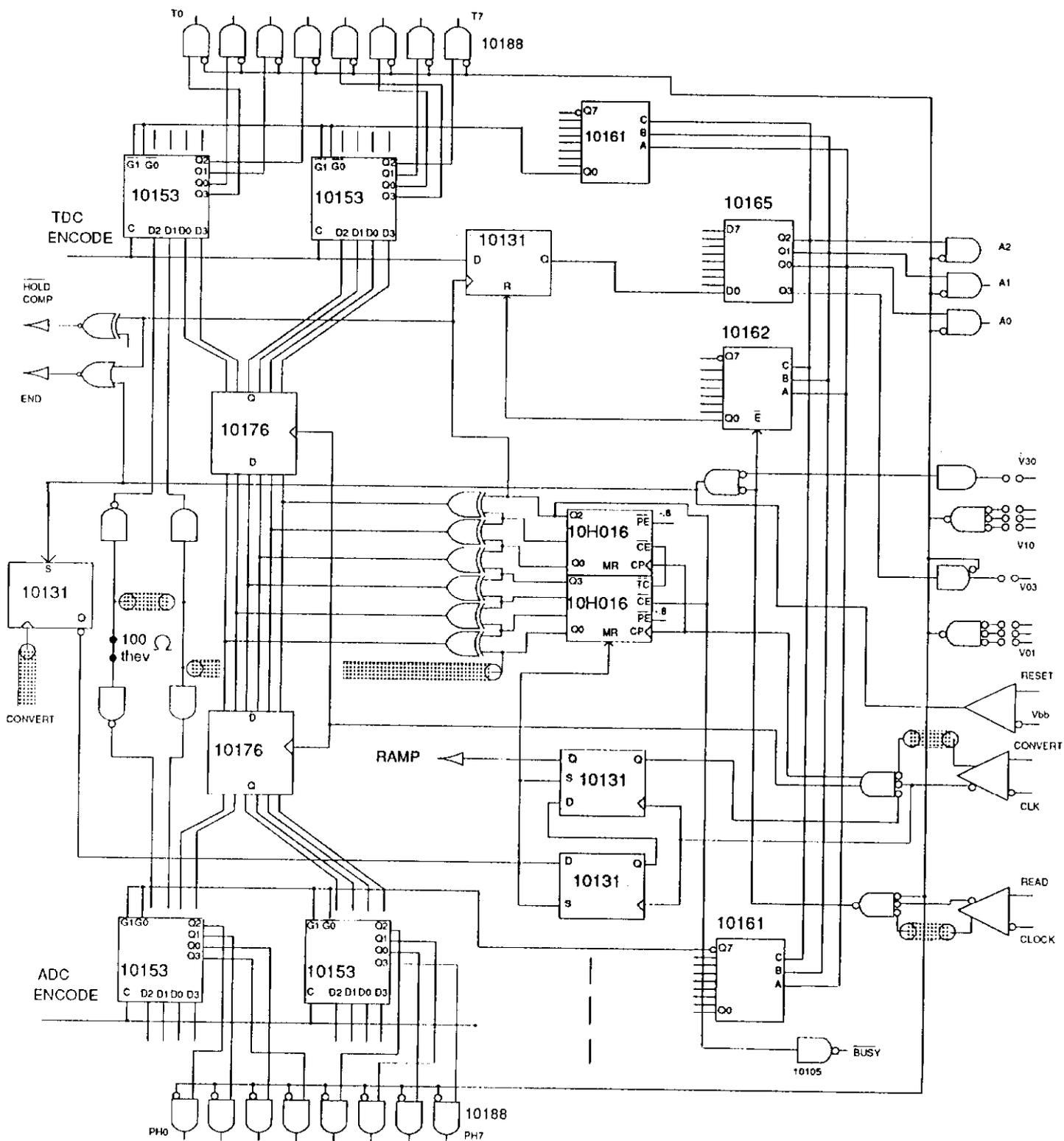


Figure 6