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Ruth Pordes, Mark Bennett, Terry Dorries, Margaret Haire,
Carmenita Moore, Gene Oleynik, and Margaret Votava
Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510 U.S.A.

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Software for FASTBUS and Motorola 68K Based Readout Controllers for Data Acquisition

Ruth Pordes, Mark Bernett, Terry Dorries, Margaret Haire,
Carmenita Moore, Gene Oleynik, Margaret Votava
Data Acquisition Software Group
Fermi National Accelerator Laboratory (*)

Abstract

Many High Energy Physics experiments at Fermilab are now including FASTBUS front-ends in their data acquisition systems. The requirements on controllers to readout and control these FASTBUS systems are increasing in complexity and speed. The Data Acquisition Software Group has designed general software for front end 68K processor boards housed in FASTBUS or VME to meet these needs. The first implementation has been developed for the General Purpose FASTBUS Master (GPM). This software is being ported to the FASTBUS Smart Crate Controller under development at Fermilab. The software is designed, using structured analysis tools and coding in C, to be easily portable in the future to new processor boards. As part of our extended support for FASTBUS, we have enhanced our software for the intelligent LeCroy 1821 FASTBUS interface and implemented the FASTBUS standard routines for the VAX/VMS operating system.

CONTEXT

Online systems at Fermilab now include many front end sub-systems, with modules in CAMAC, FASTBUS, VME or special purpose modules. Event sizes range from 200 to 200,000 bytes. Trigger rates range from 1 Hz to 10KHz. Data acquisition rates of several Megabytes/second are needed for the 1990 experiment run. Experiments now in the planning stage will require rates of ten to a hundred times this number.

VME based 68020 processor boards - developed for offline applications by the Fermilab Advanced Computer Project (ACP) [1] - are being incorporated to increase the available processing power and provide online software filtering of the acquired events. With the second generation ACP RISC processor modules [2] on the horizon, experiments are planning to incorporate them into their online systems to provide much enhanced event processing and data filtering capabilities.

GOALS

The data acquisition software groups develop and support readout and event acquisition software for experiments to satisfy their current and future needs. In the last two years there has been an increase in the data throughput requirements of the experiments we support, together with a significant increase in the number and variety of processors and intelligent modules in online systems. To address these issues we are developing a new data acquisition software system - PAN-DA [3].

We have selected a sub-set of available intelligent modules in VME and FASTBUS for development of full software and system support (Figure 1). We have designed PAN-DA software in a fashion which allows use of these modules in different experiment architectures and to satisfy differing specific requirements.

The software we have developed allows incorporation of these modules into existing data acquisition systems. An additional goal is to provide software packages that are easily transportable to new modules, whose hardware specifics are different but whose functional roles are similar to existing supported modules.

As part of PAN-DA, we are incorporating software tools for managing, synchronizing and debugging heterogenous systems incorporating many different hardware modules and front-end sub-systems, so that an "Online System" can be used as an integrated whole to acquire and analyze data.

PAN-DA software is designed to allow us to migrate support to new hardware technology as experiments incorporate such modules in their data acquisition systems.

FIRST IMPLEMENTATION OF PAN-DA SOFTWARE

Our first implementation of PAN-DA supports only Motorola 68K processors on FASTBUS and VME boards. The first modules to be supported are respectively

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the Struck GPM [4], the Motorola MVME133A-20, with additional support for incorporating use of the ACP/Omnibyte 68020 processor board.

Support for experiment written data processing code using the ACP software and hardware is provided in the ACP 68020 modules which are used to buffer events. Support for the FASTBUS Smart Crate Controller [5], now in prototype at Fermilab, is planned within the six months. Evaluation of the Cern CHI [6] and a VME based RISC processor board, the ACP II module, is also planned.

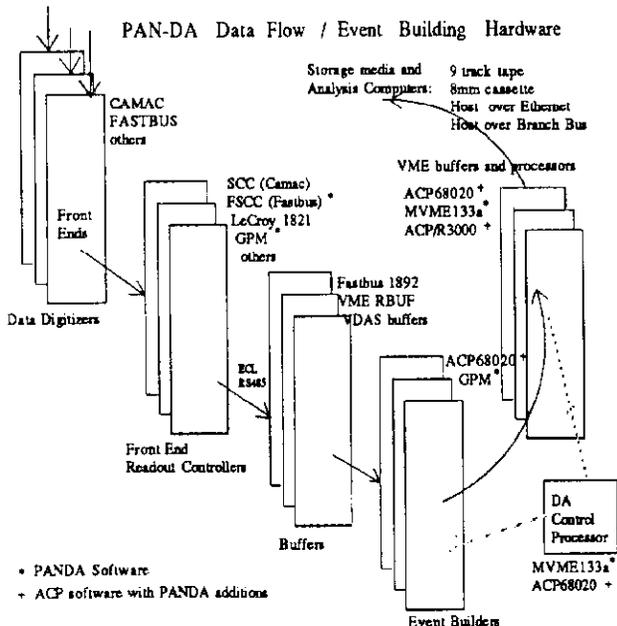
Data paths from CAMAC, FASTBUS, and VME are supported with data logging to conventional 9-track magnetic tape or 8mm cassette recording media from VME.

We use the Software Components pSOS multitasking kernel operating system. It supports a system debugger, system downloading, synchronization and multi-tasking services [7]. The VAX based Microtec cross-compiler tools are used for program development. All except time-critical code (which is written in assembler) is implemented in C. All software packages are designed using the Structured Analysis Structured Designed tool CADRE. Single centralized program sources are maintained, from which are generated the board specific codes.

Module, system control, initialization and monitoring rely on Remote Procedure eXecution (RPX) software developed by the Online Systems Group [8] for use over Ethernet (TCP/IP protocol) and serial line (RS232) using a simple connection oriented communications protocol.

ARCHITECTURES AND THROUGHPUT

Figure 1 shows a generalized picture of the event acquisition data flows and modules supported by the first implementation of PAN-DA and the existing VAXONLINE data acquisition systems.



This architecture supports effective data throughput rates for the following event builders of: 4 Mbytes/sec using the GPM, expectations of 10-20 Mbytes/sec using the FASTBUS Smart Crate Controller and 0.5 Mbytes/sec using the MVME133A-20 (This contrasts to a maximum possible throughput of 0.5 Mbyte/sec with our existing interfaces on a MicroVAX system.) Use of parallel crates for building and logging events, can provide multiples of these throughput values.

In a data "spill structure" environment, where events occur only about 30% of each minute, monitoring and diagnostic programs can be executed on particular sub-systems and/or modules during the interspill period, without compromising the overall data throughput or corrupting the main data path. The multi-master capabilities of FASTBUS, VME and auxilliary CAMAC controllers, allow software for the traditional "Q-bus to data acquisition bus" controllers to be used in parallel with the newly supported modules. PAN-DA provides a framework for user monitoring and diagnostic software to have access to all levels and modules in the system .

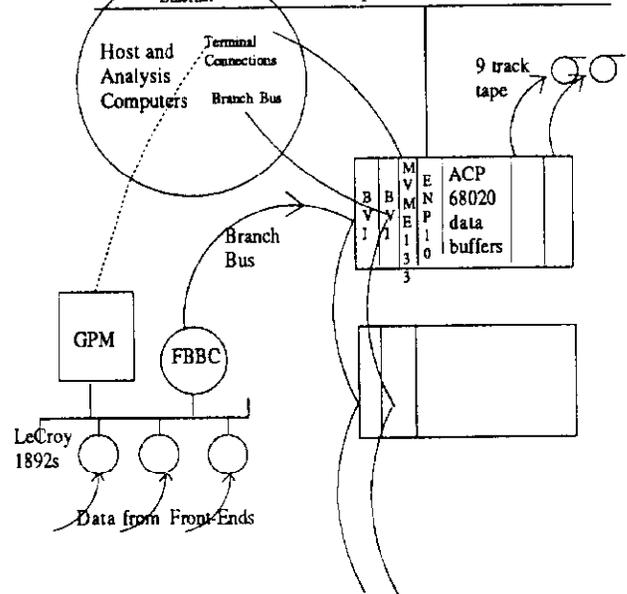
SPECIFIC EXPERIMENT CONFIGURATIONS

GPM Event Builder -

Figures 2,3 show system configurations currently planned for use with the supported modules and PAN-DA software.

In Figure 2, event building is done over the FASTBUS backplane by the GPM, with sub-systems supplying data from CAMAC, FASTBUS and "special box" systems. This provides an upgrade path for several existing experiments which previously buffered data in FASTBUS memories before building the events in a PDP-11 or MicroVAX.

PAN-DA Configuration Using the GPM for Experiment E687

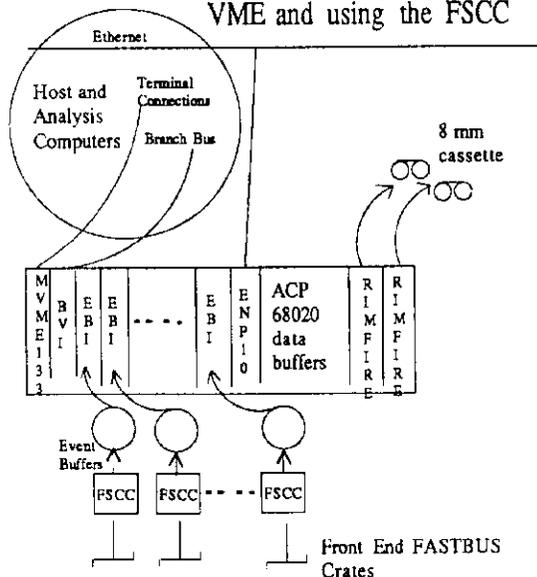


The GPM reads data from the FASTBUS memories and pushes the data through a FASTBUS to VME connection - the FASTBUS to Branch Bus controller - to buffers on ACP processor boards. The events are logged directly from VME simultaneously on two 9 track tapes. Use of the Branch Bus for transfer of the events allows data to be selectively sent to more than one VME crate as required. We will provide the software shortly, to fully support such a system for Fermilab Photoproduction Experiment 687.

Event Building Over VME -

Figure 3 shows event building being done over the VME backplane. Because of the dearth of VME Masters with fast DMA capability, the current event building rate per backplane of this architecture is limited to 1-3 Mbyte/sec. In addition, existing high speed VME crate interconnects - eg the HVE link - limit the number of VME crates that can be fed events. Hadroproduction experiment 791 will use the FASTBUS Smart Crate Controller to provide pipelined data readout from the front-end modules during the spill, and to push the data to large buffer memories for slower readout and event building in the interspill period.

Configuration with Event Building Over VME and using the FSCC



GENERAL PURPOSE MASTER (GPM)

The software provided for the GPM allows it to fulfill several different roles. It can be used as a FASTBUS event builder, front-end monitor and/or stand-alone FASTBUS host. Support for the GPM has been integrated into the extensions of pSOS which are provided as part of the PAN-DA software system. This provides a true multi-tasking environment for the application programmer such that, for example, several readout programs may be active concurrently each responding to different triggers for their processing. The extensions include system diagnostic tools for capturing a complete memory dump of the board and uploading it to a VAX/VMS system for offline examination in a non time-critical non-perturbative fashion. Figure 4 shows the internal software modules provided on the GPM.

We have ported the FASTBUS standard routines developed at Los Alamos for the GPM [9] to run under pSOS. We have extended the implementation to provide a C calling interface and to include assembly Macros to implement a sub-set of the standard routines (with the same parameter sequence and name as the standard routines). These allow FASTBUS operations to be executed with a minimum of software overheads, while allowing use of the parameter and error reporting software built into the existing routines.

A connection oriented communications software package over the terminal line is being implemented as part of the RPX package to allow control of the GPM (and any other modules with only RS232 as the control path) to be fully integrated with the other processors supported by PAN-DA.

We have coded a module independent data acquisition readout and control system (FEREAD) whose first implementation is for the GPM. Its overall structure is shown in Figure 5 [10]. FEREAD provides a framework for

- initialization and downloading of applications and run-time parameters from a VAX/VMS system
- synchronization of start and stop of data readout with the rest of the data acquisition system
- mechanisms for dynamic investigation of the status and statistics of the readout module
- execution of readout code in response to triggers
- inclusion of user specific data readout and processing programs. The system is designed to allow this to be as efficient as possible.

- pushing of event data through the output data port. The initial implementation provides for the data to be sent to VME buffers, part of the PAN-DA system.

This software - excluding the data I/O routines specific to the GPM - has been ported to the VME based Motorola MVME133A-20 - thus providing support for this module to read data and build events over the VME backplane as part of a PAN-DA system.

FASTBUS SMART CRATE CONTROLLER (FSCC)

Deficiencies in the functionality provided by the LeCroy 1821 [11] and GPM as event builders and readout controllers have been addressed in the design of a new FASTBUS readout controller - the Fermilab FASTBUS Smart Crate Controller (FSCC).

The FSCC, designed and built by the Fermilab Physics and Electrical Engineering departments to match the readout requirements of the new generation of FASTBUS front end modules (TDCs, ADCs [12]) being built at Fermilab, is now in prototype stage.

Although the LeCroy 1821 has a very high speed data input port and a 32-bit parallel output port that can support 20 Mbyte/sec output, it has limited processing capability - it has no arithmetic logic unit. For Experiment 706, which uses an 1821 to build events and send them to a Microvax for logging and analysis, this has been bypassed by using the GPM as a "friend" to the 1821. For each event to be read out, the GPM performs the initialization and cleanup operations. The GPM then triggers the 1821 to perform simple readout of the data to the Microvax.

The GPM has only a single high speed data port - its FASTBUS interface. In contrast, the FSCC includes two high speed data I/O ports - the FASTBUS backplane interface for data input and a simple 32-bit wide parallel data bus for output for which adaptor to a variety of existing buses (RS485, 1821/ECL, fibre-optic cable) are provided. The FSCC provides independent control of the ports by the on-board sequencer and 68020 processor, to give an overall throughput of approaching 20 Mbytes/sec (see Figure 6).

The FSCC includes an Ethernet interface. This allows for more reliable, higher speed control and parameter downloading of the module. It removes the distance and speed constraints imposed by only having an RS232 interface for control.

As a result of our prior experience in porting pSOS, we were able to successfully port the pSOS debugger at the first attempt with less than a weeks work. With the similar architecture of the FASTBUS interface with respect to the 68020 processor, we expect to be able to port the

FASTBUS standard routines from the GPM to the FSCC with a minimum of effort. In addition, FERREAD should port almost entirely without change to this new board. As part of our support for the FSCC, and consistent with the goals of the PAN-DA project, we are implementing a system independent portable implementation of TCP/IP, based on the Berkeley UNIX BSD 4.2 software [13]. It incorporates well defined call-outs for the system and interface dependent parts of the software. It provides user access to lower level - less overhead - ethernet protocols such as UP and raw ethernet. The software will include a user interface socket library common to that available in the VAX/VMS environment.

MODULE AND SYSTEM MONITORING

As discussed above, we emphasized the incorporation of module and system debugging and integration tools at all levels of the software - from the lowest operating system level, to the highest level centralized initialization and synchronization software.

In support of data, module and system monitoring and diagnosis of the front-end sub-systems and associated intelligent controllers, as well as to enhance support for MicroVAX based experiments, we have extended our VMS based software support for the LeCroy 1821 and the Jorway 411 controllers.

For the 1821 we have implemented the FASTBUS standard routines. Lists of FASTBUS operations to be executed, generated from calls to these routines, can include 1821 specific operations. The existing Fermilab list processing device driver for the LeCroy 1821 supports all functions required by the standard routines [14]. We are converting the diagnostic tool, DDL [15] to interface to this standard routine package. In addition, we are extending the functionality of the data readout portion of the Jorway 411 list processing device driver, to allow arithmetic and parameter operations to occur on the VAX as part of a CAMAC data readout list [16].

These enhancements extend the utility of the existing VMS based VAXONLINE data acquisition software [17].

FUTURE IMPLEMENTATIONS

The design and implementation decisions we have made for the first implementation of the PAN-DA software system for front end processor modules, event builders and data movers, puts us in a position to provide software support for new and more powerful boards. In the near future, the commercial availability and enhanced features of the Cern Host Interface (CHI) clearly make it an excellent candidate for evaluation as a replacement for the GPM. So far, our experience with the first implementation of PAN-DA

supports our goal of being able to easily port software designs, tools and applications to new intelligent modules.

The separation of control and data paths in the software system, provision of functionally layered software packages, design of module independent software tools, will allow us to evaluate and support new modules with few changes in the design of the software and minimal and well defined changes in its implementation.

As a result of our experiences so far in development of PAN-DA, we feel we are - ready to take advantage of the new hardware as it becomes available; able to provide for very high data throughput systems by the use of vertical and horizontal parallelism; providing a smooth migration path for experiments with existing data acquisition systems to use of the new hardware and software modules; not locked into a particular architecture, bus implementation, processor module or communications path; ready to make use of impending RISC and DSP based processor boards.

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REFERENCES

- [1] I. Gaines et al. "Use of the Fermilab Advanced Computer Program Multi-Microprocessor as an On-Line Trigger Processor", IEEE Transactions on Nuclear Science, Vol. NS-32, No. 4, August 1985.
- [2] See accompanying paper: J. Deppe, et al, "ACPR3000 Processors in Data Acquisition Systems"
- [3] See accompanying paper: D. Petravick et al, "The PAN-DA Data Acquisition System"
- [4] Struck Catalog Module 500, General Purpose Master.
- [5] Internal specification available from Fermilab Electrical Engineering Department.
- [6] Cern Host Interface, Internal Cern specification
- [7] See accompanying paper: David Berg, et al, "A Real Time Integrated Environment for Motorola 680xx-based VME and FASTBUS Modules"
- [8] See accompanying paper: Eileen Berman et al, "Remote Procedure Execution Software for Distributed Systems"
- [9] T. Kozlowski and W.M. Foreman, "An implementation of the new IEEE Standard Routines for FASTBUS" IEEE Transactions on Nuclear Science, Page 800, Vol.NS-34, No.4, August 1987.
- [10] See accompanying paper: Terry Dorries et al, "FEREAD - Front End Readout Software for the Fermilab PAN-DA Data Acquisition System".
- [11] LeCroy FASTBUS Model 1821, LeCroy catalog.
- [12] Specification available from Fermilab Physics Department
- [13] See accompanying paper: Mark Bernett, Gene Oleynik, "Uniform Communications Software Using TCP/IP".
- [14] R.Pordes et al, "List Processing Software for the LeCroy 1821 Segment Manager Interface", IEEE Transactions on Nuclear Science, Vol.NS-34, No.4, August 1987.
- [15] D. Lesny et al, Device Diagnostic Language manual, available from the University of Illinois.
- [16] T. Dorries et al, "VMS Software for the Jorway-411 Interface", IEEE Transactions on Nuclear Science, Vol.NS-34, No.4, August 1987.
- [17] V. White, et al "The VAXONLINE Software System at Fermilab" IEEE Transactions on Nuclear Science, Vol.NS-34, No.4, August 1987.