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A LARGE DYNAMIC RANGE CHARGE AMPLIFIER ADC FOR THE FERMILAB COLLIDER DETECTOR FACILITY*

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Abstract

A multi-channel charge amplifier ADC system for use with electromagnetic and hadronic calorimetry has been built with X1 and X16 amplifier channels which extend the range of the single 16 bit ADC to the equivalent of a 20 bit system having 0.7 fC least significant resolution. Two on-board calibration schemes, a fast analog trigger output, and redundant readout are also included. The point-wise error in linearity (expressed as the maximum error as a percentage of the full charge scale) is less than 0.02% for the X1 channels, and less than 0.002% for the X16 channels. Other features include a Before/After signal differencing scheme which provides low frequency noise rejection and compensation for baseline drifting, and temperature stability on the order of 30 ppm/C.

Introduction

The RABBIT Photomultiplier ADC (PM ADC) described here is part of the front end electronics data acquisition system for the Collider Detector Facility (CDF) at Fermilab. It has been designed and built at Fermilab for use in the central electromagnetic and hadronic calorimeters to study collisions between protons and antiprotons having a center of mass energy approaching 2 TeV. The PM ADC must be capable of measuring average energy depositions in a calorimeter tower to an accuracy of better than 1% over the range 300 MeV to 375 GeV. This requires the electronics to have a dynamic range of approximately 100,000. It is desirable to monitor drifting of gain in both the electronics and the calorimeter itself to an accuracy approaching 0.1%. On-board calibration circuitry and phototube current readout has been included in the design to accomplish this. The necessary precision and large dynamic range, coupled with the need for low cost, low power, and high reliability are the major challenges in the design and production of the amplifier.

The PM ADC is part of the RABBIT (Redundant Analog Bus Based Information Transfer) system, a redundant, low cost, front end system which is intended to be situated in close proximity to detector components [1-3]. Each crate in the system has two analog and two digital buses on the backplane and two crate controller cards (the EWE cards), one for each bus; this gives the system a high degree of redundancy and reliability. A Before-After-Timing card (BAT), which occupies one slot in the crate, generates the fast gating for the sample and hold circuits as well as signals for any TDC's in the crate. It also generates signals for calibration purposes. The remaining twenty three slots in the crate are available for up to 1400 channels of general purpose front end electronics: charge amplifiers for photomultipliers and wire chambers, time to digital converters, trigger cards, etc. In CDF, seven different types of cards are used to read, calibrate, and trigger on four of the major detector systems: scintillator calorimetry, gas calorimetry, drift tubes for shower localization, and drift tubes for muon detection.

On each EWE there resides a single 16 bit linear ADC to which amplifier outputs are multiplexed on the analog bus of the crate backplane. The EWE cards are controlled by a host computer that can be located a large distance away from the detector components. A channel address is down-loaded to a EWE, an ADC convert command issued, and the digital number read back by the host. This scheme has several important advantages: performing the analog to digital operation on the detector not only reduces the number of interconnection wires between the counting room and the detector, but also eliminates many of the problems associated with transmitting sensitive analog signals over long distances. Reducing the number of ADC chips in a crate to one or two helps to minimize calibration errors between different ADCs, and reduces overall channel cost as well.

The RABBIT electronics make use of the Before/After gating scheme described in [3-4]. The output of each charge amplifier is connected to two sample and hold circuits. The first sample is taken just before an expected event, and the second sample taken just after. This eliminates baseline drift errors in the data. The Before and After timing signals are generated in the crate by the BAT module which derives them from an external trigger input. For CDF, the trigger is a single timing pulse that is centrally produced and distributed to the entire detector. The Before and After signals are timed off of the leading and trailing edges of this trigger signal.

Circuit Description

The PM ADC is a 12 channel charge integrating amplifier card. Each channel consists of a charge sensitive amplifier, sample and hold circuitry followed by X1 and X16 amplification, a DC current channel, and two sets of analog multiplexers for sending the analog signals to either EWE crate controller for ADC readout. Each channel also has Fast Out circuitry which sends analog pulse height information to the trigger system. The overall circuit is shown in Fig. 1.

The charge-integrating amplifier is of the same class of amplifiers as described in [5-11] and elsewhere. The basic circuit

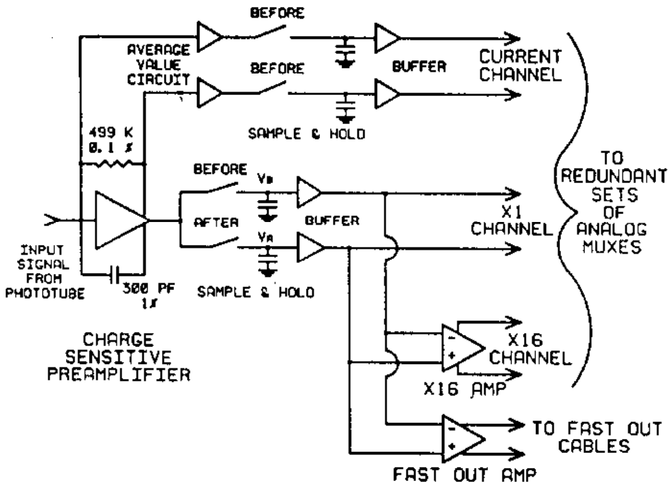

FIG. 1 RABBIT PM ADC

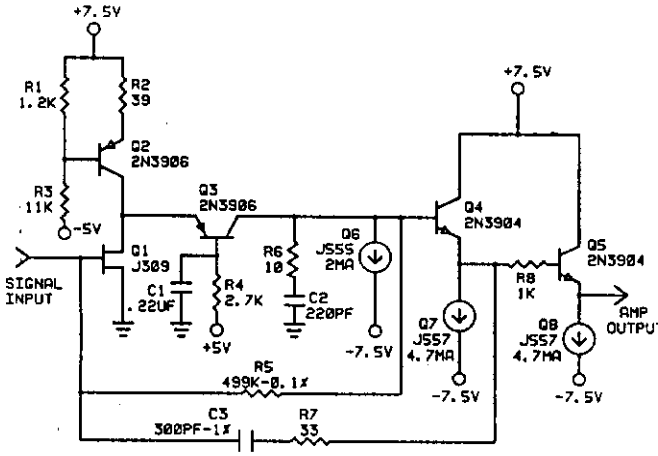

FIG. 2 PM ADC AMPLIFIER SCHEMATIC

configuration is shown in Fig. 2. The FET input, cascode stage amplifier formed by Q1 and Q3 provides high input impedance and current gain. Transistor Q2 is an adjustable current source for biasing the circuit. The output stage is formed by Q4 and Q5. One interesting feature of this configuration is the ability for the output to accomodate three consecutive full scale hits without saturating the amplifier.

The open loop frequency response is shown in Fig. 3. The open loop mid frequency voltage gain is given approxiamately by:

$$Vo / Vi = - gm * Rx$$

where Rx is the impedance of the J555 current source, which is approximately 500 K ohms. For the J309 FET, gm is approxiamtely 0.010 mhos. This gives a mid-frequency gain of about 5000. The lag network formed by C2 and R6 determine the open loop corner frequency, and have been chosen to match the dynamic input impedance of the amplifier to the 50 ohm signal cable. For mid frequencies, this is given by:

$$Zi = 1 / (Cf * 2 * pi * Ao * Fo)$$

where Ao * Fo is the gain bandwidth product. Another function of the lag network is to guarantee closed loop stability by having the

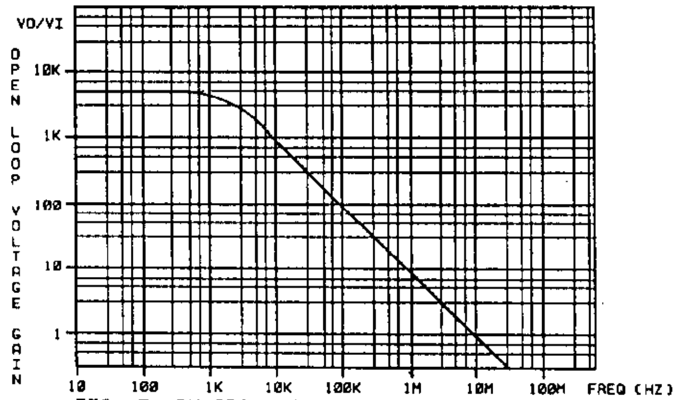

FIG. 3 PM ADC OPEN LOOP FREQUENCY RESPONSE

open loop transfer function roll off at -20 db/decade through unity gain.

The amplifier output is sampled by CMOS HEF4066 type switches using the Before/After scheme. Each Before and After switch consists of two switches connected in parallel to achieve lower "on" resistance. This reduces the charging time constant of each sample and hold capacitor to approximately 25 nSec. The samples are held on 470 pF polypropylene capacitors, which have driven guard rings surrounding all sensitive solder connections and traces. The capacitors are buffered using RCA 3240E op amps. The open-circuited CMOS switch together with the high input impedance of the buffer give an effective holding time constant of approximately 200 Sec, although the RC decay deviates from a simple exponential after this time. The polypropylene capacitors were found to have the lowest dielectric absorption of all types tested.

The choice of feedback resistors and capacitors for the amplifier was made with temperature stability in mind. The feedback capacitor is a 1%, NPO type ceramic, having a 30 ppm/degree C temperature coefficient. The resistors used in the feedback loop and in all gain and Fast Out stages are 0.1%, RN55C type metal film, having 50 ppm/degree C temperature coefficient.

The analog-to-digital converter used in the RABBIT system is the Burr-Brown ADC-76, a linear 16 bit resolution device which has a 17 uSec conversion time. The gain of the ADC has been calibrated so that the full scale ADC range corresponds to 0 to 2.5 Volts at the input. In terms of charge from a phototube, the 300 pF feedback capacitor in the amplifier yields full scale at 750 pC. The 16 bit resolution of the ADC gives a least significant bit resolution of 11.4 fC for the X1 channel. The X16 gain stage on the PM ADC card provides an accurate measurement of the energy loss of minimum ionizing particles and gives the system the equivalent of 20 bits of dynamic range with 16 bits of resolution. The least significant bit resolution associated with the X16 channel is 0.7 fC. In terms of energy, this corresponds to 5.7 MeV for the X1 channel, and 0.35 MeV for the X16 channel.

The circuit board has two on-board calibration systems. The first is an on-board charge-injection circuit which is addressed to inject charge into one channel at a time. This circuitry provides a method of accurately measuring the gain of the amplifier. The second system is the current channel readout for calibration of the calorimeter itself. The average current flowing through the feedback resistor of the charge-integrating amplifier is sampled at a single instant in time by use of sample and hold circuitry. The calorimeters are equipped with Cs-137 sources which are attached to a wire which loops through the calorimeter. A motor moves the source through the calorimeter, illuminating the scintillators in the process. This injects 50 nA of current into the amplifier for the duration that the source is traversing a particular tower. By reading out the current channel on the PM ADC card and knowing the strength of the source, the response of the calorimeter can be monitored.

The only analog signals which are transmitted over long distances to the counting room are those coming from the Fast Out circuitry for making trigger decisions. The Fast Out circuitry is a fast op amp configured as a differencing amplifier with a gain of -0.75. The Harris HA-2605 was selected as the best device for this application based on cost performance. The circuit drives 220 foot, 100 ohm, series terminated, twisted pair cables to the counting room, where trigger decisions must be made before the next proton-antiproton beam crossing. The present cycle time at CDF is 7 uSec.

The circuit board is a standard two-sided board, and all the parts except for the precision capacitors, precision resistors, and sample and hold capacitors are standard stock items. The board is made entirely of discrete and monolithic components. These factors, combined with the absence of resident ADCs on the board have put production costs at $500.00 per board including test and calibration. This translates to $40.00 per amplifier, or $10.00 per readout channel.

Performance Characteristics

Lab tests performed on the production version of the PM ADC card have yielded the following performance characteristics for the electronics:

1. The integral linearity of the entire charge-integrating amplifier - ADC readout system has a typical error of less than 0.02 % (as a percentage of full scale) over the range 0.004 to 0.9 of full scale (750 pc) for the X1 channels. Typical error for the X16 channels is less than 0.002 % over the range 0 to 0.045 of the full charge scale. These results are shown in Fig. 4. The data was obtained using a precision external charge injection circuit.

2. Typical noise figures at pedestal are sigmas of 20 fC (0.003% of full scale) for the X1 channel without signal cables and phototubes, and approximately 40 fC connected to the detector. The X16 channels amplify the noise in the charge-integrating amplifier although it is typically less than sixteen times the noise in the X1 channels. This indicates that some of the statistical variation in ADC readout is due to noise in the readout circuitry, and also to quantization error in the ADC itself.

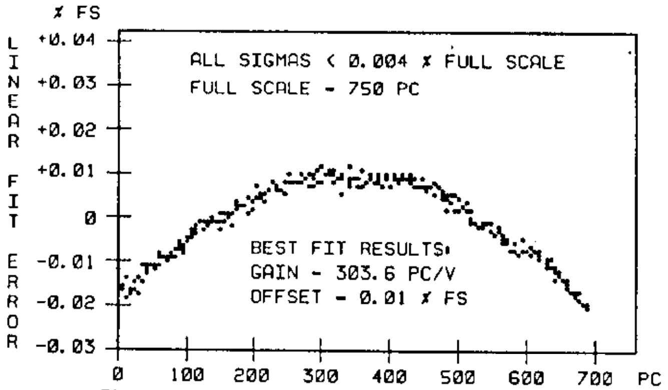

FIG. 4 ERROR IN LINEARITY (% OF FULL SCALE) VS. INJECTED CHARGE FOR THE X1 CHANNEL

3. Typical pedestal temperature dependence for the X1 channels is +/- 15 ppm / degree C over 20 to 70 degrees. Worst observed case for the X1 channels was a +/- 45 ppm / degree C dependence. For the X16 channels, typical pedestal temperature dependence is of order +/- 75 ppm / degree C, with worst case at +/- 225 ppm / degree C. These results are shown in Fig. 5. The pedestal drifts are primarily due to the input offset voltage dependence on temperature of the X1 buffer and X16 differencing op amps.

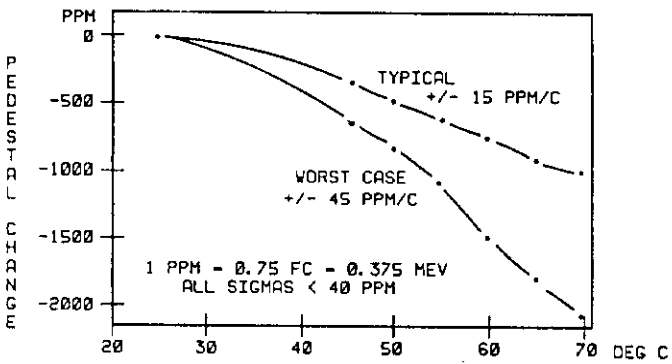

FIG. 5 CHANGE IN X1 CHANNEL PEDESTAL FROM ROOM TEMP VS. OVEN TEMPERATURE

4. The plot in Fig. 6a shows pedestal fluctuation over time. Typical drift is on the order of +/- 0.02 % of full scale over the course of 80 hours. As shown in Fig. 6b, the pedestal drift followed the temperature deviation, and appears to be consistent with the temperature test data.

5. The ADC readout of the amplifier response as a function of integration time (the time between charge injection and the opening of the After switch) settles within 0.6 % of the final value in 200 nSec, and rises within 0.08 % of the final value in 300 nSec. Maximum ADC

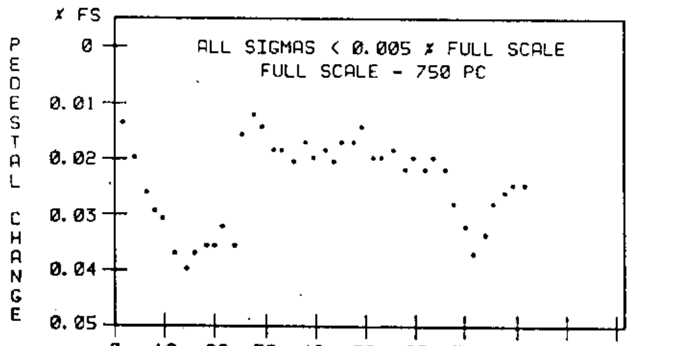

FIG. 6A X1 PEDESTAL DRIFT VS. TIME AS A PERCENT OF FULL SCALE

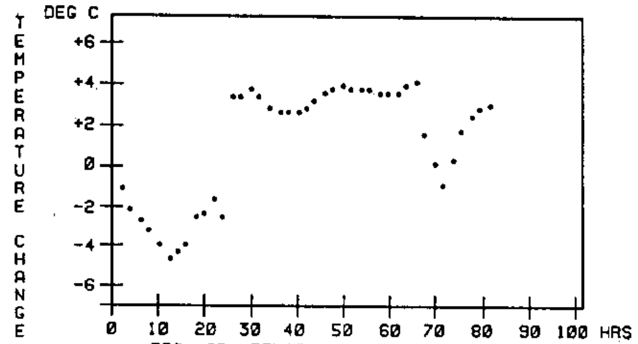

FIG. 6B TEMPERATURE CHANGE VS. TIME DURING PEDESTAL RUNS

readout occurs at 350 nS in response to a full scale hit. After this time, the ADC readout begins to droop with the 150 uSec decay of the charge integrating amplifier. This measurement is consistent with the measured 100 nSec rise time of the amplifier. The gating for the CDF detector has been chosen to optimize this result.

6. Crosstalk measurements using an external charge pulser showed approximately 80 db rejection between neighboring channels, and no perceptable variation in other channels above normal channel noise. The measurement was made by injecting full scale charge into a selected amplifier and reading out all other channels.

7. The card requires +8 V., +5.5 V., -5.5 V. and -8 V. power supplies. Total power consumption of the card is 12.5 watts.

8. The Before/After gating scheme provides effective low frequency noise filtering. Noise rejection of the ADC readout of a channel subject to the presence of sinusoidal noise induced into the PM ADC amplifier input via transformer coupling is on the order of 50 db at 1 kHz. Below 1 kHz the rejection improves with some broadening of the pedestal over the normal noise of the amplifier noted, although the average value remains constant. This measurement is strongly dependent upon the integration time (time between the Before and After samples). The above result was made using a 500 nSec integration time.

Conclusion

The RABBIT PM ADC is a relatively inexpensive charge amplifier, current amplifier, and ADC system which measures charge to an accuracy better than 0.1 % over nearly the full scale. Pedestal variations over time are better than 0.015% of full scale. Of particular importance is the dynamic range which is equivalent to a full 20 bit system. This is sufficient not only for measurements at the Collider Detector Facillity at Fermilab, but should also be adequate in terms of dynamic range, linearity, and stability for use at accelerators such as the proposed Superconducting Super Collider (SSC) at which the range of particle energies are 100 MeV to 5 TeV.

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