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ON-SHORE PROCESSING*

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ABSTRACT

A proposal is made to use a fast trigger processor to utilize the data acquisition system proposed at this workshop.

In another paper in these Proceedings[1], a data acquisition system is outlined which has the capability of transmitting data from each module to shore at an average rate of 10^5 samples per second. The data from an entire string of 24 detectors are time multiplexed with a well defined position for each detector in the transmission time sequence onto a single optical fiber which operates at a $\sim$ 44 MHz rate. This fiber carries the data from that string all the way to shore. The station on shore has 36 such fibers (one for each string) all spewing out data at $\sim$ 44 MHz for a total data transmission rate of $\sim$ 1.6 GHz. This rate is impossible for conventional computers to handle, therefore, some preprocessing of the data is necessary before processing in a conventional computer. In this paper, we propose a model for such a preprocessor.

The first step in this preprocessing is to load the data into fast memories as it appears at the shore station. The transmission of the data is controlled by a clock on shore and is synchronous; all 36 lines will have data arriving simultaneously. Each fiber has transmission records which consist of a sequence consisting of a header, twenty-four 24 bit words (Fig. 1) from the twenty-one DUMAND optical detectors and three ancillary detectors on each string, and a tail record. These words contain the analog to digital converter (ADC) and time to digital converter (TDC) scaler information and flag bits from the modules on that string. There is no need to transmit a detector ID, since each detector occupies a unique position in the transmission record of the optics fiber of its string. Furthermore, because of this unique location in the transmission sequence and the synchronous nature of the system, the contents of the ADC and TDC scalers can be loaded sequentially into a bank of fast memory containing 756 words with each fiber using 21 unique DUMAND optical detector words. However, the wrap-around feature of the time (modulo the reset period) must be taken into account.

After completion of one transmission cycle, another bank of fast memory is readied to receive the next cycle. At the same time, as the data is loaded into the memory, a kick sort is performed on the first bank choosing a small fraction of the data which will be used to make the trigger decision. Such sorts could be made on pulse height or on the coincidence bit generated by the near neighbor fast coincidence logic option, if implemented[2]. If not implemented at the array, such logic may be inserted at the shore processor and invoked as the data is received on shore. The object of such a sort would be to choose the 8-10 most promising signals for further processing. At this time, a module ID tag is added to the data giving it indices IJK which locate its position in the array. Upon completion of the second data transmission cycle, the 8-10 most promising signals from the second bank of fast memory are added to the first set. Data from both banks of fast memory are necessary because the actual arrival of true signals is not synchronous with the data transmission, and true signals may occur spread over two transmission cycles. At this point, 16-20 words have been chosen for further processing. Schematically, this process is shown in Fig. 2.

Using a method similiar to that previously discussed by Roberts[3], one TDC count is extracted and all others tested against it for coincidence. A table consisting of 6 x 6 x 21 elements defined by the ΔI, ΔJ, and ΔK values between the two detectors is stored which contains the time of flight differences between any pair of sensors. A single table is possible since the array is approximately a regular lattice. Thus, to perform the coincidence test, all that is required is a simple table lookup. If the difference between the two sensor TDC counts is not equal to the quantity stored in the table, the relationship is not timelike, and the two are not on the same track; the interval can then be labelled spurious. By performing pair-wise comparisons between all members of the chosen subset, candidates for true coincidences can be found and thus used to establish a trigger criterion.

The object of this exercise is to reduce the event rate from the $\sim 10^5$/sec being transmitted from the detector array to ~ 10/sec transmitted to the computer. This latter number is driven by the rate which one can write to normal computer memory. By choosing different fast trigger algorithms, varying the Δt of the time coincidence and the number of coincidences required for triggering the desired ¢10^4 rate reduction should be achievable.

The proposed fast trigger algorithm is by no means unique. Very crude time sorts could be initially performed to establish timelike behavior at the 2 μsec level, equivalent to the array traversal time. Then the detailed time correlation described above could be carried out. Also, simultaneous parallel processing using several algorithms could be carried out. All that these algorithms must decide is whether the data in the original memories should be passed on to the general purpose computer for "on-line" analysis and/or for recording on magnetic tape, or should it be discarded. What is necessary, is that this decision be made quickly, within ~ 100 μsec. An array of 10 to 20 fast buffer memories and the same number of fast processors are typically needed to match current computer memory and calculation speeds.

Once the decision is made that the trigger condition is satisfied, the contents of the associated two banks of fast memory (1512 words) are passed to the normal computer and then returned to the stack of fast buffers.

The computer then processes the data, typically suppressing zeros and properly justifying the TDC counts between the two transmission cycles for use by more sophisticated track finding programs and finally for recording it on tape. The computer required to do this is a typical present generation data acquisition computer similiar to the DEC VAX 11/780. The tape usage for , 10 events/sec x 1500 words/event is one tape every 40 minutes, using a 6250 BPI tape. It would be highly desirable to depress this rate by yet another factor ~ 5 to reduce the tape and computing load.

We conclude that a special processor, adequate to the presently proposed DUMAND system needs, is practical within present technology. The cost which will not be trivial will be small compared to the array costs.

REFERENCES

1. A. E. Brenner *et al.*, The DUMAND Array Data Acquisition System - These Proceedings.

2. A. E. Brenner, *et al.*, *ibid*, Section on Limited Coincidence Option.

3. A. Roberts, Fast Event-Analyzing Algorithm, DUMAND, HDC 81-15.

FIGURE CAPTIONS

1. The DUMAND array data stream including the header and 24 words of 24 bits each of data followed by a trailer for each string in each communication cycle of approximately 13 microseconds. Note that only 21 of the 24 detector words are relevant to the primary DUMAND experiments. The other three detectors are ancillary and are not relevant to the processing on shore of the DUMAND experiment.

2. An overall block diagram of the mechanism of handling the 36 string communications streams to be handled by the front end of the shore processing system. Each data stream is reconstructed into 21 words at 24 bits each. These are then inserted into a well-defined memory bank in the next available buffer. The position of the memory bank in the buffer defines the string to which the data belongs. All 36 transmission lines feed the same buffer in parallel. The next communication cycle fills the next available buffer. A trigger selection logic operates on two pairs of buffers selecting potential candidates for tracking. These include either flagged near coincidence pairs or high pulse height signals. A fast trigger analyzer then performs the necessary tracking algorithm and flags the event as success or failure. On success, the contents of both buffers are transferred to the shore processor for additional processing and for recording on magnetic tape.

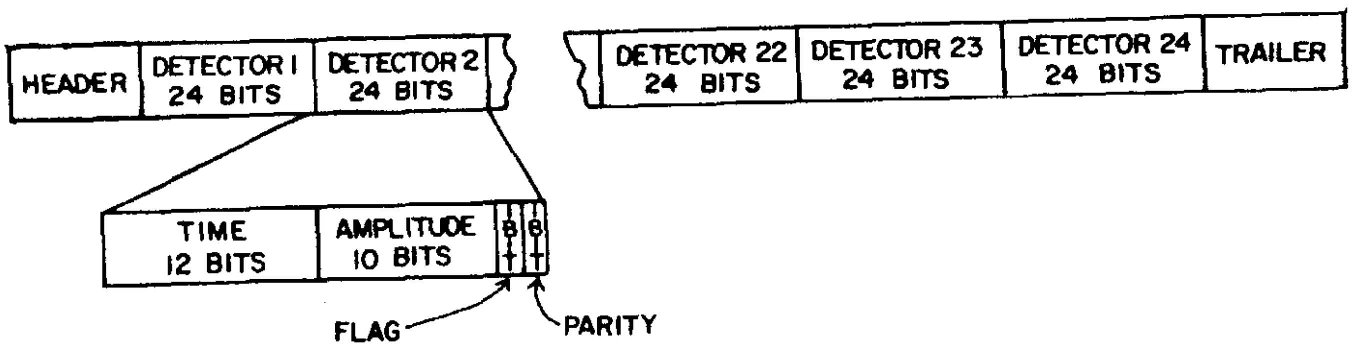
HEADER
DETECTOR 1
24 BITS
DETECTOR 2
24 BITS
DETECTOR 22
24 BITS
DETECTOR 23
24 BITS
DETECTOR 24
24 BITS
TRAILER
TIME
12 BITS
AMPLITUDE
10 BITS
FLAG
PARITY

Fig. 1

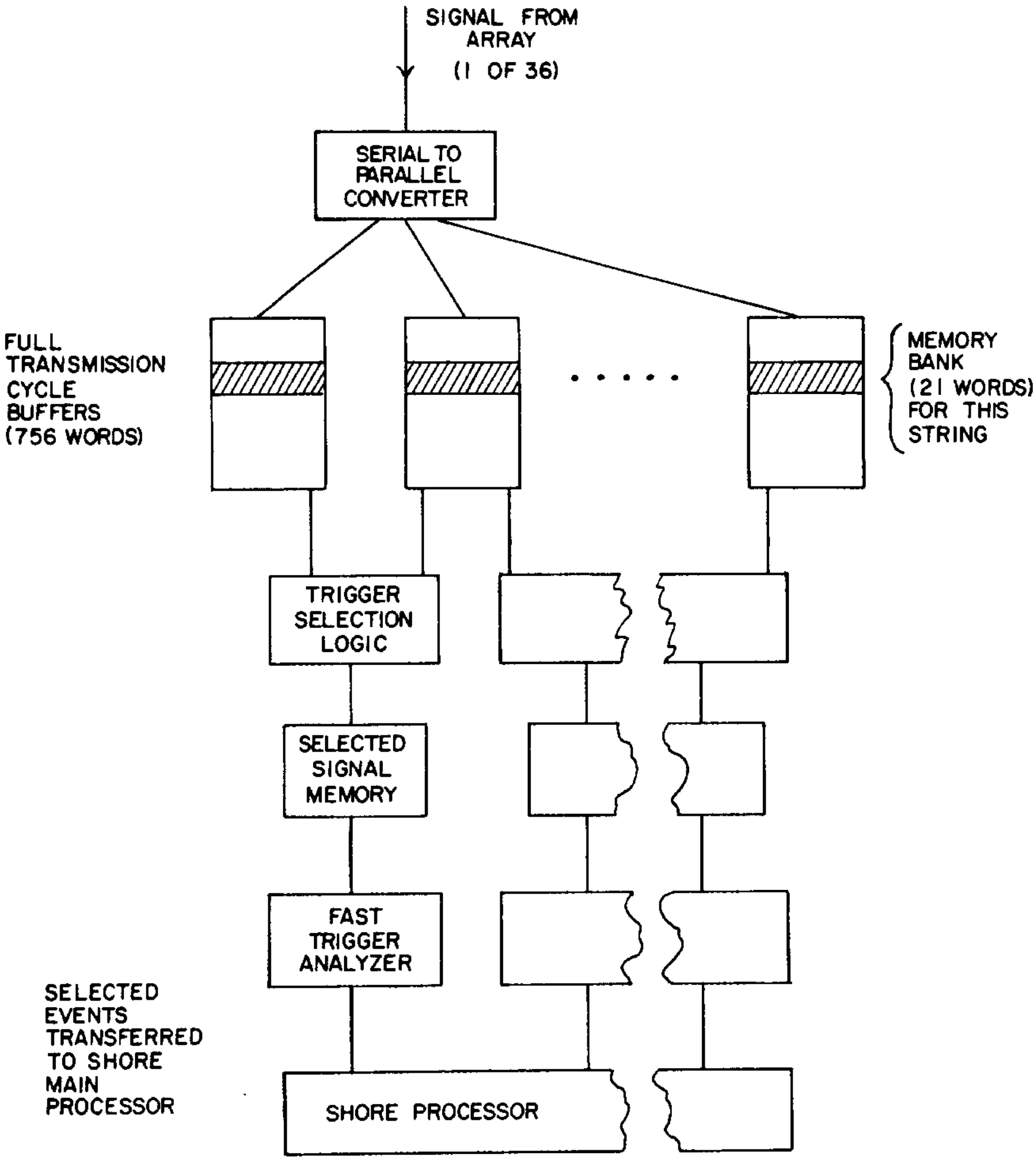
SIGNAL FROM ARRAY (1 OF 36)
SERIAL TO PARALLEL CONVERTER
FULL TRANSMISSION CYCLE BUFFERS (756 WORDS)
MEMORY BANK (21 WORDS) FOR THIS STRING
TRIGGER SELECTION LOGIC
SELECTED SIGNAL MEMORY
FAST TRIGGER ANALYZER
SELECTED EVENTS TRANSFERRED TO SHORE MAIN PROCESSOR
SHORE PROCESSOR

Fig. 2