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DESIGN PHILOSOPHY FOR A HARDWARE PRELIMINARY DATA REDUCTION IN A HIGH ENERGY SCATTERING EXPERIMENT USING SOLID STATE DETECTORS

P. Franzini, S. Childress
Columbia University
New York, N.Y., U.S.A.

J. Lee-Franzini, R. McCarthy, R.D. Schamberger
SUNY at Stony Brook
Stony Brook, N.Y., U.S.A.

With the great variety of large scale integrated circuits available today, it is probably just as simple to design hardware to perform simple data reduction tasks as to write programs on a general purpose computer. The advantages of the first alternative are reduction of the amount of storage required, increased speed in data collection and avoiding a two-way communication between computer and detector electronics.

In the specific example discussed, the experiment consists of a series of telescopes each formed of two solid state detectors. All telescopes look at a target bombarded with the 200 to 400 GeV external proton beam and they are used to detect recoils from such a target. In addition, the energy of the recoils is to be determined by measuring the charge signal output by the detector to one part in 2^{12}. An event thus consists of two counters in a telescope giving a simultaneous signal. It is however of interest to know how many times another counter in the array was also crossed by a particle. In other words, all counters are to be examined, whenever any telescope is active. A severe constraint is the extremely low duty cycle and high instantaneous even rate.

To this end, each counter signal is fed to a discriminator and an analog channel terminating in a sample and hold amplifier as shown in Fig. 1. A master trigger is formed corresponding to a coincidence in any telescope. Upon receipt of such trigger, all discriminators are entered into registers and all sample and hold amplifiers are switched to sample mode and back to hold mode. All these operations are performed in approximately 400 nsec, this time being necessary for the S and H amplifier to settle to the required accuracy.

About 100 nsec after receipt of a trigger the data reduction hardware begins to analyze the data by performing the following operations:

1. Initiate register scan.
2. Generate addresses corresponding to active registers (i.e., counters which gave a signal).
3. Pack such addresses two per 16 bit word (up to 256 counters or 128 telescopes) and enter into the memory of a PDP-11 computer via direct memory access.
4. First and second address are also wired to two analog multiplexors which connect directly the output of the sample and hold amplifier corresponding to the two active counters to two 12 bits successive approximation converters.
5. The system waits for transients to settle, then initiates conversion. Upon receipt of end of conversion signal, the two pulse heights are entered into the computer (2 words, 12 bit per word used).
6. Continue register scan and repeat above as necessary.

A schematic drawing of such operation is shown in Fig. 2. The whole logic circuit is built on three cards 15 x 30 cm^2. The register scan is performed in a serial parallel way - groups of 8 registers are examined together. If no register is on, the next group is examined. With very modest clock speed (~ 5 Mc), it is thus possible to scan 40 registers in approximately 2 μsec. The system is built to accept up to 80 registers. The relevant properties of the system are - one event, with only two counters, requires 17 μsec and produces four 16 bit words. The four words contain: Word 1 - run data and flag bit to signal beginning of event; Word 2 - two counter addresses; Word 3 - first pulse height; Word 4 - second pulse height. The 17 μsec are divided as follows a) register scan 2 μsec, b) analog switches turn on delay 2 μsec, c) analog signal setting time 4 μsec, d) digitize time 4 μsec, e) storing time, 5 μsec. With the system described, we have been able to collect as many as 4000 events per machine burst in a run at 400 GeV at the National Accelerator Laboratory with a gross spill length of ~ 300 msec. In a previous run, at 300 GeV, we have collected ~ 18,000,000 events in ~ 17 hours of running time.

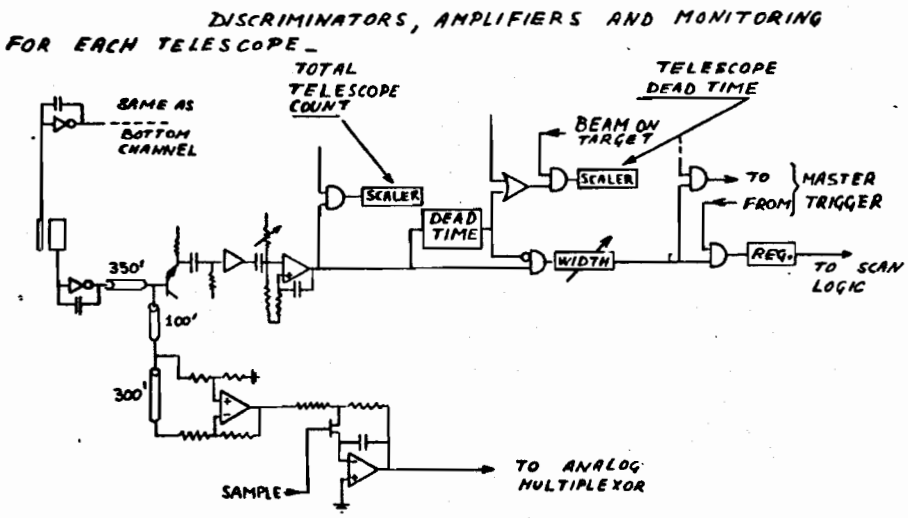
DISCRIMINATORS, AMPLIFIERS AND MONITORING
FOR EACH TELESCOPE_
TOTAL TELESCOPE COUNT
TELESCOPE DEAD TIME
SAME AS BOTTOM CHANNEL
BEAM ON TARGET
SCALER
SCALER
DEAD TIME
TO
FROM
MASTER TRIGGER
WIDTH
REG.
TO SCAN LOGIC
350'
100'
300'
SAMPLE
TO ANALOG MULTIPLEXOR

FIG. 1

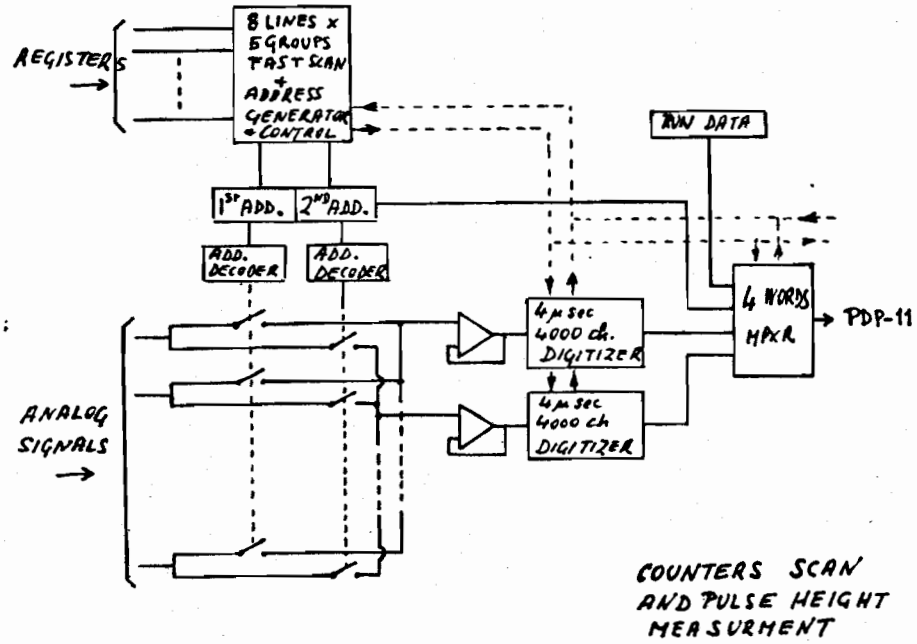
REGISTERS
8 LINES x 5 GROUPS FAST SCAN + ADDRESS GENERATOR + CONTROL
RAW DATA
1ST ADD.
2ND ADD.
ADD. DECODER
ADD. DECODER
4 μ sec 4000 ch. DIGITIZER
4 μ sec 4000 ch DIGITIZER
4 WORDS MPXR
PDP-11
ANALOG SIGNALS
COUNTERS SCAN AND PULSE HEIGHT MEASURMENT

FIG. 2