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ELECTRONICS FOR SOLID STATE DETECTORS IN HIGH ENERGY PHYSICS EXPERIMENT

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We have developed the entire electronics required for using silicon solid state detectors. This consists of charge sensitive preamplifiers, discriminators with special features, active filters and sample and hold amplifiers. The reasons for developing anew such devices were many, notably cost and non-existence of some items with characteristics suitable to the use of silicon detectors at a very low duty cycle machine (see paper on design philosophy presented at this conference). We present here with a brief description, the schematic of each circuit.

1, Charge Sensitive Preamplifier

Typically, we want to detect and measure to better than 1% accuracy charges in the range 10^{-14} to 1.5×10^{-12} coulomb. Coincidence between two detectors have to be made with resolving times around 50 nsec. Also, the dynamical range should extend another factor 5 above the mentioned range because of the very high instantaneous rate of both signal and background. Finally, detector and preamplifier are located far away from the location where the output signal is processed, thus the preamplifier has to be able to drive a low impedance load (93 Ω RG 62 cable) with rather large voltage swing (± 7.5 V). Figure 1 shows the schematics of such amplifiers.

Gain is achieved through a grounded source stage DC coupled into a common base stage seeing at its output a current source as the load. The DC gain for this part of the circuit is $\sim g_m/(A_1+A_2)$ where g_m is the transconductance for the FET and A_1, A_2 are the output admittance of the two transistors. The input FET is chosen here mainly as the cheapest device which is acceptable. The 2N4857 is usually described as suited for audio amplifiers and switching applications. As used here $g_m \simeq 18 \times 10^{-3}$ mho, A_1, $A_2 \leq 10 \times 10^{-6}$ thus the small signal DC gain $\geq 10^3$. This stage is followed by a source follower to couple into a complementary emitter follower capable of driving a 93 Ω load up to the required voltage. The DC negative feedback through the 100 MΩ resistor is somewhat uncommon because the gate of the input FET is kept a few volt negative while the output is approximately at DC zero. This has the advantage of decreasing the input capacitance; it does require however AC coupling across the voltage divider to bias the input gate. No degradation of the amplifier is observed even for recovery from large signals.

The conversion gain (output voltage/input charge) is determined by the feedback capacitor. We use a teflon trimmer adjustable between 0.5 and 1.5 pF. Electrostatic shielding reduces all other couplings from output to input to below 0.1 pF. We have used for the last six months 50 such amplifiers without a single failure. The gain of the amplifiers was adjusted to about 1.1 V/pC. Under this condition, the output risetime is ~ 30 nsec. Such risetime can be halved by halving the gain as well as using a more expensive input FET such as the 2N5433.

We did not choose to do so because a) the signal risetime after 350 ft of cable is considerably slower than 30 nsec, b) the second counter on each telescope is 5 mm thick and its charge collection time is ~ 200 nsec.

The total parts and printed circuit cost for such amplifier is ~ $10 to be compared with ~ $450 for comparable commercial units. The noise contribution of the amplifier is of the order of 10^{-16} Coul equivalent at the input, typically a factor 10 smaller than the intrinsic detector noise. Another consideration which was determinant in the final circuit design was that many such preamplifiers were to work in extreme closeness to each other as well as in a highly noisy environment (S.C.R.). This was obtained by heavy decoupling the input power, by having a printed circuit with ground plane and an additional ground plane ~ 1 cm away from the component side, input and output signals are connected via shielded cable soldered to the printed board and finally great care was spent in avoiding multiple ground loops. This is shown schematically in Fig. 2. As a result, an array of 50 such amplifiers in groups of 20 mounted together inside a small aluminum box and 10 under high vacuum proved to be completely stable even if any number of the 350 ft cables were left open or shorted rather than properly terminated. Also no noise pickup from the many surrounding sources was evident.

2. Discriminators

The requirement for the discriminators to follow the above amplifier are: sensitive to an input voltage step of 10 mV with 100 nsec risetime, ≤ 350 nsec recovery time for the input step of 5 V, slewing less than 50 nsec for 1.1 x threshold to 100 x threshold. To improve packing density the following additional features were incorporated. a) Each channel has an updating deadtime generator of variable length between 0.5 and 50 μsec; b) every pair of channels is "and'ed" together to provide a coincidence signal from the elements of a telescope; c) every channel generates a pulse of length between 50 and 500 nsec to set, upon receipt of a strobe signal, a corresponding register. Finally, in order to monitor the total deadtime of each telescope, the output of the corresponding deadtime circuits are "or'ed" together. This signal is then used to gate on a scaler which counts the instantaneous beam rate. The circuit shown in Fig. 3 is largely self-explanatory. The signal is coupled in without input loading, is differentiated, amplified, differentiated again. A Schmidt trigger is the discriminator proper. The updating deadtime is generated by discharging a condenser for each threshold crossing and recharging the condenser with a current source. The same method is used for generating the output width. The entire circuit uses MECL II logic. In particular amplifiers, Schmidt trigger and sensing of the ramp for the deadtime are built using the MECL 1039 line receiver as a differential amplifier. The register output is available as a TTL level. Eight discriminators, coupled as four double channels as described are mounted in a single width NIM bin. An "or" of all eight discriminators is available at a front connector for diagnostic purposes.

3. Active Filter Amplifiers

The output of the charge sensitive amplifier is to a good approximation a voltage step over an arbitrary DC value. In order to measure the charge deposited in the solid state detectors, it is necessary to measure such voltage step, irrespective of the average DC level. This is ideally done by subtracting from the input signal the same signal delayed by some time, t. t should be as short as possible for two reasons: a) The DC base level has low frequency (see Fig. 5) noise due to fluctuations in the detector bias current. b) Pileup probability increases as t increases. On the other hand, the shortness of t is determined by the risetime of the amplifiers used to invert, to sum etc. Using a true operational amplifier it is possible to directly obtain the difference of the signal and the delayed signal as well as to have gain > 1 with a single stage. This is shown in Fig. 4. The amplifier used is the Harris 2055 (~ $15) which has a slew rate of 120 V/μsec and can be used without compensation for gain > 3. Since we want t to be as small as possible, the delay line has to have very good frequency properties and thus we use 93Ω RG62 cable. The circuit shown has a gain of 4 at the positive input and a gain of 3 for a signal applied to the resistor connected to the inverting input. To perform a proper subtraction, the signal at the positive input has thus to be reduced by x 3/4. Rather than using a fixed divider, a 10 turn trimmer is used. This allows also to compensate for signal attenuation through the delay cable. It also partly compensates for the fact that the input voltage is not a step but more precisely a step followed by an exponential decay with a time constant of 100 μsec. The circuit described has an overall gain of about 2.5 when used with 300 nsec delay and about 2.2 with 500 nsec. (The loss from the nominal gain of 3 is due to the cable attenuation.) For an input step, the output risetime is about 50 nsec. The output returns to DC zero at the end of the delay time plus risetime of the pulse except for a small and long tail (~ 5 μsec) which is about 1% of the output signal. Such tail can be very easily reduced to less than 0.1% after 1 μsec by the use of RC networks to compensate for high frequency losses in the cable. Since such compensation is dependent upon risetime of input and differentiation time, it is only indicated here. The ability of the circuit to extract signal from noise is shown in Figs. 5a, b. Figure 5a shows the actual output of a very poor solid state detector. Buried in the slow noise are signals from 5.477 MeV α's. Figure 5b gives the filter output for the same α signal. A pulse height analysis of the output signal for this extreme bad case gives a full width at half maximum of about 60 keV or a factor 2 better than available commercial amplifiers. The useful output range for the amplifier is ~ ± 10 V. They were used in our application for positive signals up to 5 V. Linearity was tested to be better than 1% and is believed to be better than 0.05%.

4. Sample and Hold Amplifier

As described previously the solid state detector output has been processed so far to produce an approximately rectangular voltage pulse whose amplitude is proportional to the charge released in the detector. Upon receipt of a trigger, it is required to measure the pulse amplitude to record it in the computer memory. Because the pulse is

of very short duration (300 to 500 nsec), it is necessary to store the pulse amplitude in analog form before initiating multiplexing and analog to digital conversion. This operation is performed by an integrating type sample and hold amplifier.

As shown by the schematic in Fig. 6, the circuit is an integrator with essentially zero input current when the 2N4416 FET is off (gate at - 6 V). Thus, the output voltage is held constant except for drift due to leakage currents. Notice that the integrating capacitor is 20 pF!

If the FET switch is on, then we have an inverting amplifier with gain given by R_{out}/R_{in}. The output risetime is ~ 70 nsec and settling time to ~ 0.1% is 400 nsec for a gain of one. Larger gains give slower risetime but approximately the same settling time.

The FET switch has been here chosen with the two requirements of a) small gate drain capacitance, b) small $V_{GD\ off}$. Points a) and b) together insure that the on and off transition inject the least charge into the amplifier summing junction. Although this effect in this configuration is equivalent to a constant DC shift it is rather annoying to have a few volt shift over a few volt signal. This shift is further reduced by coupling into the summing function the complement of the pulse driving the FET. Point b) further allows to use open collector TTL inverters for double pulse inversion. We have observed no damage to the TTL inverters by using +6 V on the open collector outputs. The drift rate of the output in the hold mode varies for 40 amplifiers, without component selection, between 0.01 and 5 mV/nsec. Since our full scale signal is 5 V and we digitize to 1 part in 4000 or 1.25 mV in ~ 20 μsec, the worst case drift is still better than necessary by a factor 10.

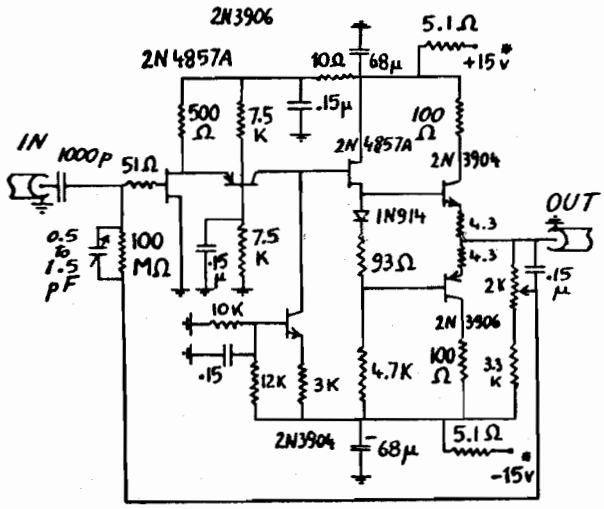


FIG. 1

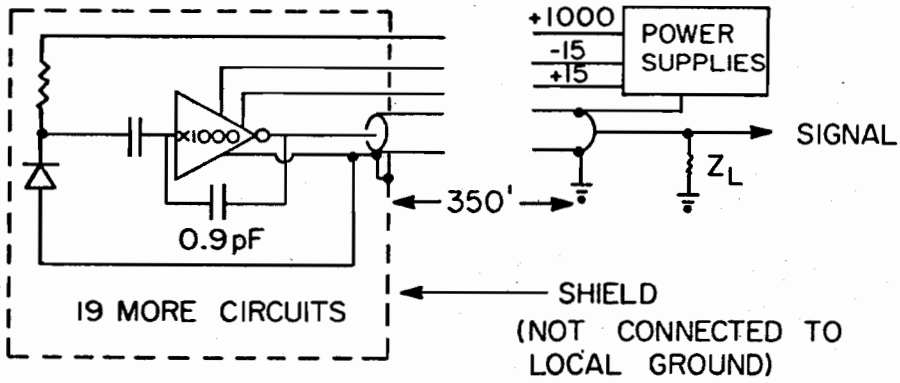


FIG. 2

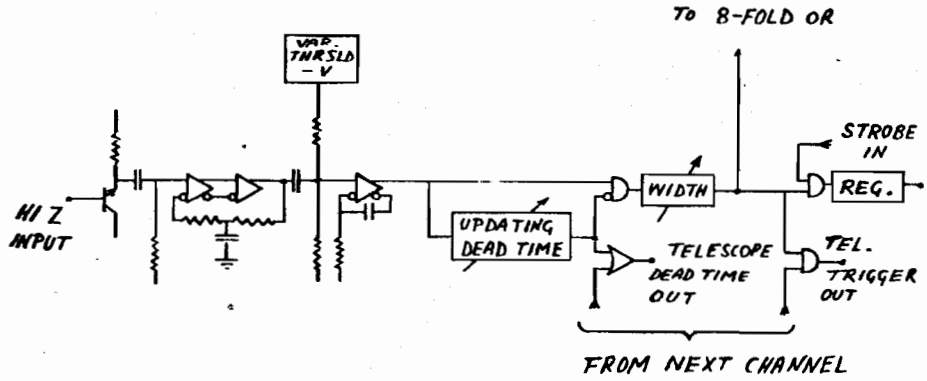


FIG. 3

DISCRIMINATOR BLOCK DIAGRAM

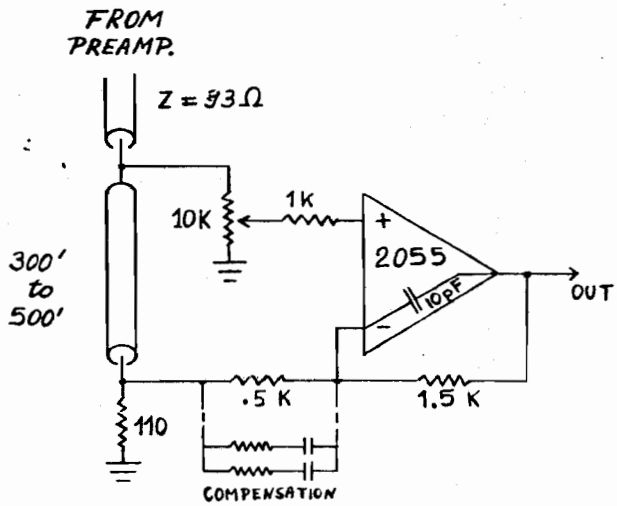


FIG. 4

ACTIVE FILTER AMPLIFIER

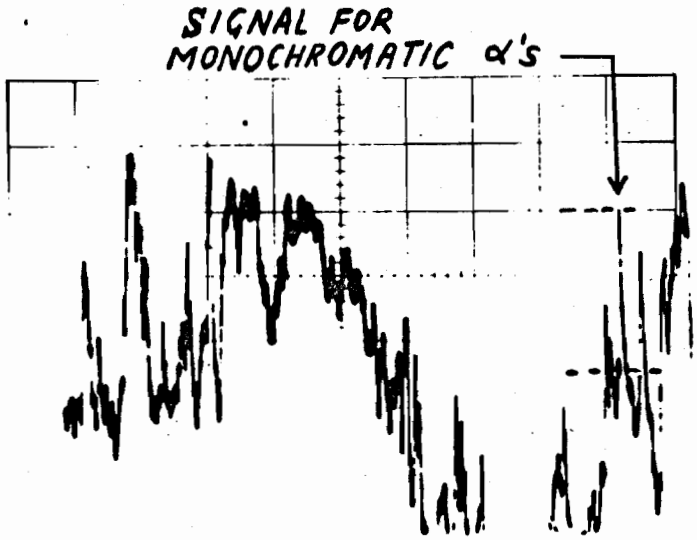
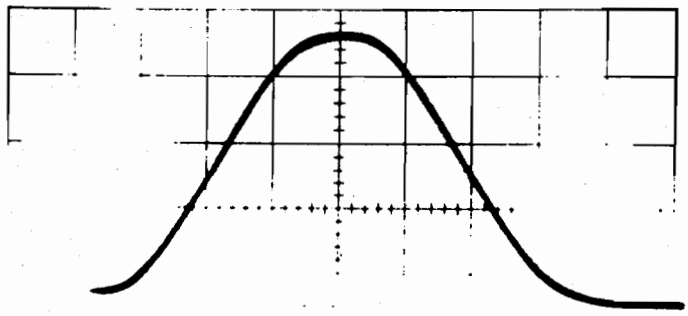
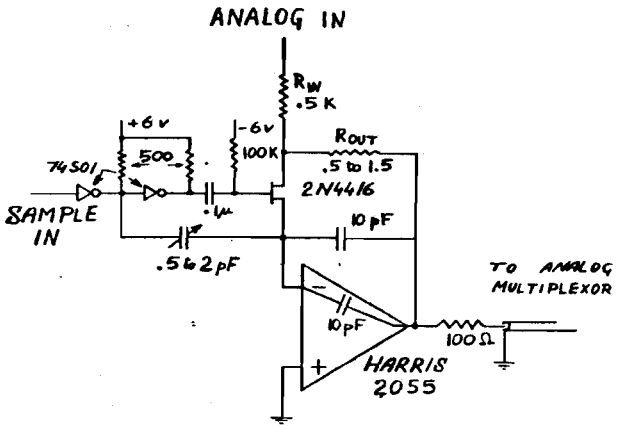


FIG. 5a



ACTIVE FILTER OUTPUT FOR MONOCHROMATIC α's

FIG. 5b



SAMPLE AND HOLD AMPLIFIER

FIG. 6